74LVC332Triple 3-input OR gate Rev. 1 — 20 March 2013

Product data sheet

General description 1.

The 74LVC332 is a triple 3-input OR gate.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

Features and benefits 2.

- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

Ordering information 3.

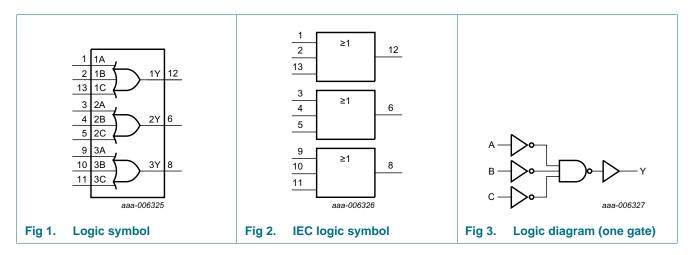
Ordering information Table 1.

Type number	Package	Package									
	Temperature range	Name	Description	Version							
74LVC332D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1							
74LVC332DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1							
74LVC332PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1							
74LVC332BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 \times 3 \times 0.85 mm	SOT762-1							



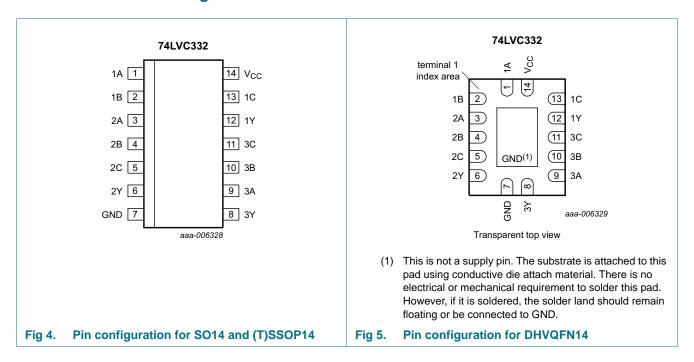
Triple 3-input OR gate

4. Functional diagram



5. Pinning information

5.1 Pinning



Triple 3-input OR gate

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 9	data input
1B, 2B, 3B	2, 4, 10	data input
1C, 2C, 3C	13, 5, 11	data input
1Y, 2Y, 3Y	12, 6, 8	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function selection[1]

Input	nput						
nA	nB	nC	nY				
L	L	L	L				
X	X	Н	Н				
X	Н	X	Н				
Н	X	X	Н				

^[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0	-50	-	mA
V_{I}	input voltage		<u>[1]</u> –0.5	+5.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	±50	mA
Vo	output voltage		<u>[2]</u> –0.5	$V_{CC} + 0.5$	V
I _O	output current	$V_O = 0 V to V_{CC}$	-	±50	mA
I _{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-60	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$	<u>[3]</u> _	500	mW

^[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

^[2] The output voltage ratings may be exceeded if the output current ratings are observed.

^[3] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K. For (T)SSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K. For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly with 4.5 mW/K.

NXP Semiconductors 74LVC332
Triple 3-input OR gate

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V_{CC}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall	V_{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
	rate	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	-	10	ns/V

9. Static characteristics

 Table 6.
 Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	35 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
	input voltage	V _{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V_{IL}	LOW-level	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
	input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	0.8	V
V _{OH} HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}							
	•	$I_O = -100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	V _{CC} - 0.2	-	-	$V_{CC}-0.3$	-	V
		$I_{O} = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	1.05	-	V
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.8	-	-	1.65	-	V
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	V
		$I_{O} = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.25	-	V
		$I_{O} = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.2	-	-	2.0	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	$I_O = 100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	-	-	0.2	-	0.3	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.6	-	0.8	V
		$I_{O} = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
l _l	input leakage current	$V_{CC} = 3.6 \text{ V}; V_I = 5.5 \text{ V or GND}$	-	±0.1	±5	-	±20	μΑ

Triple 3-input OR gate

Table 6. Static characteristics ... continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +85	5 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
I _{CC}	supply current	V_{CC} = 3.6 V; V_{I} = V_{CC} or GND; I_{O} = 0 A	-	0.1	10	-	40	μΑ
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V};$ $V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A}$	-	5	500	-	5000	μА
C _I	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V};$ $V_{I} = \text{GND to } V_{CC}$	-	5.0	-	-	-	pF

^[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 7.

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit	
				Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nA, nB, nC to nY; see Figure 6	[2]						
	V_{CC} = 1.65 V to 1.95 V		0.5	4.6	11.6	0.5	13.4	ns	
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.0	2.7	6.6	1.0	7.6	ns
	$V_{CC} = 2.7 \text{ V}$		1.1	2.8	7.0	1.1	8.1	ns	
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		0.8	2.4	5.9	8.0	6.8	ns
C_{PD}	power dissipation	per gate; $V_I = GND$ to V_{CC}	[3]						
	capacitance	V_{CC} = 1.65 V to 1.95 V		-	8.1	-	-	-	pF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		-	8.2	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		-	9.2	-	-	-	pF

^[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

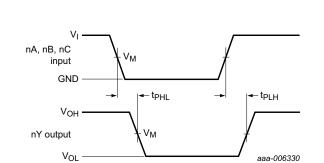
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

^[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

^[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

Triple 3-input OR gate

11. AC waveforms

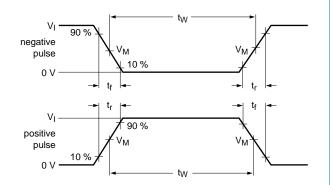


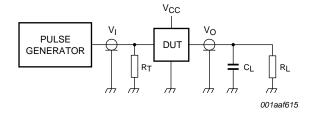
 V_M = 1.5 V at $V_{CC} \ge 2.7$ V

 V_{M} = 0.5 \times V_{CC} at V_{CC} < 2.7 V.

 $\ensuremath{V_{OL}}$ and $\ensuremath{V_{OH}}$ are typical output voltage levels that occur with the output load.

Fig 6. Input (nA, nB and nC) to output (nY) propagation delays





Test data is given in Table 8. Definitions for test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 7. Test circuit for measuring switching times

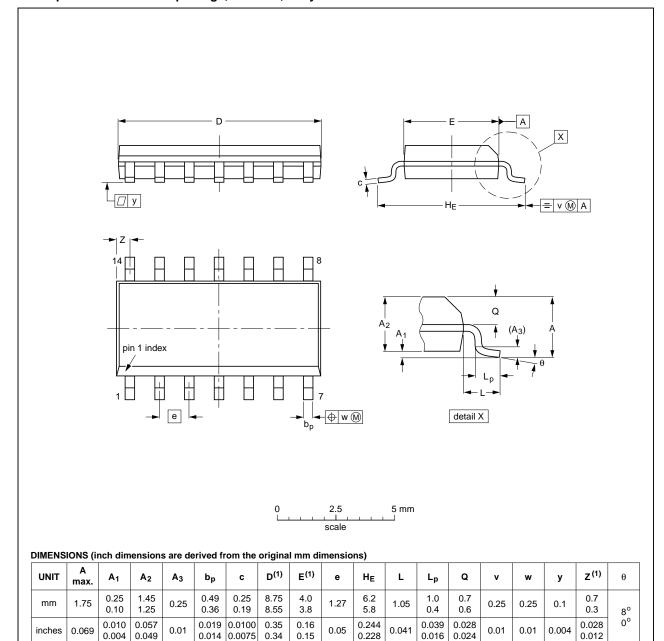
Table 8. Test data

Supply voltage	Input	Load		
	V _I	t _r , t _f	C _L	R _L
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

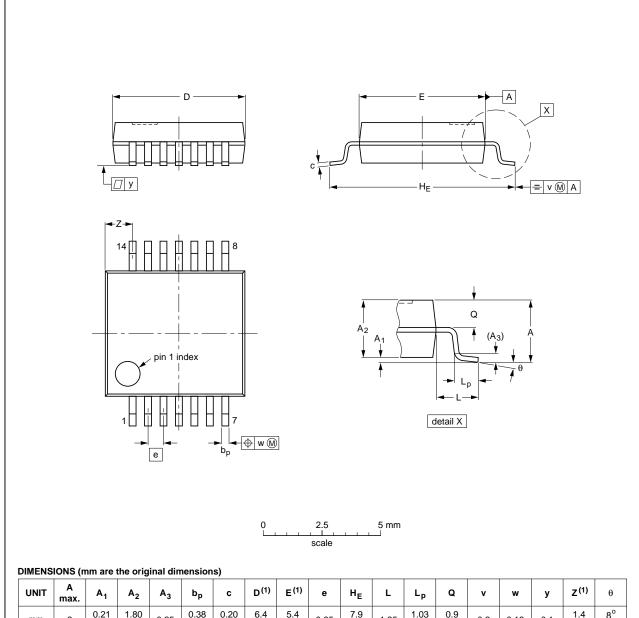
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VERSION	IEC	IEC JEDEC JEITA		PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012			99-12-27 03-02-19	

Fig 8. Package outline SOT108-1 (SO14)

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



	•																	
UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT337-1		MO-150				-99-12-27 03-02-19	

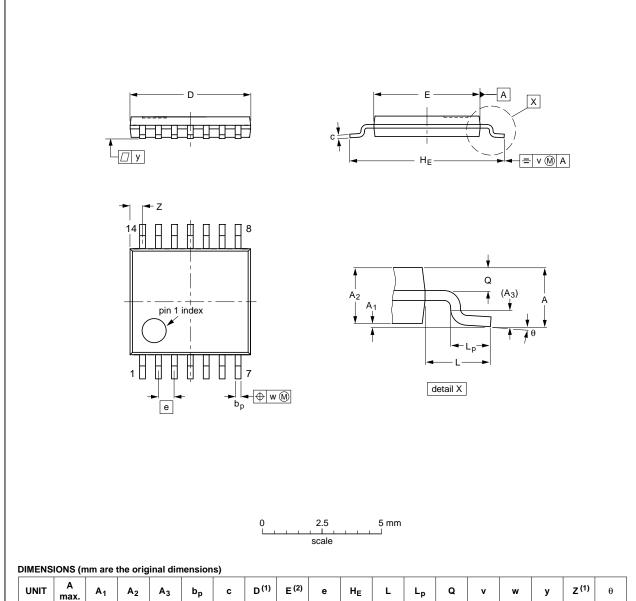
Fig 9. Package outline SOT337-1 (SSOP14)

74LVC332

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

VERSION IEC JEDEC JEITA PROJECTION ISSUE DATE SOT402-1 MO-153 ————————————————————————————————————	OUTLINE		REFER	EUROPEAN	ISSUE DATE			
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	SOT402-1		MO-153					

Fig 10. Package outline SOT402-1 (TSSOP14)

74LVC33

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DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm SOT762-1

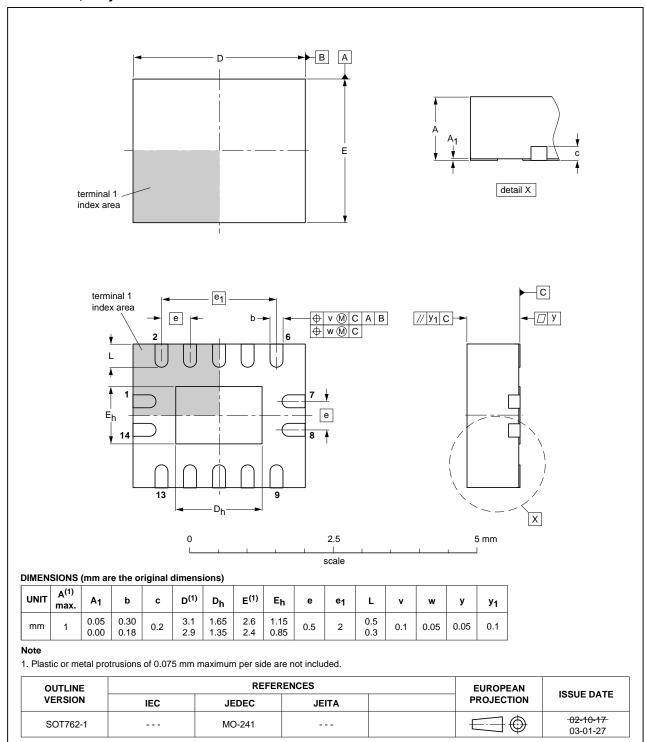


Fig 11. Package outline SOT762-1 (DHVQFN14)

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Triple 3-input OR gate

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC332 v.1	20130320	Product data sheet	-	-

Triple 3-input OR gate

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Triple 3-input OR gate

17. Contents

1	General description
2	Features and benefits
3	Ordering information 1
4	Functional diagram 2
5	Pinning information 2
5.1	Pinning
5.2	Pin description
6	Functional description 3
7	Limiting values
8	Recommended operating conditions 4
9	Static characteristics 4
10	Dynamic characteristics 5
11	AC waveforms 6
12	Package outline
13	Abbreviations11
14	Revision history
15	Legal information
15.1	Data sheet status
15.2	Definitions
15.3	Disclaimers
15.4	Trademarks13
16	Contact information
17	Contents

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