

# 74LVCH322244A

32-bit buffer/line driver; 30  $\Omega$  series termination resistors; 5 V tolerant input/output; 3-state

Rev. 3 — 16 December 2011

Product data sheet

## 1. General description

The 74LVCH322244A is a 32-bit non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $\overline{nOE}$ . A HIGH on input  $\overline{nOE}$  causes the outputs to assume a high-impedance OFF-state.

The device is designed with 30  $\Omega$  series termination resistors in both HIGH and LOW output stages to reduce line noise.

To ensure the high-impedance state during power-up or power-down, input  $\overline{nOE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3 V or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 V and 5 V environment.

Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

## 2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- Integrated 30  $\Omega$  termination resistors
- All data inputs have bus hold
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-B exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$



■ Packaged in plastic fine-pitch ball grid array package

3. Ordering information

Table 1: Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVCH322244AEC	−40 °C to +85 °C	LFBGA96	plastic low profile fine pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

4. Functional diagram

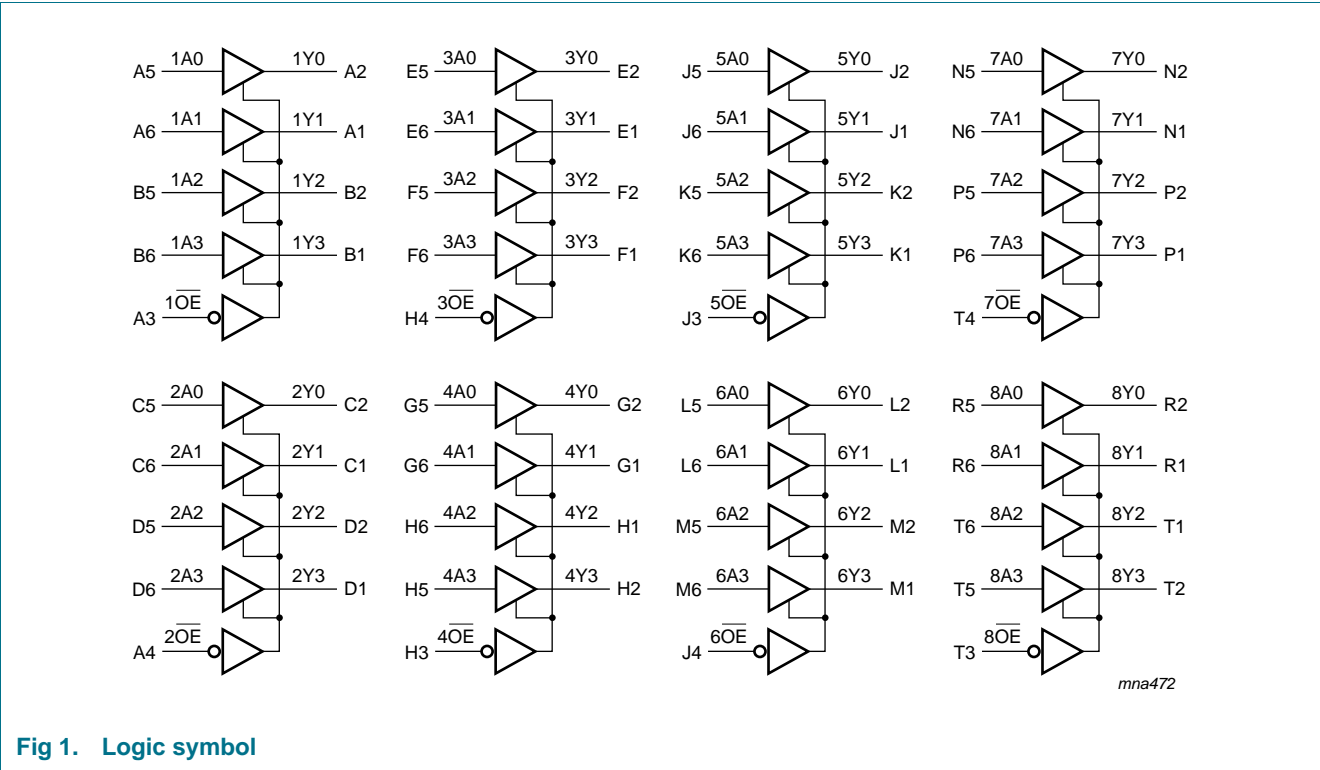


Fig 1. Logic symbol

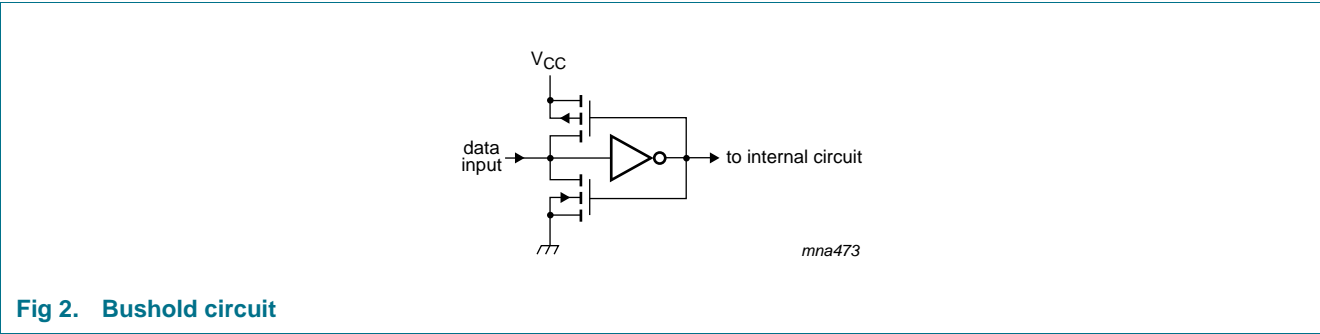


Fig 2. Bushold circuit

## 5. Pinning information

### 5.1 Pinning

*mna471*

6	1A1	1A3	2A1	2A3	3A1	3A3	4A1	4A2	5A1	5A3	6A1	6A3	7A1	7A3	8A1	8A2
5	1A0	1A2	2A0	2A2	3A0	3A2	4A0	4A3	5A0	5A2	6A0	6A2	7A0	7A2	8A0	8A3
4	2 $\overline{\text{OE}}$	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	3 $\overline{\text{OE}}$	6 $\overline{\text{OE}}$	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	7 $\overline{\text{OE}}$
3	1 $\overline{\text{OE}}$	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	4 $\overline{\text{OE}}$	5 $\overline{\text{OE}}$	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	8 $\overline{\text{OE}}$
2	1Y0	1Y2	2Y0	2Y2	3Y0	3Y2	4Y0	4Y3	5Y0	5Y2	6Y0	6Y2	7Y0	7Y2	8Y0	8Y3
1	1Y1	1Y3	2Y1	2Y3	3Y1	3Y3	4Y1	4Y2	5Y1	5Y3	6Y1	6Y3	7Y1	7Y3	8Y1	8Y2
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

Fig 3. Pin configuration

### 5.2 Pin description

Table 2: Pin description

Ball	Symbol	Description
n $\overline{\text{OE}}$ (n = 1 to 8)	A3, A4, H4, H3, J3 J4, T4, T3	3-state output enable inputs (active LOW)
1A[0:3]	A5, A6, B5, B6	data input
2A[0:3]	C5, C6, D5, D6	
3A[0:3]	E5, E6, F5, F6	
4A[0:3]	G5, G6, H6, H5	
5A[0:3]	J5, J6, K5, K6	
6A[0:3]	L5, L6, M5, M6	
7A[0:3]	N5, N6, P5, P6	
8A[0:3]	R5, R6, T6, T5	
1Y[0:3]	A2, A1, B2, B1	data output
2Y[0:3]	C2, C1, D2, D1	
3Y[0:3]	E2, E1, F2, F1	
4Y[0:3]	G2, G1, H1, H2	
5Y[0:3]	J2, J1, K2, K1	
6Y[0:3]	L2, L1, M2, M1	
7Y[0:3]	N2, N1, P2, P1	
8Y[0:3]	R2, R1, T1, T2	
V <sub>CC</sub>	C3, C4, F3, F4, L3, L4, P3, P4	supply voltage
GND	B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4	ground (0 V)

## 6. Functional description

Table 3: Functional table<sup>[1]</sup>

Input		Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$	-50	-	mA
$V_I$	input voltage		<sup>[1]</sup> -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$	-	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW state	<sup>[2]</sup> -0.5	$V_{CC} + 0.5$	V
		output 3-state	<sup>[2]</sup> -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	200	mA
$I_{GND}$	ground current		-200	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	<sup>[3]</sup> -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 70 °C the value of  $P_{tot}$  derates linearly with 1.8 mW/K.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	output HIGH or LOW state	0	-	$V_{CC}$	V
		output 3-state	0	-	5.5	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to 2.7 V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to 3.6 V	-	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	1.08	-	-	1.08	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	0.65 × V <sub>CC</sub>	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0.12	-	0.12	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = –100 $\mu$ A; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> – 0.2	V <sub>CC</sub>	-	V <sub>CC</sub> – 0.3	-	V
		I <sub>O</sub> = –2 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	1.05	-	V
		I <sub>O</sub> = –4 mA; V <sub>CC</sub> = 2.3 V	1.8	-	-	1.65	-	V
		I <sub>O</sub> = –6 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	2.05	-	V
		I <sub>O</sub> = –12 mA; V <sub>CC</sub> = 3.0 V	2.2	-	-	2.0	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
		I <sub>O</sub> = 100 $\mu$ A; V <sub>CC</sub> = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I <sub>O</sub> = 2 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.65	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 2.3 V	-	-	0.6	-	0.8	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.6	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.8	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V or GND <sup>[2]</sup>	-	±0.1	±5	-	±20	$\mu$ A
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 5.5 V or GND; <sup>[2]</sup>	-	±0.1	±5	-	±20	$\mu$ A
I <sub>OFF</sub>	power-off leakage supply	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V	-	±0.1	±10	-	±20	$\mu$ A
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	40	-	160	$\mu$ A
$\Delta$ I <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0 A	-	5	500	-	5000	$\mu$ A
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5.0	-	-	-	pF
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 1.65 V; V <sub>I</sub> = 0.58 V <sup>[3][4]</sup>	10	-	-	10	-	$\mu$ A
		V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 0.7 V	30	-	-	25	-	$\mu$ A
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 0.8 V	75	-	-	60	-	$\mu$ A

**Table 6.** Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 1.65 V; V <sub>I</sub> = 1.07 V <a href="#">[3][4]</a>	–10	-	-	–10	-	$\mu$ A
		V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 1.7 V	–30	-	-	–25	-	$\mu$ A
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 2.0 V	–75	-	-	–60	-	$\mu$ A
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 1.95 V <a href="#">[3][5]</a>	200	-	-	200	-	$\mu$ A
		V <sub>CC</sub> = 2.7 V	300	-	-	300	-	$\mu$ A
		V <sub>CC</sub> = 3.6 V	500	-	-	500	-	$\mu$ A
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 1.95 V <a href="#">[3][5]</a>	–200	-	-	–200	-	$\mu$ A
		V <sub>CC</sub> = 2.7 V	–300	-	-	–300	-	$\mu$ A
		V <sub>CC</sub> = 3.6 V	–500	-	-	–500	-	$\mu$ A

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.[2] The bus hold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub>, allowing 5.5 V on the input terminal.

[3] Valid for data inputs only. Note that control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

## 10. Dynamic characteristics

**Table 7.** Dynamic characteristicsVoltages are referenced to GND (ground = 0 V). For test circuit see [Figure 6](#).

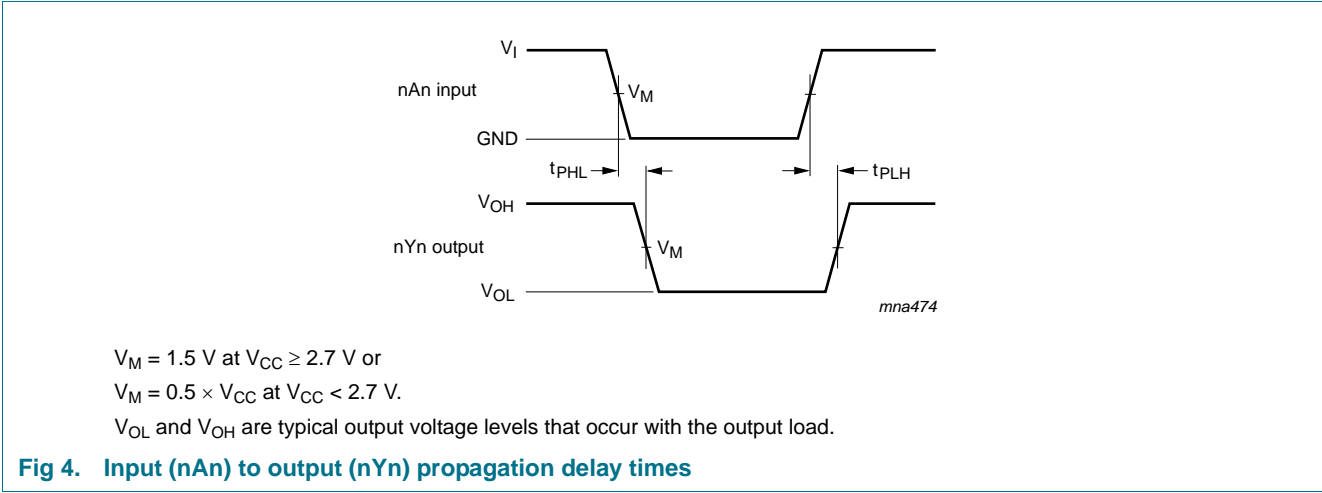
Symbol	Parameter	Conditions	T <sub>amb</sub> = –40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nAn to nYn; see <a href="#">Figure 4</a> <a href="#">[2]</a>						
		V <sub>CC</sub> = 1.2 V	-	11.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	6.0	15.0	1.5	17.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.2	7.4	1.0	8.2	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.3	6.7	1.0	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.7	5.8	1.0	7.5	ns
t <sub>en</sub>	enable time	n $\overline{\text{OE}}$ to nYn; see <a href="#">Figure 5</a> <a href="#">[2]</a>						
		V <sub>CC</sub> = 1.2 V	-	15.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.7	6.8	15.3	1.7	17.7	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	3.8	8.0	1.5	8.9	ns
		V <sub>CC</sub> = 2.7 V	1.5	4.2	7.6	1.5	9.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.1	6.0	1.0	7.5	ns
t <sub>dis</sub>	disable time	n $\overline{\text{OE}}$ to nYn; see <a href="#">Figure 5</a> <a href="#">[2]</a>						
		V <sub>CC</sub> = 1.2 V	-	10.0	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.2	3.9	8.2	2.2	9.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	2.1	4.4	0.5	5.0	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.1	4.7	1.5	6.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.5	2.8	4.5	1.5	6.0	ns

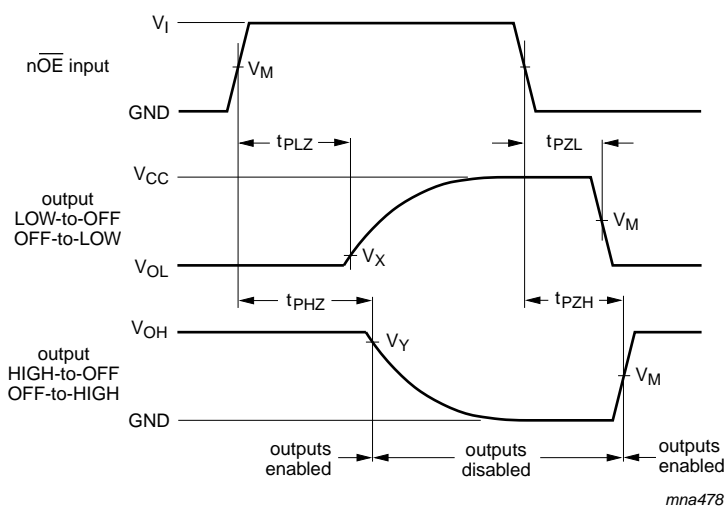
Table 7. Dynamic characteristics ...continued  
Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 6.

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>sk(o)</sub>	output skew time	V <sub>CC</sub> = 3.0 V to 3.6 V <sup>[3]</sup>	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation capacitance	per flip-flop; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[4]</sup>						
		outputs enabled						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	4.8	-	-	-	pF
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	8.3	-	-	-	pF
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	11.4	-	-	-	pF

- [1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:  
f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz  
C<sub>L</sub> = output load capacitance in pF  
V<sub>CC</sub> = supply voltage in Volts  
N = number of inputs switching  
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs

11. AC waveforms





$V_M = 1.5 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$ ;

$V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7 \text{ V}$ .

$V_X = V_{OL} + 0.3 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$  or

$V_X = V_{OL} + 0.1 \text{ V}$  at  $V_{CC} < 2.7 \text{ V}$ .

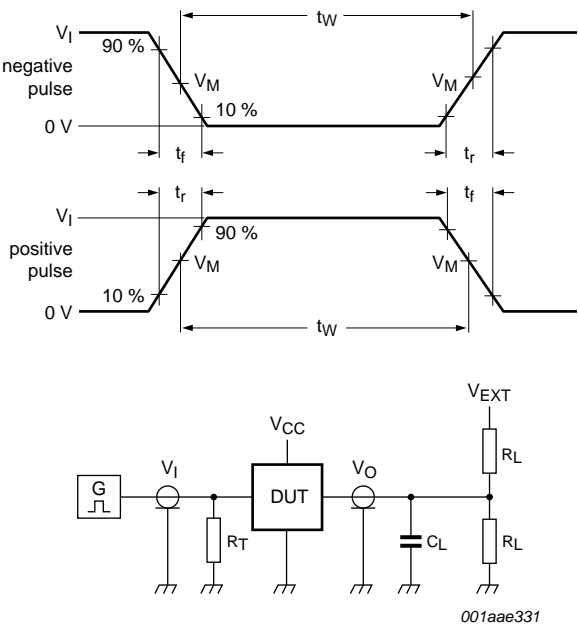
$V_Y = V_{OH} - 0.3 \text{ V}$  at  $V_{CC} \geq 2.7 \text{ V}$  or

$V_Y = V_{OH} - 0.1 \text{ V}$  at  $V_{CC} < 2.7 \text{ V}$ .

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 5. 3-state enable and disable times**





Test data is given in [Table 8](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 6. Load circuitry for switching times**

**Table 8. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1

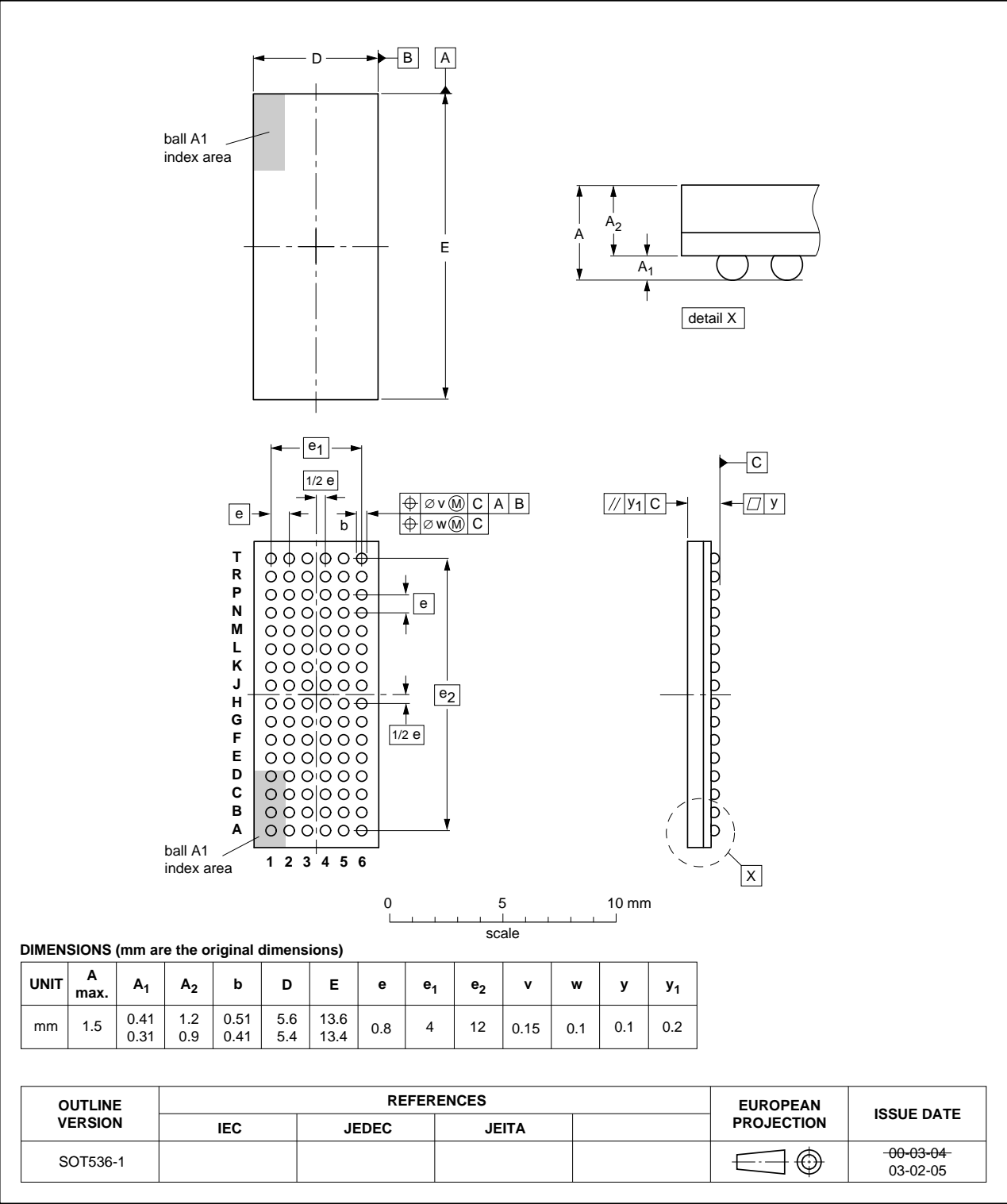


Fig 7. Package outline SOT536-1 (LFBGA96)

## 13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCH322244A v.3	20111216	Product data sheet	-	74LVCH322244A v.2
Modifications:	<ul style="list-style-type: none"><li>The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li><a href="#">Table 4</a>, <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a> and <a href="#">Table 8</a>: values added for lower voltage ranges.</li></ul>			
74LVCH322244A v.2	20040519	Product specification	-	74LVCH322244A v.1
74LVCH322244A v.1	19991124	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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