

# DATA SHEET

**74LVT00**

3.3V Quad 2-input NAND gate

Product specification

1996 Aug 15

IC24 Data Handbook

3.3V Quad 2-input NAND gate

74LVT00

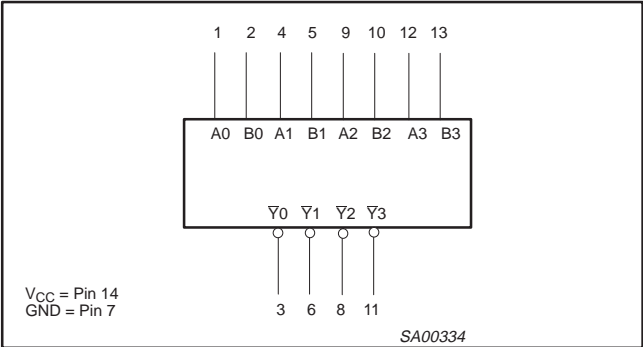
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{\text{amb}} = 25^{\circ}\text{C}$ ; $\text{GND} = 0\text{V}$	TYPICAL	UNIT
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay An or Bn to $\bar{Y}_n$	$C_L = 50\text{pF}$ ; $V_{\text{CC}} = 3.3\text{V}$	2.7 2.7	ns
$C_{\text{IN}}$	Input capacitance	$V_I = 0\text{V}$ or $3.0\text{V}$	3	pF
$I_{\text{CCL}}$	Total supply current	Outputs Low; $V_{\text{CC}} = 3.6\text{V}$	1	mA

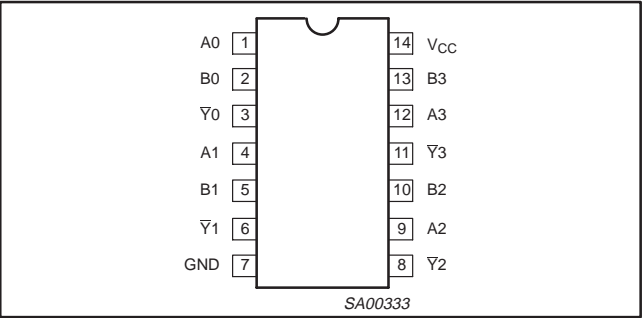
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
14-Pin Plastic SO	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVT00 D	74LVT00 D	SOT108-1
14-Pin Plastic SSOP	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVT00 DB	74LVT00 DB	SOT337-1
14-Pin Plastic TSSOP	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVT00 PW	74LVT00PW DH	SOT402-1

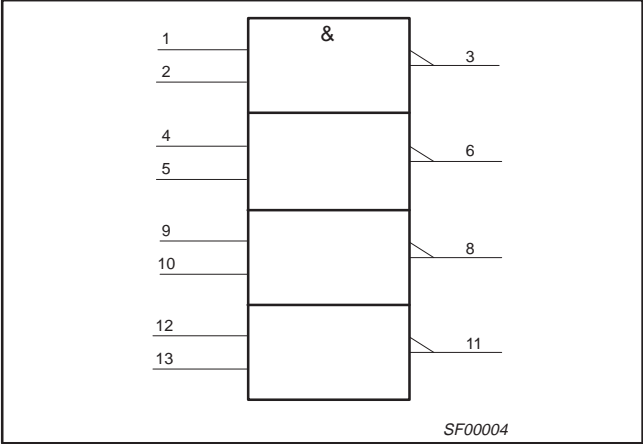
LOGIC SYMBOL



PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



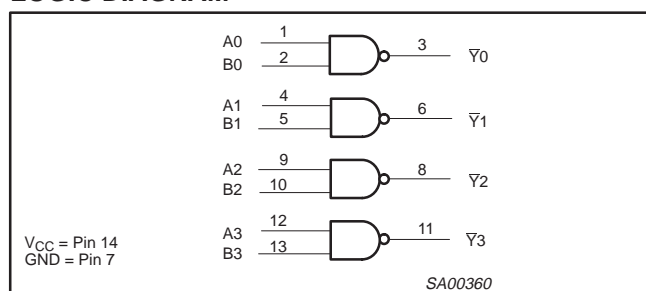
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 4, 5, 9, 10, 12, 13	An-Bn	Data inputs
3, 6, 8, 11	$\bar{Y}_n$	Data outputs
7	GND	Ground (0V)
14	V <sub>CC</sub>	Positive supply voltage

## 3.3V Quad 2-input NAND gate

74LVT00

## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS		OUTPUT
Dna	Dnb	Qn
L	L	H
L	H	H
H	L	H
H	H	L

## NOTES:

H = High voltage level  
L = Low voltage level

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		−0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	−50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		−0.5 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	−50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or High state	−0.5 to +7.0	V
I <sub>OUT</sub>	DC output current	Output in High state	−32	mA
		Output in Low state	64	
T <sub>stg</sub>	Storage temperature range		−65 to 150	°C

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V <sub>CC</sub>	DC supply voltage	2.7	3.6	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0		V
V <sub>IL</sub>	Low-level Input voltage		0.8	V
I <sub>OH</sub>	High-level output current		−20	mA
I <sub>OL</sub>	Low-level output current		32	mA
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	−40	+85	°C

## 3.3V Quad 2-input NAND gate

74LVT00

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 2.7V; I <sub>IK</sub> = −18mA			−1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 2.7 to 3.6V; I <sub>OH</sub> = −100μA	V <sub>CC</sub> −0.2			V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = −6mA	2.4			
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = −20mA	2.0			
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 100μA			0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 24mA			0.5	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 32mA			0.5	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 0 or 3.6V; V <sub>I</sub> = 5.5V			10	μA
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND			±1	
I <sub>OFF</sub>	Output off current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5V			±100	μA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0			0.02	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 3.6V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		1	2	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 3V to 3.6V; One input at V <sub>CC</sub> −0.6V, Other inputs at V <sub>CC</sub> or GND			0.2	μA
C <sub>I</sub>	Input capacitance	V <sub>I</sub> = 3V or 0		3		pF

**NOTES:**

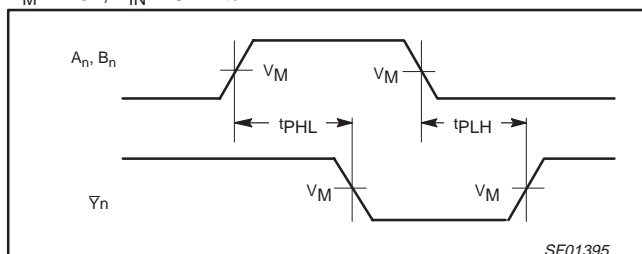
1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ C$ .
2. This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

**AC CHARACTERISTICS**GND = 0V;  $t_R = t_F = 2.5ns$ ;  $C_L = 50pF$ ,  $R_L = 500\Omega$ ;  $T_{amb} = -40^\circ C$  to  $+85^\circ C$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP <sup>1</sup>	MAX	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay An or Bn to $\bar{Y}_n$	1	1.0 1.0	2.7 2.7	4.1 3.9	5.0 3.8	ns

**NOTE:**

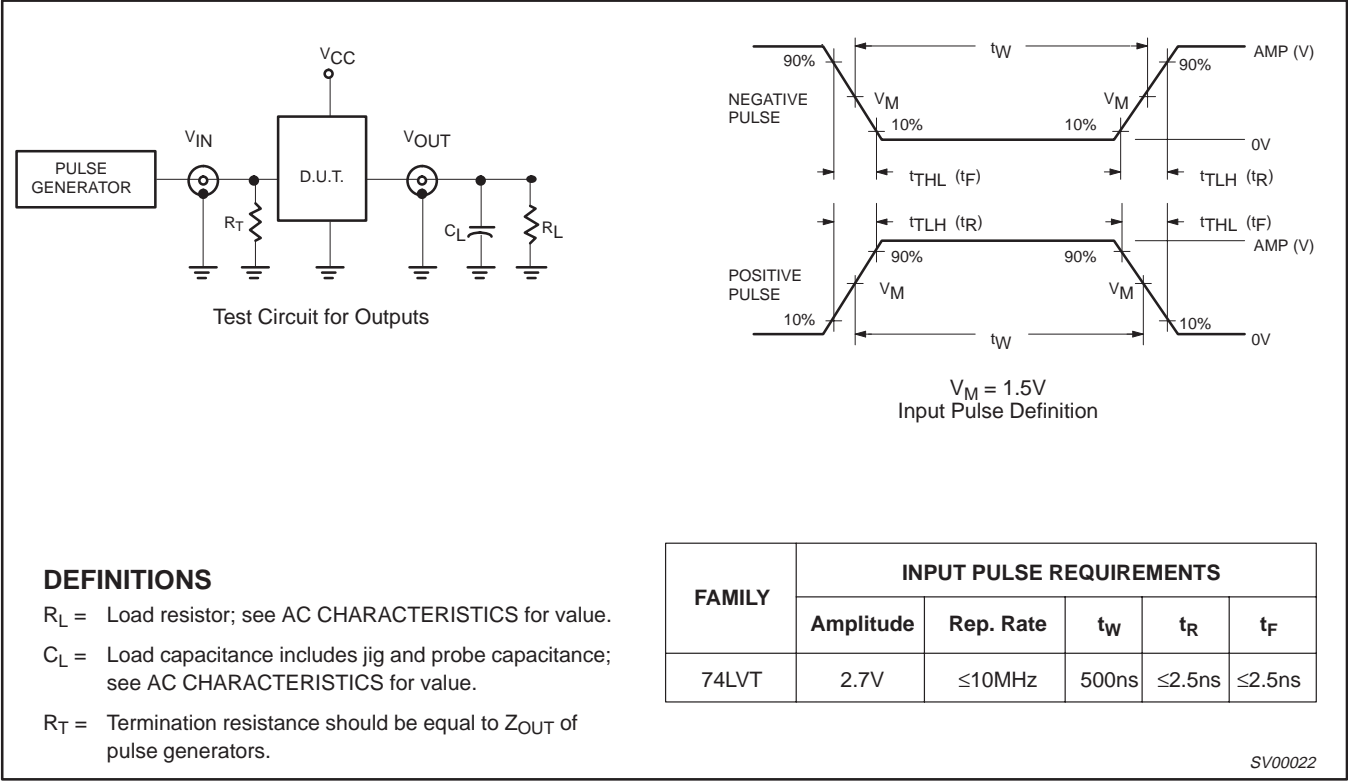
1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ C$ .

**AC WAVEFORMS** $V_M = 1.5V$ ,  $V_{IN} = GND$  to  $2.7V$ **Waveform 1. Propagation delay for inverting outputs**

3.3V Quad 2-input NAND gate

74LVT00

TEST CIRCUIT AND WAVEFORMS

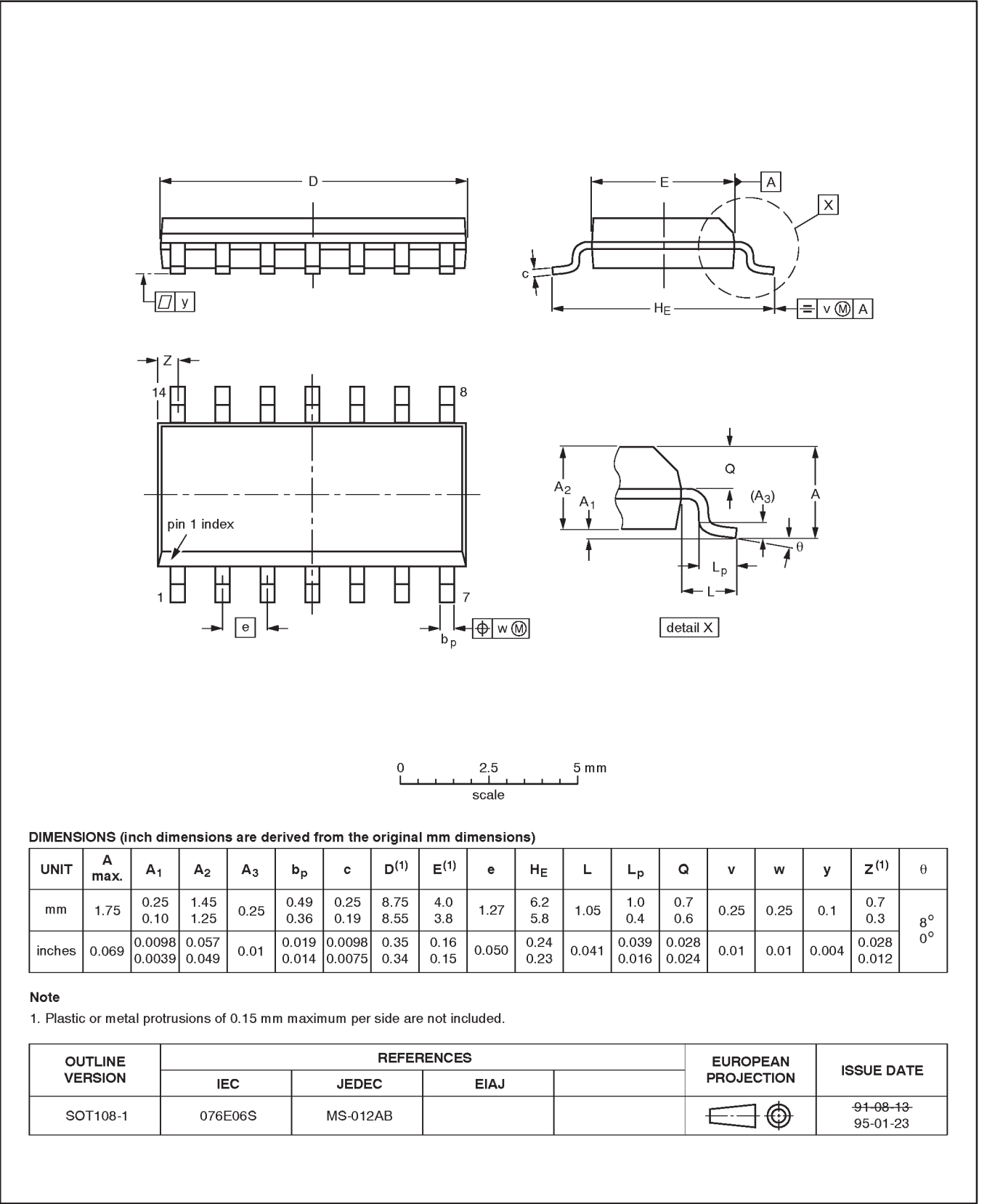


3.3V Quad 2-input NAND gate

74LVT00

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

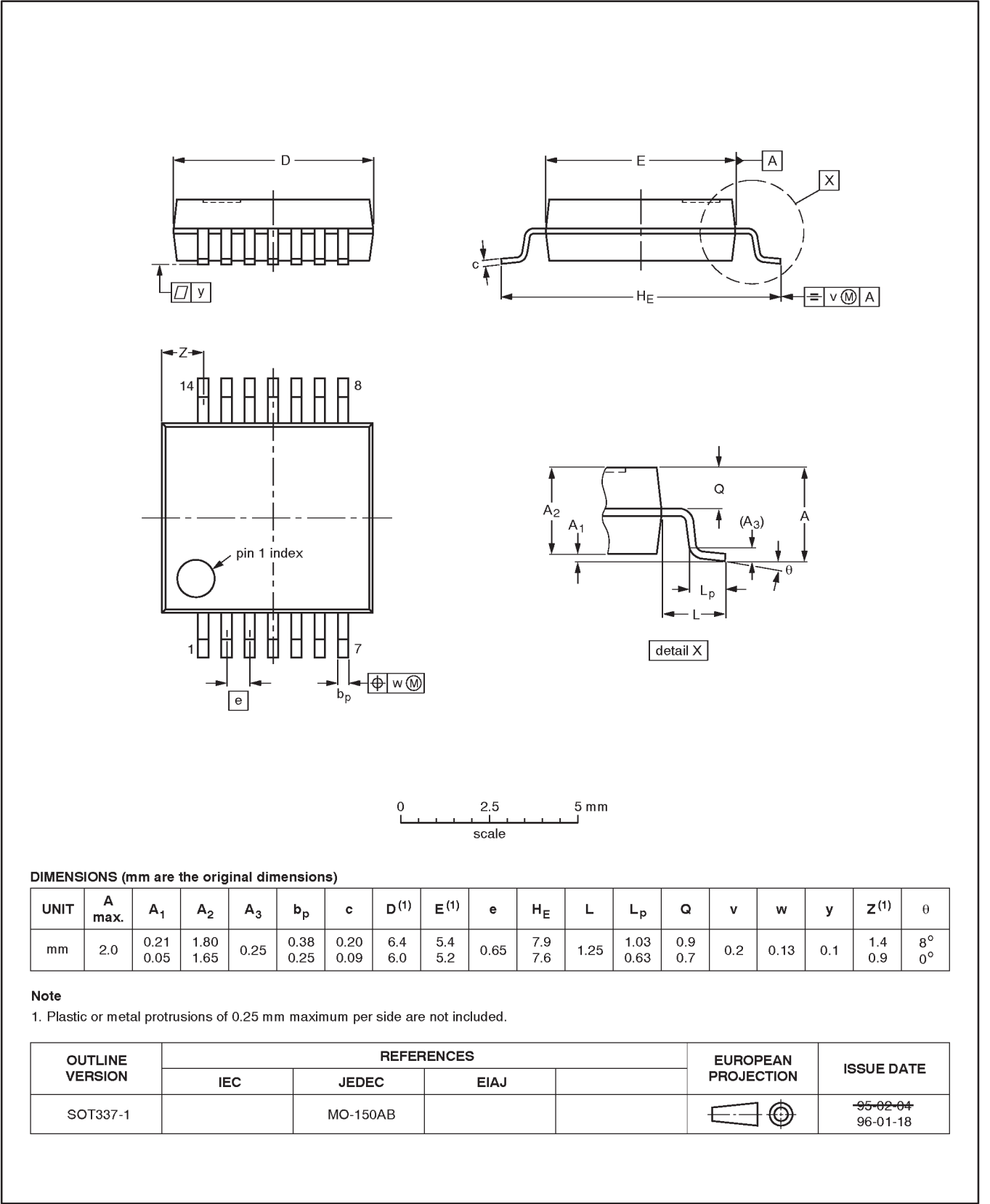


3.3V Quad 2-input NAND gate

74LVT00

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

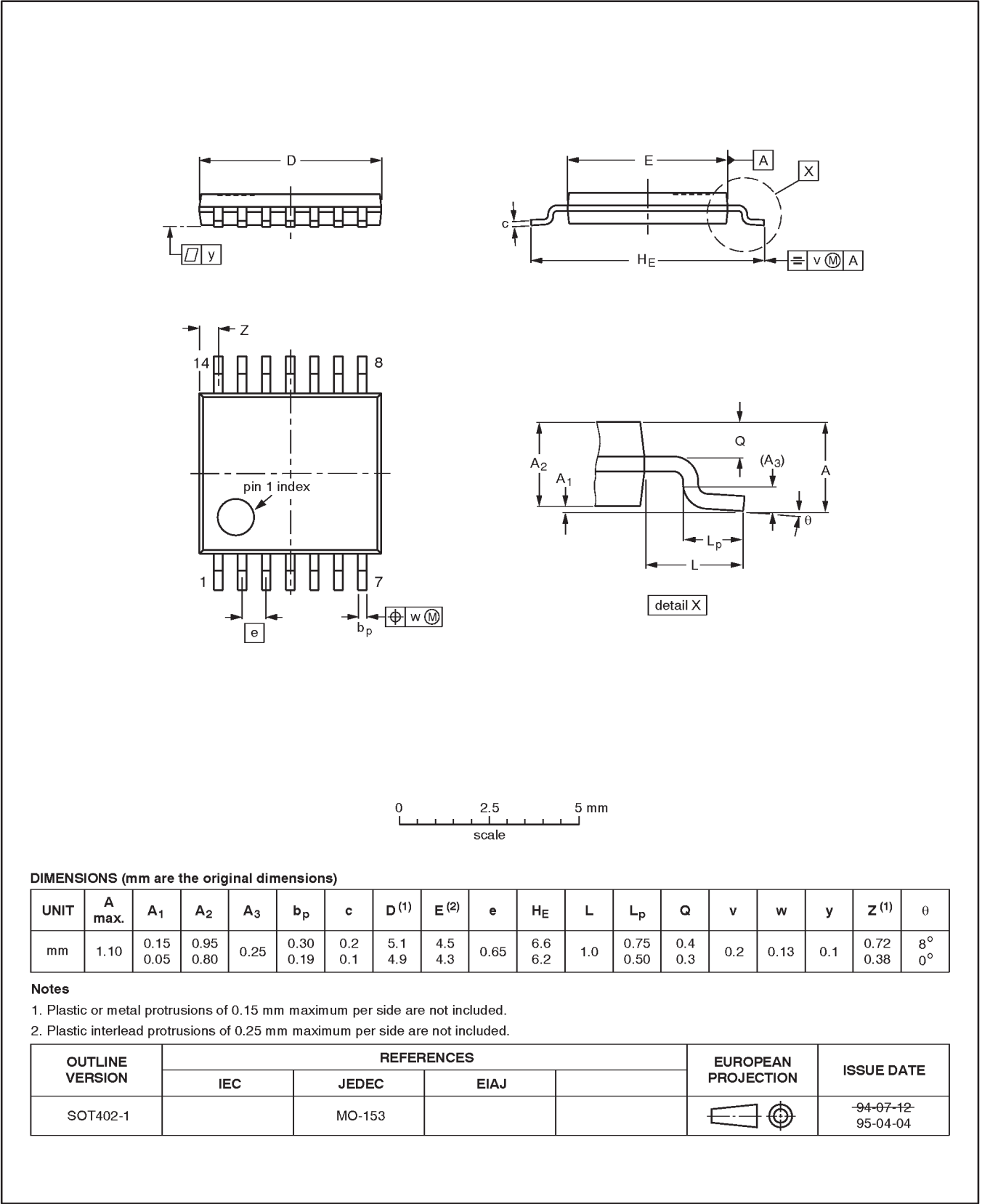


3.3V Quad 2-input NAND gate

74LVT00

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1





---

3.3V Quad 2-input NAND gate74LVT00

---

**NOTES**

3.3V Quad 2-input NAND gate

74LVT00

DEFINITIONS		
Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Philips Semiconductors and Philips Electronics North America Corporation reserve the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**LIFE SUPPORT APPLICATIONS**  
Philips Semiconductors and Philips Electronics North America Corporation Products are not designed for use in life support appliances, devices, or systems where malfunction of a Philips Semiconductors and Philips Electronics North America Corporation Product can reasonably be expected to result in a personal injury. Philips Semiconductors and Philips Electronics North America Corporation customers using or selling Philips Semiconductors and Philips Electronics North America Corporation Products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors and Philips Electronics North America Corporation for any damages resulting from such improper use or sale.