

74LVTH32245

3.3 V 32-bit bus transceiver; 3-state

Rev. 01 — 23 January 2008

Product data sheet

1. General description

The 74LVTH32245 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V. The 74LVTH32245 is a 32-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features four output enable (\overline{nOE}) inputs for easy cascading and four send/receive ($nDIR$) inputs for direction control. Pin \overline{nOE} controls the outputs so that the buses are effectively isolated. Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features

- 32-bit bidirectional bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
 - ◆ JESD78 Class II level A exceeds 500 mA
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVTH32245EC	-40 °C to +85 °C	LFPGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

4. Functional diagram

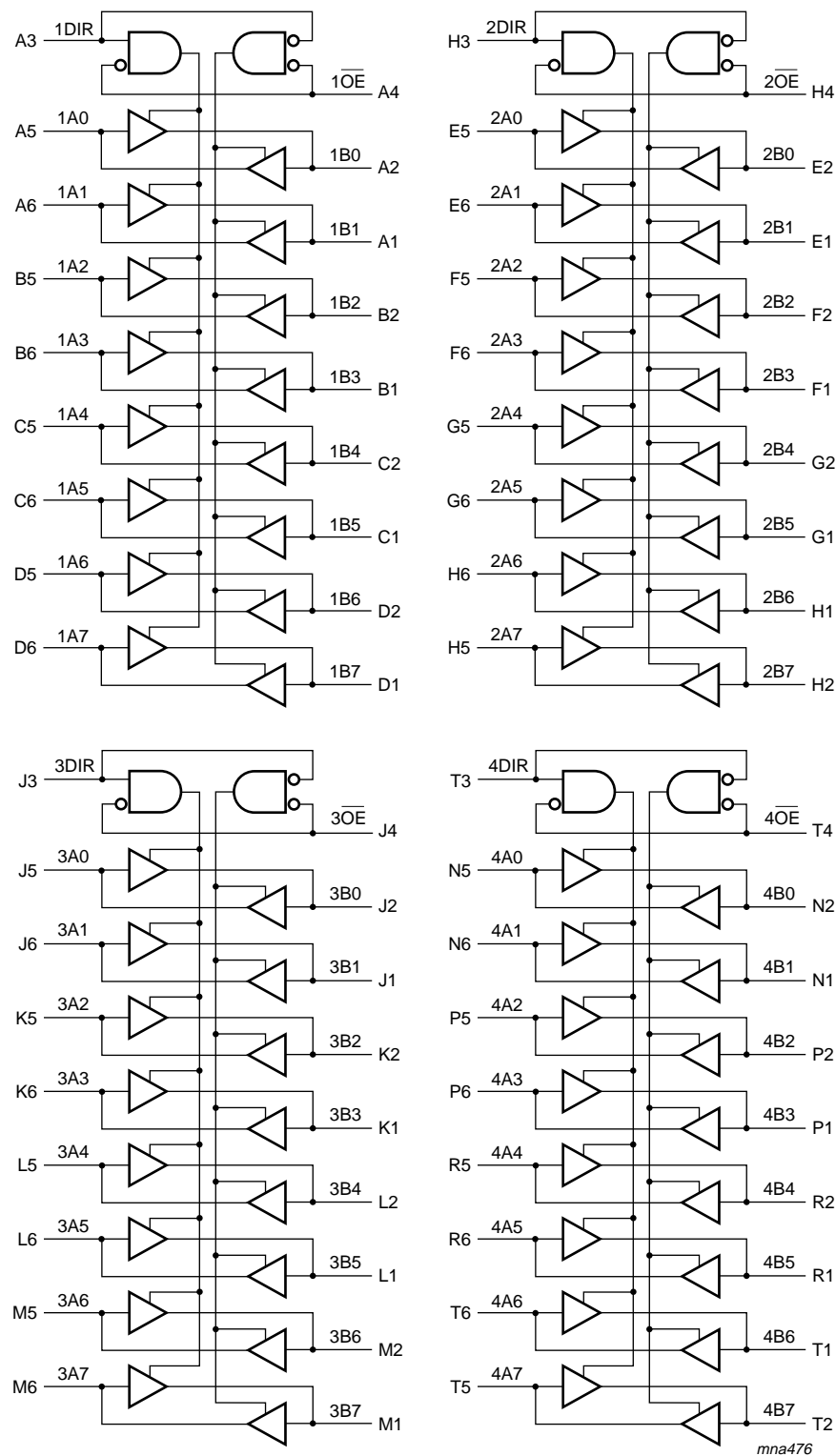
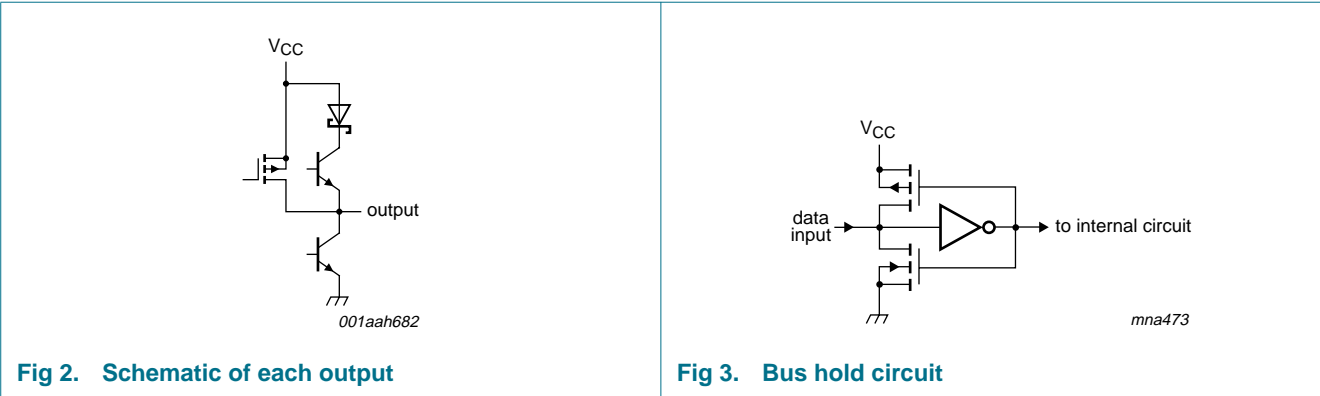


Fig 1. Logic symbol



5. Pinning information

5.1 Pinning

6

1A1

1A3

1A5

1A7

2A1

2A3

2A5

2A6

3A1

3A3

3A5

3A7

4A1

4A3

4A5

4A6

5

1A0

1A2

1A4

1A6

2A0

2A2

2A4

2A7

3A0

3A2

3A4

3A6

4A0

4A2

4A4

4A7

4

1OE

GND

VCC

GND

GND

VCC

GND

2OE

3OE

GND

VCC

GND

GND

VCC

GND

4OE

3

1DIR

GND

VCC

GND

GND

VCC

GND

2DIR

3DIR

GND

VCC

GND

GND

VCC

GND

4DIR

2

1B0

1B2

1B4

1B6

2B0

2B2

2B4

2B7

3B0

3B2

3B4

3B6

4B0

4B2

4B4

4B7

1

1B1

1B3

1B5

1B7

2B1

2B3

2B5

2B6

3B1

3B3

3B5

3B7

4B1

4B3

4B5

4B6

A

B

C

D

E

F

G

H

J

K

L

M

N

P

R

T

mna475

Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Ball	Description
nDIR (n = 1 to 4)	A3, H3, J3, T3	direction control
nOE (n = 1 to 4)	A4, H4, J4, T4	output enable input (active LOW)
1A[0:7]	A5, A6, B5, B6, C5, C6, D5, D6	input or output
1B[0:7]	A2, A1, B2, B1, C2, C1, D2, D1	input or output
2A[0:7]	E5, E6, F5, F6, G5, G6, H6, H5	input or output
2B[0:7]	E2, E1, F2, F1, G2, G1, H1, H2	input or output
3A[0:7]	J5, J6, K5, K6, L5, L6, M5, M6	input or output
3B[0:7]	J2, J1, K2, K1, L2, L1, M2, M1	input or output
4A[0:7]	N5, N6, P5, P6, R5, R6, T6, T5	input or output

Table 2. Pin description ...continued

Symbol	Ball	Description
4B[0:7]	N2, N1, P2, P1, R2, R1, T1, T2	input or output
GND	B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4	ground (0 V)
V _{CC}	C3, C4, F3, F4, L3, L4, P3, P4	supply voltage

6. Functional description

Table 3. Function selection^[1]

Input		Input/output	
nOE	nDIR	nAn	nBn
L	L	nAn = nBn	inputs
L	H	inputs	nBn = nAn
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)^{[1][2]}

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage		^[3] -0.5	+7.0	V
V _O	output voltage	output in OFF or HIGH-state	^[3] -0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		-	150	°C

[1] Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond indicated under [Section 8 "Recommended operating conditions"](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[3] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.7	-	3.6	V
V _I	input voltage		0	-	5.5	V
I _{OH}	HIGH-level output current		-32	-	-	mA
I _{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	64	mA
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V
P _{tot}	total power dissipation		[1] -	-	1000	mW

[1] Above 70 °C the value of P_{tot} derates linearly with 1.8 mW/K.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C [1]						
V _{IK}	input clamping voltage	V _{CC} = 2.7 V; I _{IK} = -18 mA	-1.2	-0.85	-	V
V _{IH}	HIGH-level input voltage		2.0	-	-	V
V _{IL}	LOW-level input voltage		-	-	0.8	V
V _{OH}	HIGH-level output voltage	V _{CC} = 2.7 V to 3.6 V; I _{OH} = -100 μA	V _{CC} - 0.2	V _{CC}	-	V
		V _{CC} = 2.7 V; I _{OH} = -8 mA	2.4	2.5	-	V
		V _{CC} = 3.0 V; I _{OH} = -32 mA	2.0	2.3	-	V
V _{OL}	LOW-level output voltage	V _{CC} = 2.7 V; I _{OL} = 100 μA	-	0.07	0.2	V
		V _{CC} = 2.7 V; I _{OL} = 24 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 16 mA	-	0.25	0.4	V
		V _{CC} = 3.0 V; I _{OL} = 32 mA	-	0.3	0.5	V
		V _{CC} = 3.0 V; I _{OL} = 64 mA	-	0.4	0.55	V
I _I	input leakage current	control pins				
		V _{CC} = 3.6 V; V _I = V _{CC} or GND	-	0.1	±1	μA
		V _{CC} = 0 V or 3.6 V; V _I = 5.5 V	-	0.1	10	μA
		input/output data pins; V _{CC} = 3.6 V	[2]			
		V _I = 5.5 V	-	0.1	20	μA
		V _I = V _{CC}	-	0.5	10	μA
I _{OFF}	power-off leakage current	V _I = 0 V	-5	-0.1	-	μA
		V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	0.1	±100	μA
		V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V	-	0.1	±100	μA
I _{LO}	output leakage current	output HIGH; V _O = 5.5 V; V _{CC} = 3.0 V	-	75	125	μA
I _{O(pu/pd)}	power-up/power-down output current	V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; nOE = don't care	[4] -	40	±100	μA

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{BHL}	bus hold LOW current	$V_{CC} = 3\text{ V}$; $V_I = 0.8\text{ V}$	75	135	-	μA
I_{BHH}	bus hold HIGH current	$V_{CC} = 3\text{ V}$; $V_I = 2.0\text{ V}$	-	-135	-75	μA
I_{BHLO}	bus hold LOW overdrive current	$V_{CC} = 0\text{ V to } 3.6\text{ V}$; $V_I = 3.6\text{ V}$	[3] 500	-	-	μA
I_{BHHO}	bus hold HIGH overdrive current	$V_{CC} = 0\text{ V to } 3.6\text{ V}$; $V_I = 3.6\text{ V}$	[3] -	-	-500	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = \text{GND or } V_{CC}$; $I_O = 0\text{ A}$				
		outputs HIGH	-	0.14	0.24	mA
		outputs LOW	-	8.4	12	mA
		outputs disabled	[5] -	0.14	0.24	mA
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 3\text{ V to } 3.6\text{ V}$; one input at $V_{CC} - 0.6\text{ V}$; other inputs at V_{CC} or GND	[6] -	0.1	0.2	mA
C_I	input capacitance	control pins; $V_O = 0\text{ V or } 3.0\text{ V}$	-	3	-	pF
$C_{I/O}$	input/output capacitance	input/output data pins; outputs disabled; $V_{CC} = 3.6\text{ V}$; $I_O = 0\text{ A}$; $V_I = \text{GND or } V_{CC}$	-	9	-	pF

[1] All typical values are at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ }^\circ\text{C}$ unless otherwise specified.[2] Unused pins at V_{CC} or GND.

[3] This is the bus-hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ a transition time of 100 μs is permitted. This parameter is valid for $T_{amb} = 25\text{ }^\circ\text{C}$ only.[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V); for load circuit see [Figure 7](#).

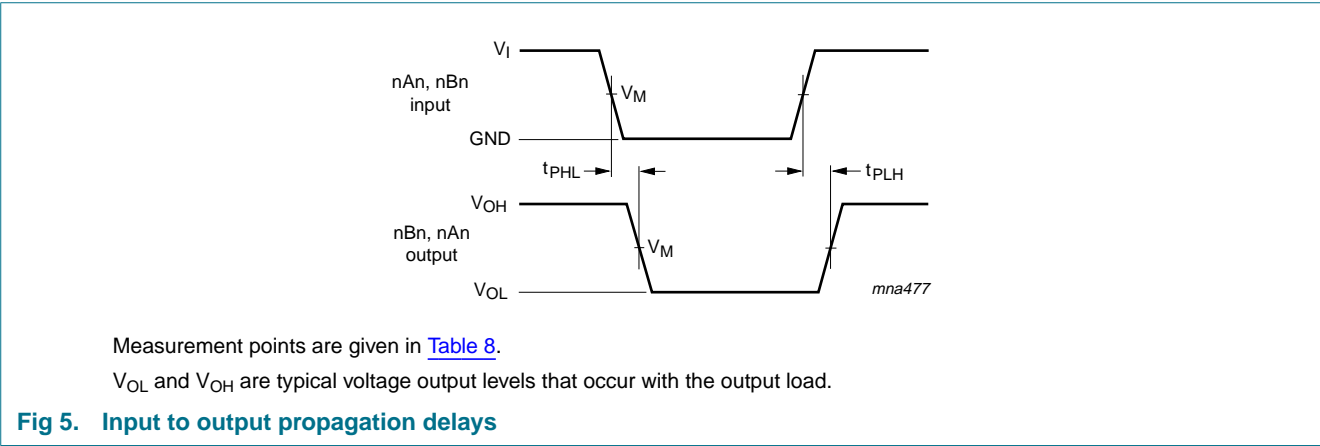
Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$T_{amb} = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$						
t_{PLH}	LOW to HIGH propagation delay	nAn to nBn or nBn to nAn; see Figure 5				
		$V_{CC} = 2.7\text{ V}$	-	-	3.5	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	1.9	3.3	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nBn or nBn to nAn; see Figure 5				
		$V_{CC} = 2.7\text{ V}$	-	-	3.5	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	1.7	3.3	ns
t_{PZH}	OFF-state to HIGH propagation delay	n $\overline{\text{OE}}$ to nAn or nBn; see Figure 6				
		$V_{CC} = 2.7\text{ V}$	-	-	5.3	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	2.8	4.5	ns

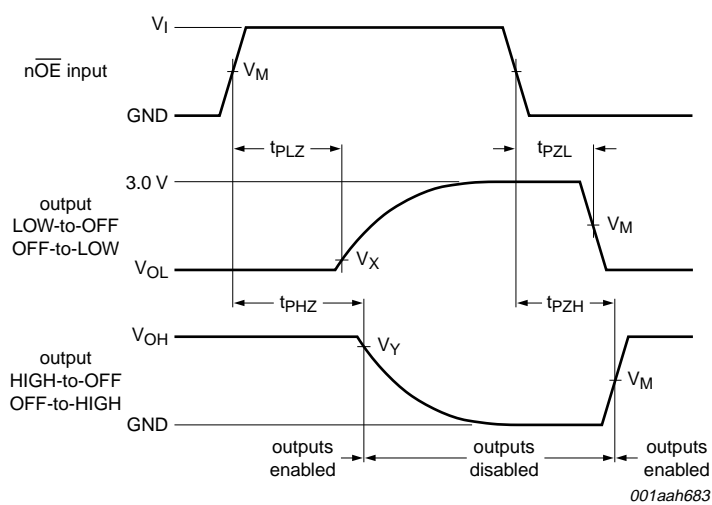
Table 7. Dynamic characteristics ...continued
Voltages are referenced to GND (ground = 0 V); for load circuit see [Figure 7](#).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
t _{PZL}	OFF-state to LOW propagation delay	n $\overline{\text{OE}}$ to nAn or nBn; see Figure 6				
		V _{CC} = 2.7 V	-	-	5.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.8	4.1	ns
t _{PHZ}	HIGH to OFF-state propagation delay	n $\overline{\text{OE}}$ to nAn or nBn; see Figure 6				
		V _{CC} = 2.7 V	-	-	5.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.2	5.1	ns
t _{PLZ}	LOW to OFF-state propagation delay	n $\overline{\text{OE}}$ to nAn or nBn; see Figure 6				
		V _{CC} = 2.7 V	-	-	4.6	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.0	4.6	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Waveforms



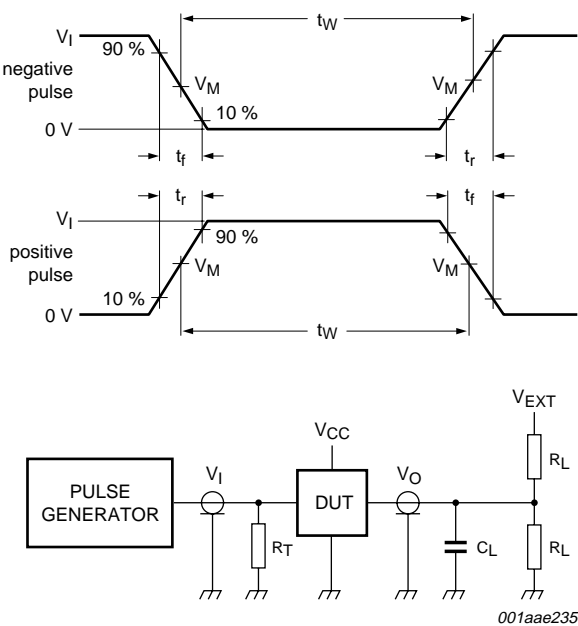


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$



Test data is given in [Table 9](#).
Definitions test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
 V_{EXT} = External voltage for measuring switching times.

Fig 7. Load circuitry for switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	R_L	C_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	500 Ω	50 pF	GND	6 V	open

12. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1

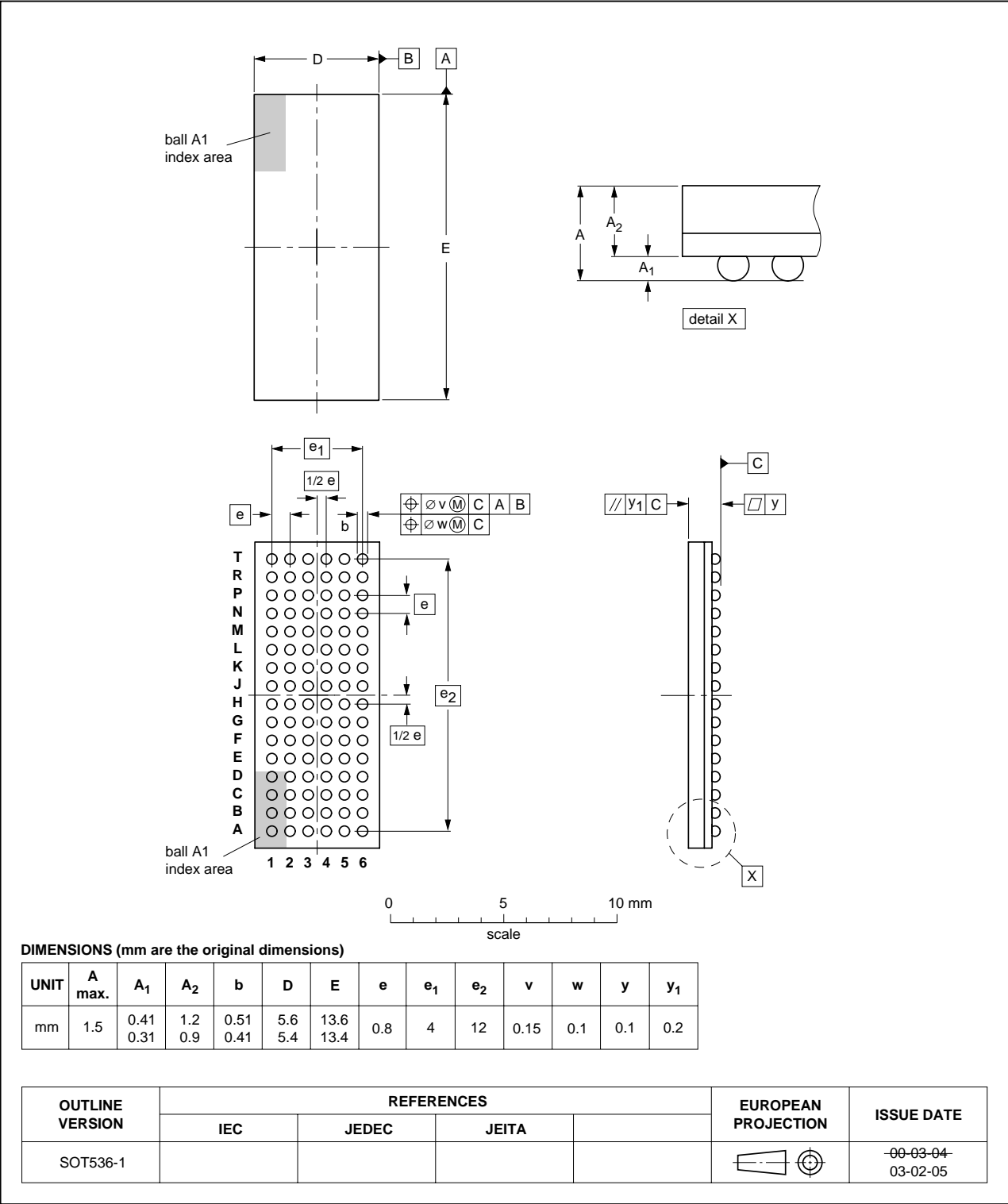


Fig 8. Package outline SOT536-1 (LFBGA96)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVTH32245_1	20080123	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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