

DATA SHEET

BF1100WR Dual-gate MOS-FET

Product specification

1995 Apr 25



Dual-gate MOS-FET

BF1100WR

FEATURES

- Specially designed for use at 9 to 12 V supply voltage
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT343R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g ₂	gate 2
4	g ₁	gate 1

Top view

MAM192

s,b

g₂

g₁

d

Marking code: MF.

Fig.1 Simplified outline (SOT343R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DS}	drain-source voltage		–	–	14	V
I _D	drain current		–	–	30	mA
P _{tot}	total power dissipation		–	–	280	mW
T _j	operating junction temperature		–	–	150	°C
y _{fs}	forward transfer admittance		24	28	33	mS
C _{ig1-s}	input capacitance at gate 1		–	2.2	2.6	pF
C _{rs}	reverse transfer capacitance	f = 1 MHz	–	25	35	fF
F	noise figure	f = 800 MHz	–	2	–	dB

Dual-gate MOS-FET

BF1100WR

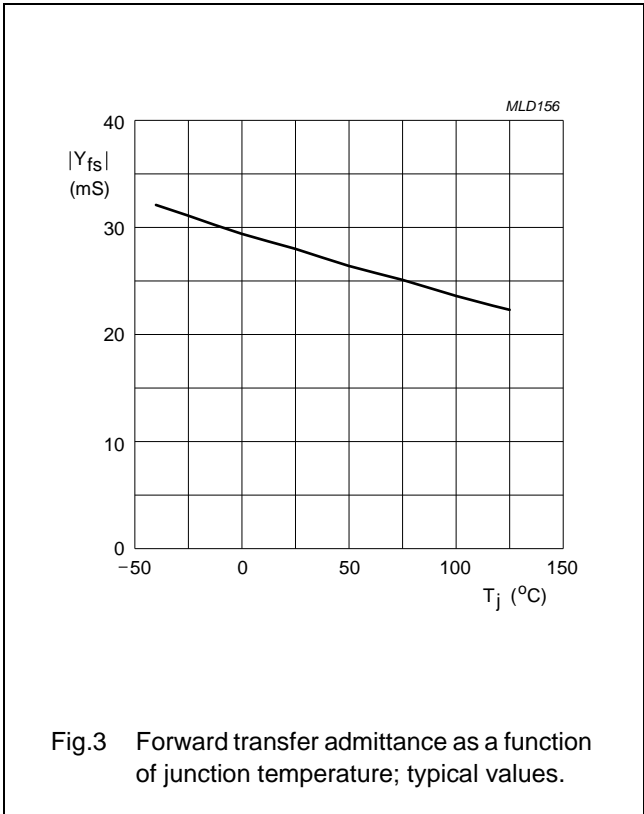
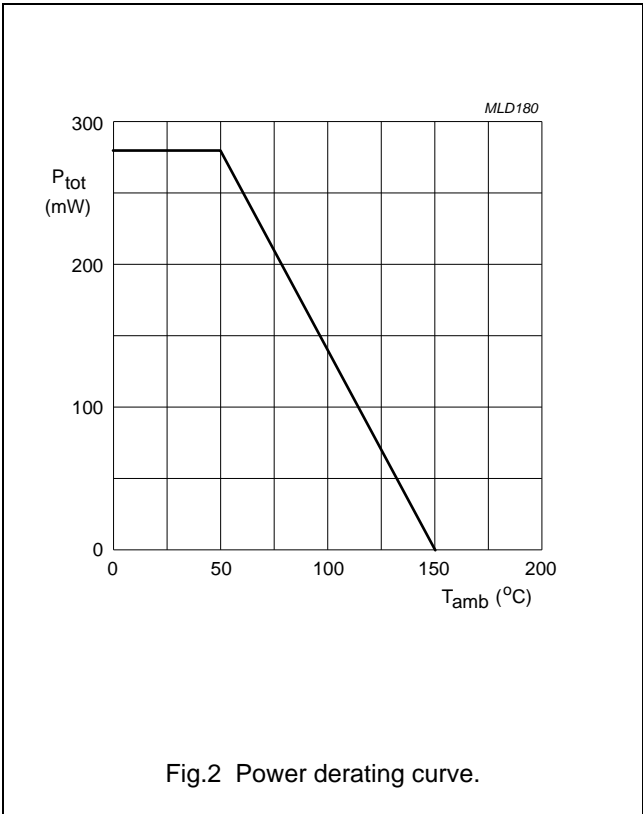
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	14	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	± 10	mA
I_{G2}	gate 2 current		–	± 10	mA
P_{tot}	total power dissipation	see Fig.2; up to $T_{amb} = 50\text{ }^{\circ}\text{C}$; note 1	–	280	mW
T_{stg}	storage temperature		–65	+150	$^{\circ}\text{C}$
T_j	operating junction temperature		–	+150	$^{\circ}\text{C}$

Note

- 1. Device mounted on a printed-circuit board.



Dual-gate MOS-FET

BF1100WR

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	350	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point	$T_s = 91\ ^\circ\text{C}$; note 2	210	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

 $T_j = 25\ ^\circ\text{C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 1\ \text{mA}$	13.2	20	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 1\ \text{mA}$	13.2	20	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10\ \text{mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10\ \text{mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\ \text{V}$; $V_{DS} = 9\ \text{V}$; $I_D = 20\ \mu\text{A}$	0.3	1	V
		$V_{G2-S} = 4\ \text{V}$; $V_{DS} = 12\ \text{V}$; $I_D = 20\ \mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = 4\ \text{V}$; $V_{DS} = 9\ \text{V}$; $I_D = 20\ \mu\text{A}$	0.3	1.2	V
		$V_{G1-S} = 4\ \text{V}$; $V_{DS} = 12\ \text{V}$; $I_D = 20\ \mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4\ \text{V}$; $V_{DS} = 9\ \text{V}$; $R_{G1} = 180\ \text{k}\Omega$; note 1	8	13	mA
		$V_{G2-S} = 4\ \text{V}$; $V_{DS} = 12\ \text{V}$; $R_{G1} = 250\ \text{k}\Omega$; note 2	8	13	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; $V_{G1-S} = 12\ \text{V}$	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 12\ \text{V}$	–	50	nA

Notes

1. R_{G1} connects gate 1 to $V_{GG} = 9\ \text{V}$; see Fig.26.
2. R_{G1} connects gate 1 to $V_{GG} = 12\ \text{V}$; see Fig.26.

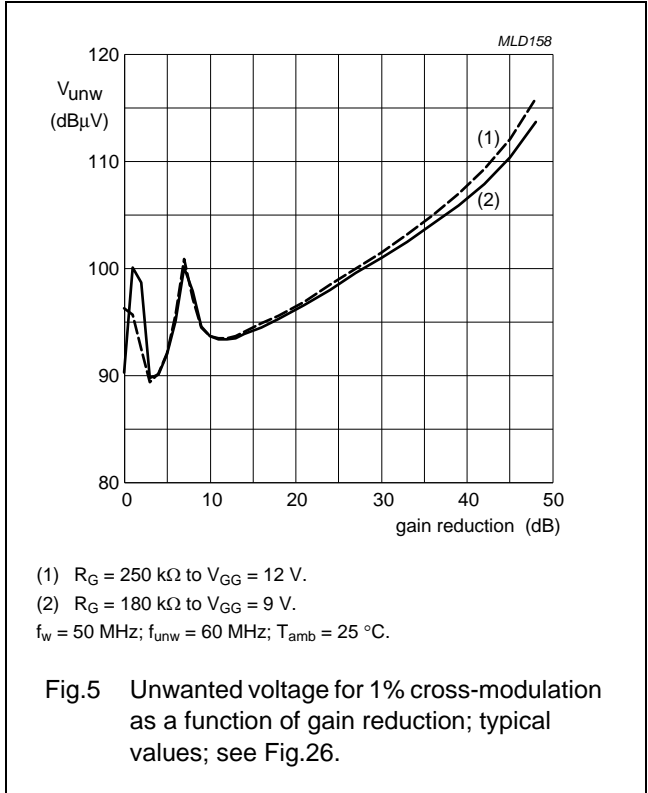
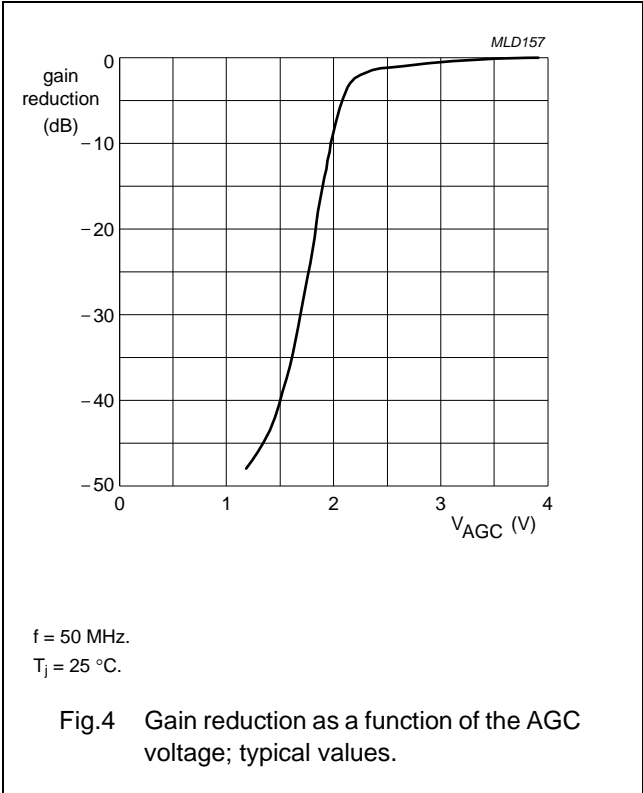
Dual-gate MOS-FET

BF1100WR

DYNAMIC CHARACTERISTICS

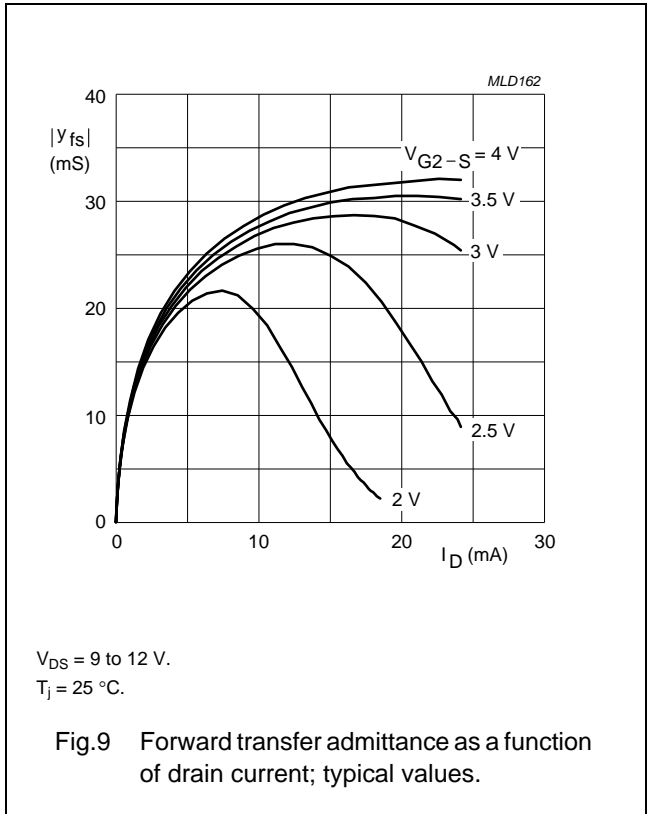
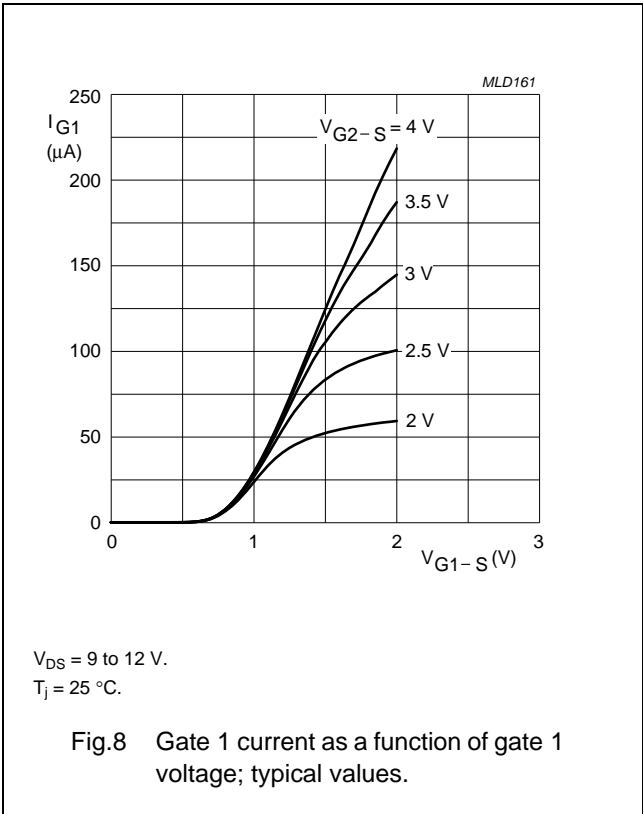
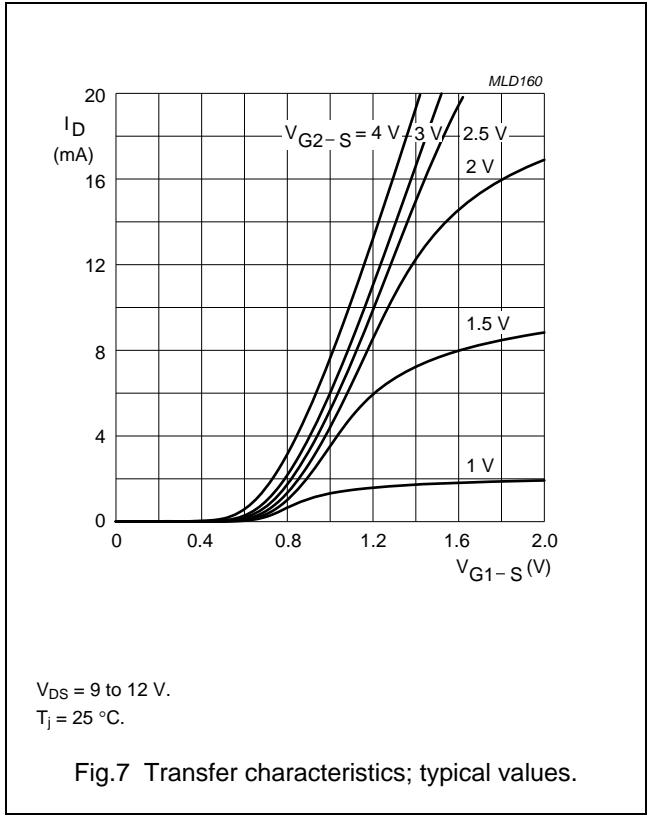
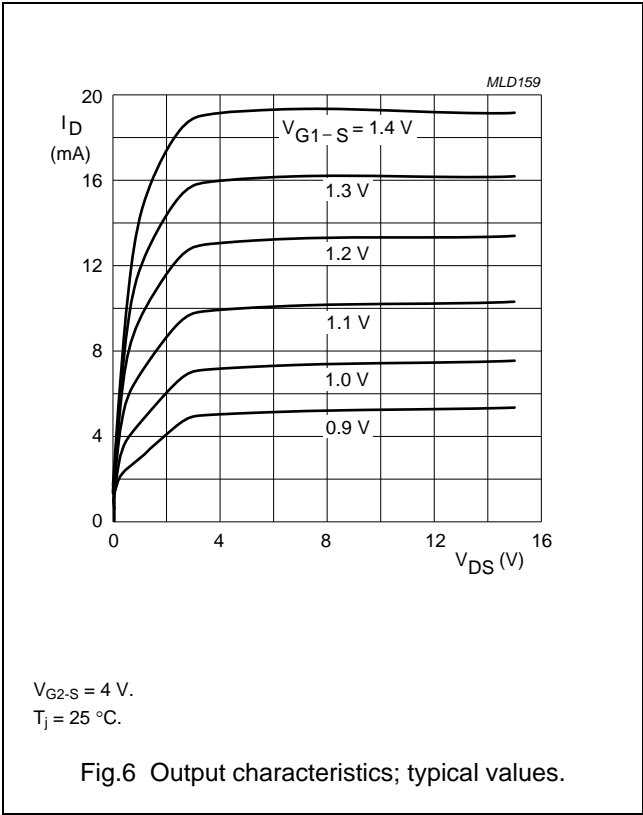
Common source; $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$; $V_{\text{G2-S}} = 4\text{ V}$; $I_{\text{D}} = 10\text{ mA}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{\text{fs}} $	forward transfer admittance	pulsed; $T_{\text{j}} = 25\text{ }^{\circ}\text{C}$ $V_{\text{DS}} = 9\text{ V}$ $V_{\text{DS}} = 12\text{ V}$	24 24	28 28	33 33	mS mS
$C_{\text{ig1-s}}$	input capacitance at gate 1	$f = 1\text{ MHz}$ $V_{\text{DS}} = 9\text{ V}$ $V_{\text{DS}} = 12\text{ V}$	— —	2.2 2.2	2.6 2.6	pF pF
$C_{\text{ig2-s}}$	input capacitance at gate 2	$f = 1\text{ MHz}$ $V_{\text{DS}} = 9\text{ V}$ $V_{\text{DS}} = 12\text{ V}$	— —	1.6 1.4	— —	pF pF
C_{OS}	drain-source capacitance	$f = 1\text{ MHz}$ $V_{\text{DS}} = 9\text{ V}$ $V_{\text{DS}} = 12\text{ V}$	— —	1.4 1.1	1.8 1.5	pF pF
C_{rs}	reverse transfer capacitance	$f = 1\text{ MHz}$ $V_{\text{DS}} = 9\text{ V}$ $V_{\text{DS}} = 12\text{ V}$	— —	25 25	35 35	fF fF
F	noise figure	$f = 800\text{ MHz}$; $G_{\text{S}} = G_{\text{Sopt}}$; $B_{\text{S}} = B_{\text{Sopt}}$ $V_{\text{DS}} = 9\text{ V}$ $V_{\text{DS}} = 12\text{ V}$	— —	2 2	2.8 2.8	dB dB



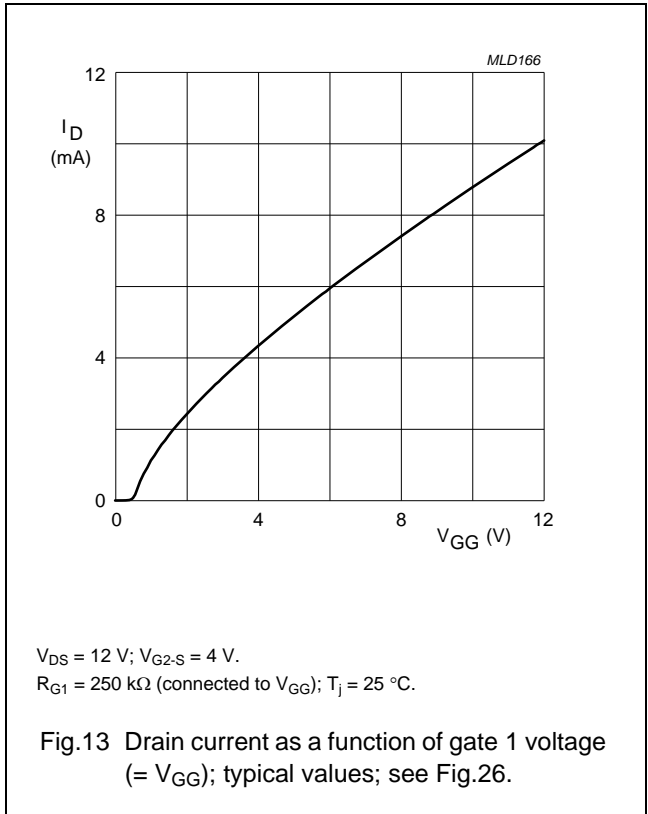
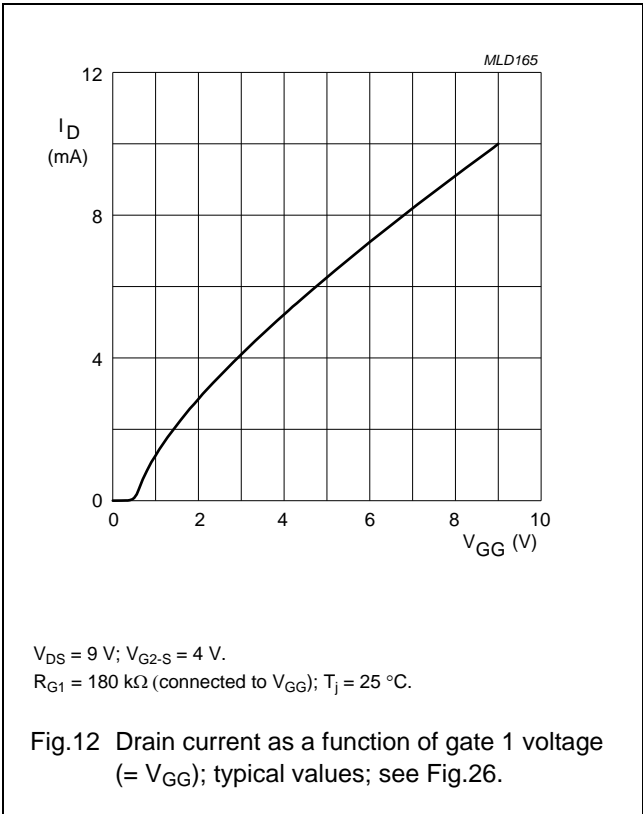
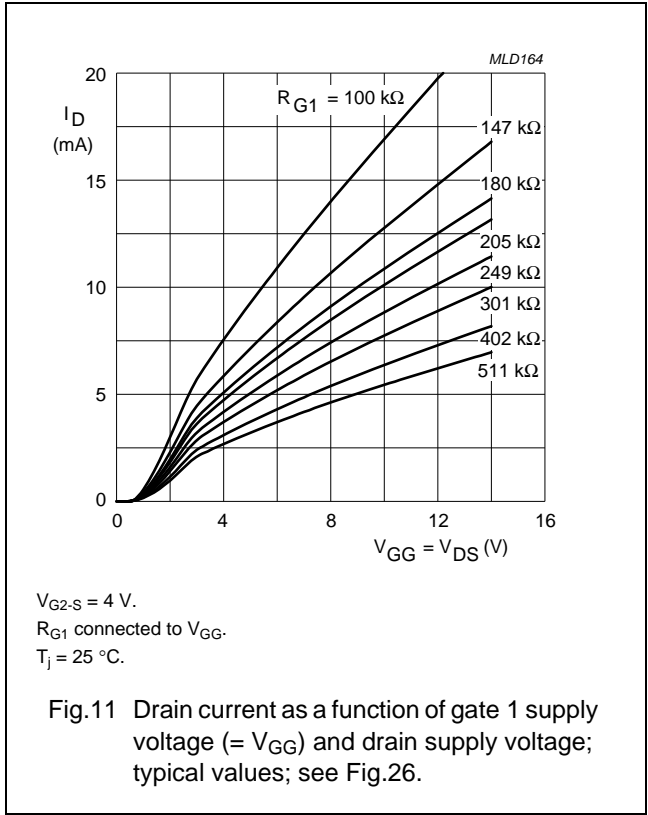
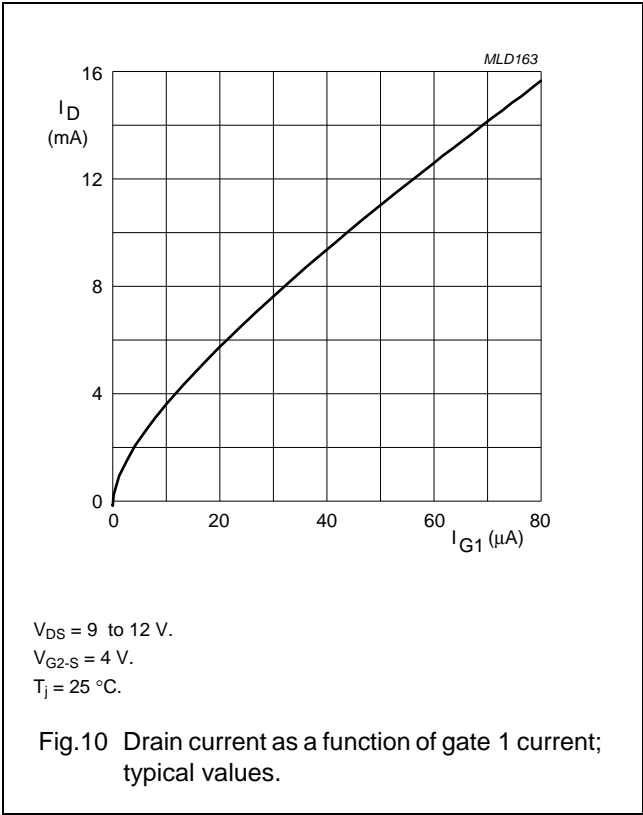
Dual-gate MOS-FET

BF1100WR



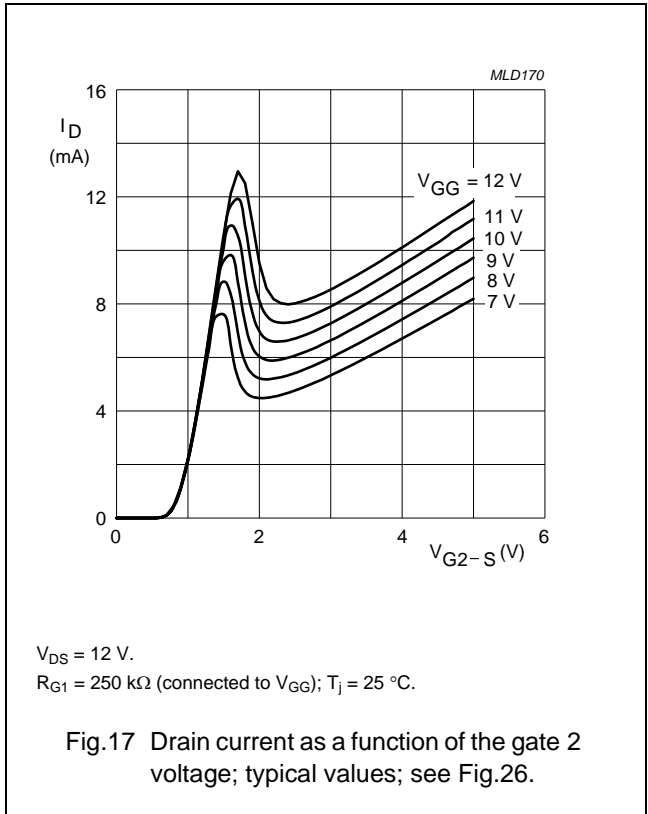
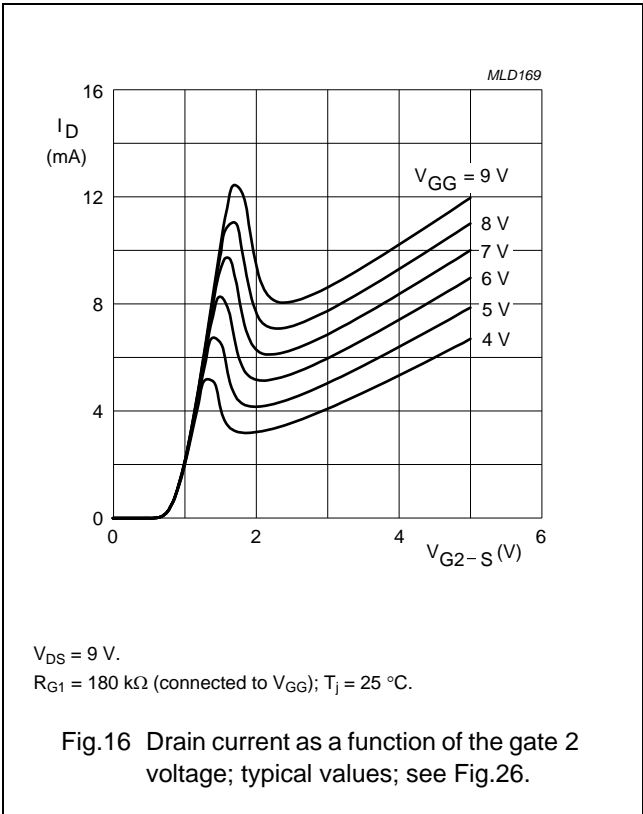
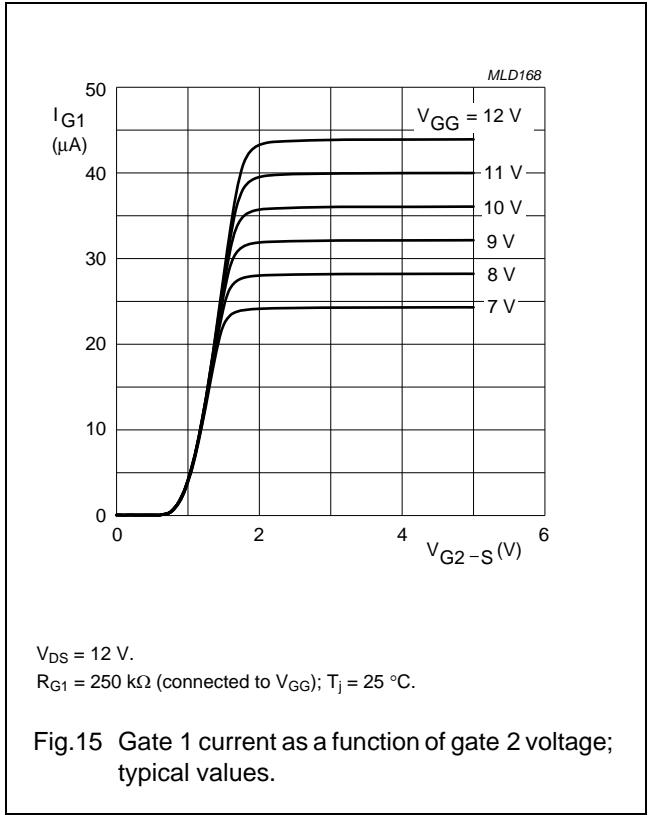
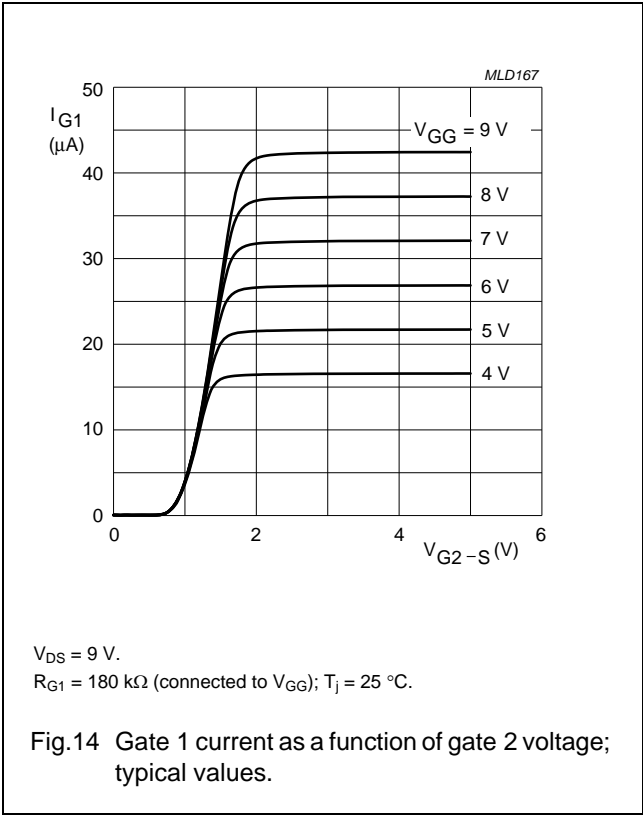
Dual-gate MOS-FET

BF1100WR



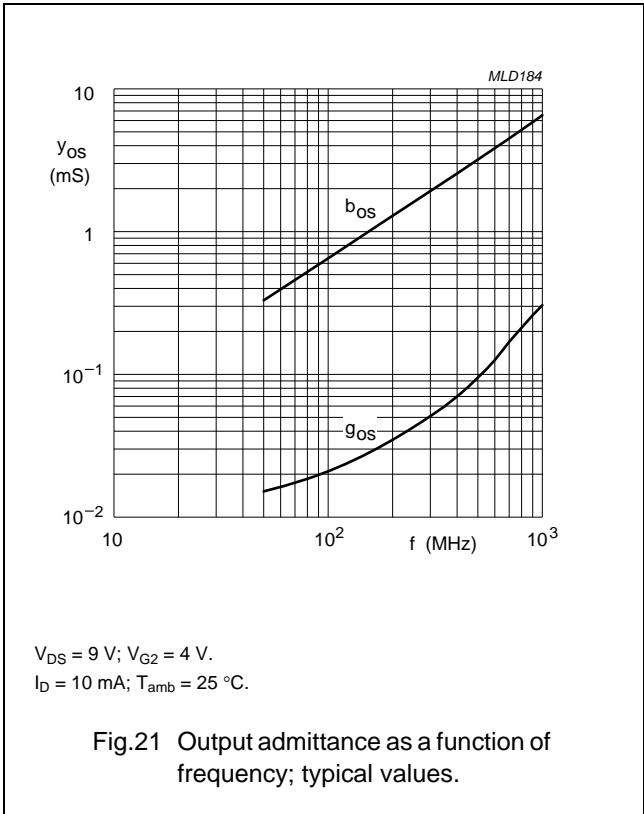
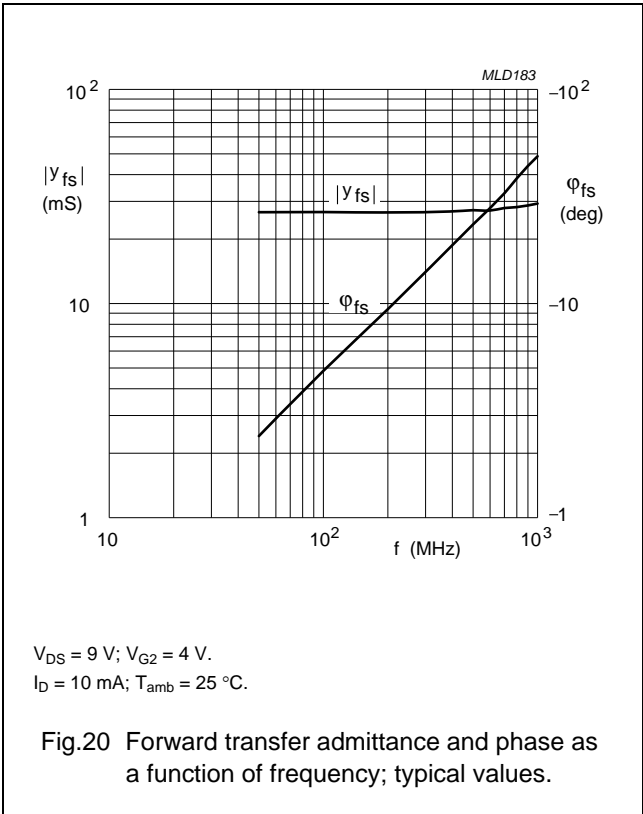
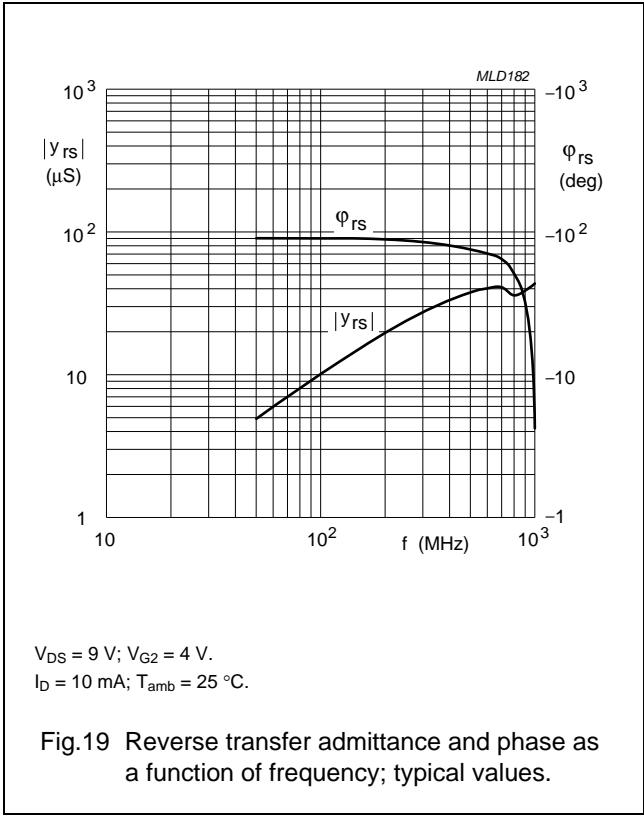
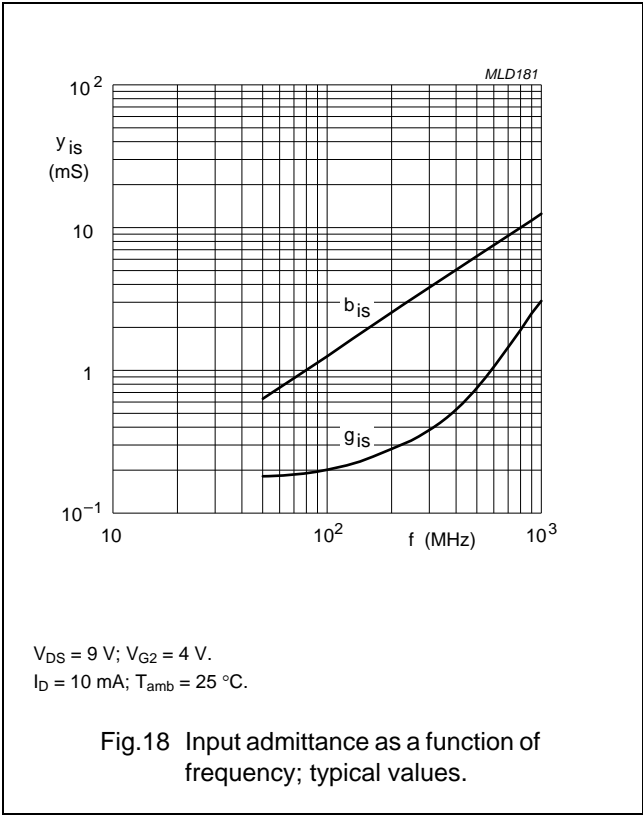
Dual-gate MOS-FET

BF1100WR



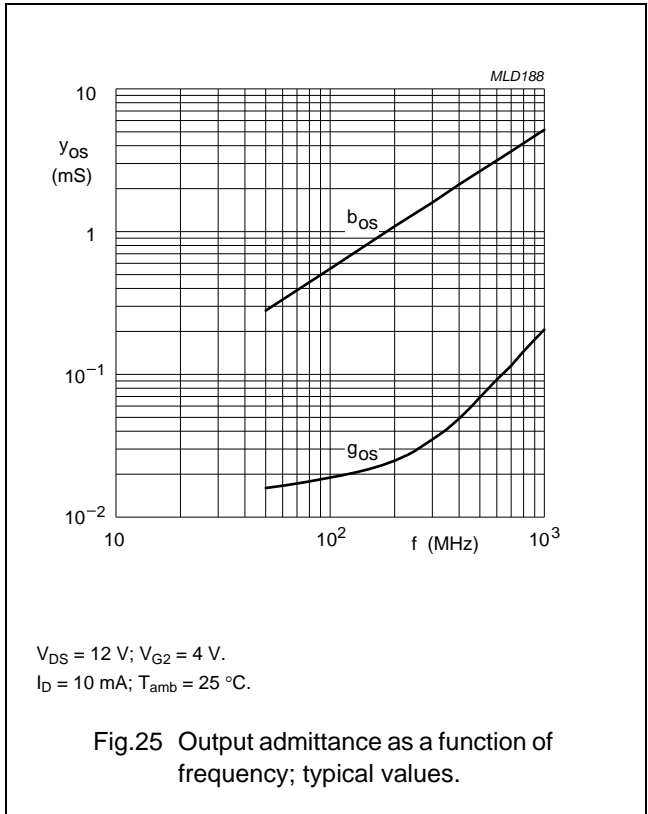
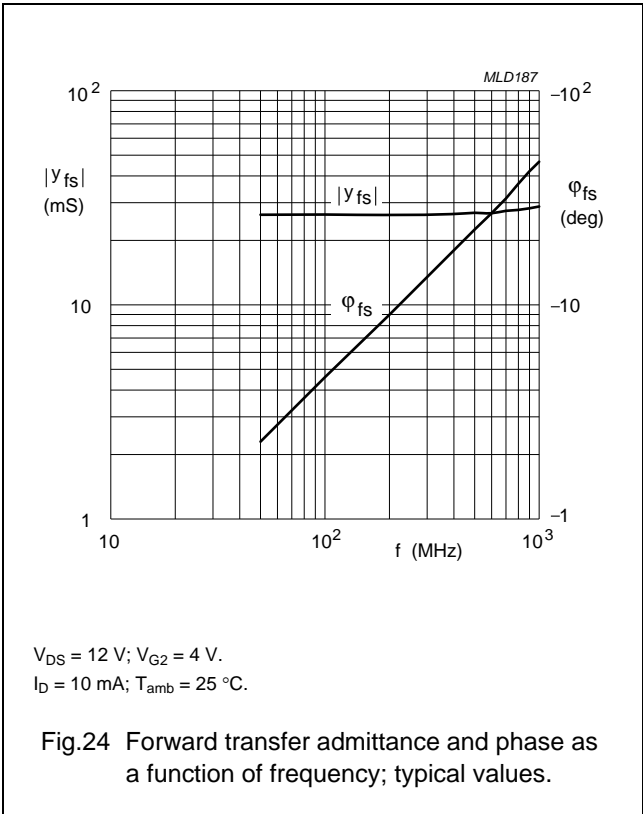
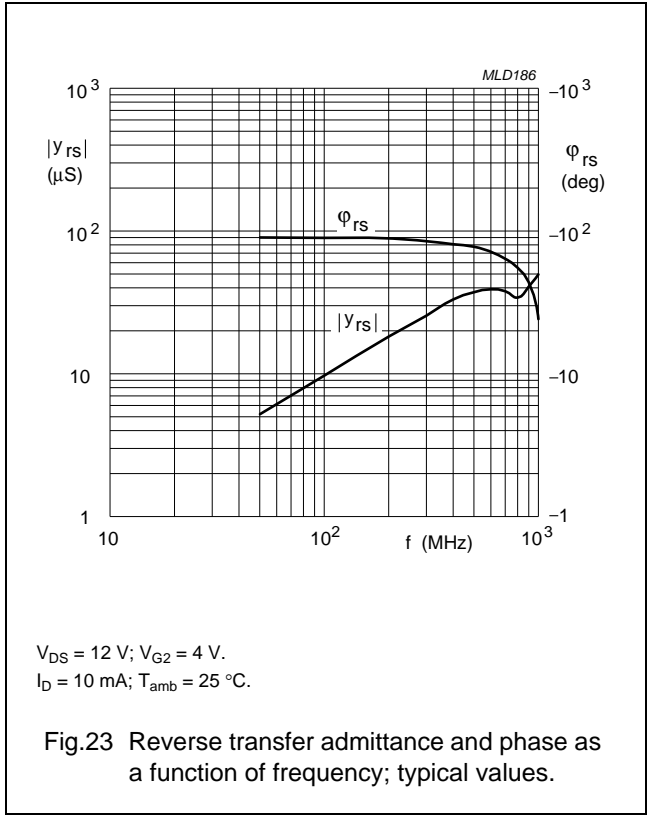
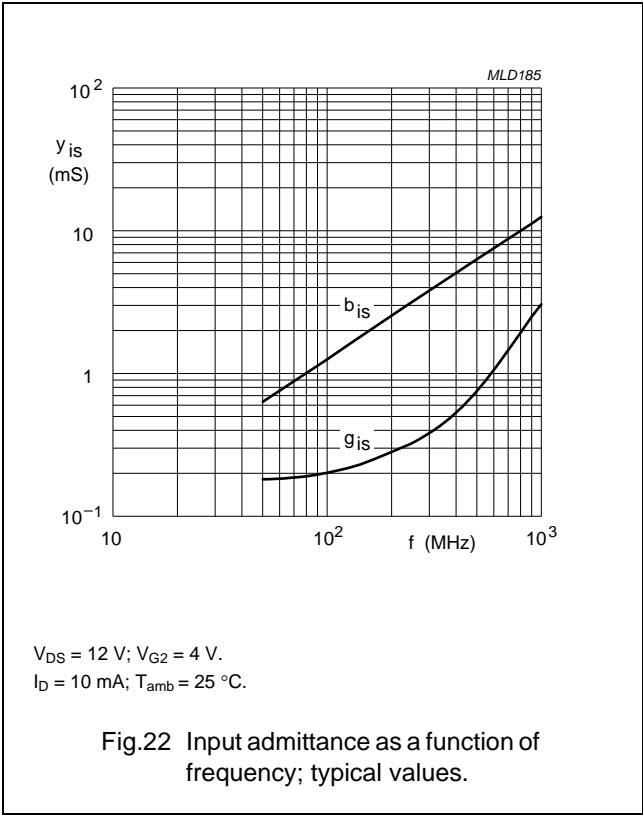
Dual-gate MOS-FET

BF1100WR



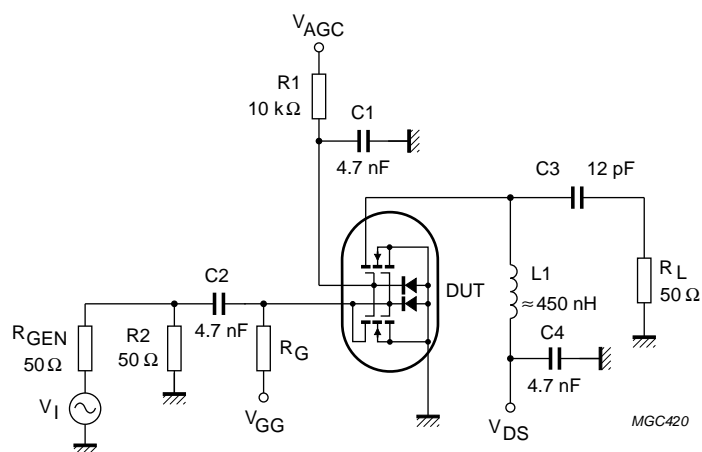
Dual-gate MOS-FET

BF1100WR



Dual-gate MOS-FET

BF1100WR



For $V_{GG} = V_{DS} = 9$ V, $R_G = 180$ k Ω .
 For $V_{GG} = V_{DS} = 12$ V, $R_G = 250$ k Ω .

Fig.26 Cross-modulation test circuit.

Dual-gate MOS-FET

BF1100WR

Table 1 Scattering parameters: $V_{DS} = 9\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 10\text{ mA}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	-3.9	2.618	175.1	0.001	137.9	1.000	-1.9
100	0.981	-7.3	2.602	170.5	0.001	80.4	0.999	-4.0
200	0.975	-14.4	2.577	160.7	0.002	74.0	0.995	-7.6
300	0.965	-21.6	2.555	151.6	0.002	79.3	0.994	-11.3
400	0.947	-28.3	2.513	141.8	0.003	80.5	0.992	-15.0
500	0.927	-34.9	2.449	133.4	0.003	82.8	0.988	-18.5
600	0.913	-41.7	2.339	124.6	0.003	78.9	0.984	-22.0
700	0.890	-47.9	2.361	115.4	0.003	80.6	0.982	-25.3
800	0.869	-54.0	2.302	106.4	0.003	93.9	0.979	-28.8
900	0.845	-59.7	2.228	97.6	0.003	104.8	0.976	-32.1
1000	0.823	-65.4	2.167	89.6	0.003	129.3	0.974	-35.5

Table 2 Noise data: $V_{DS} = 9\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 10\text{ mA}$

f (MHz)	F _{min} (dB)	Γ _{opt}		r _n
		(ratio)	(deg)	
800	2.00	0.67	43.9	0.89

Table 3 Scattering parameters: $V_{DS} = 12\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 10\text{ mA}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	-3.7	2.576	175.3	0.000	125.0	1.000	-1.6
100	0.980	-7.4	2.563	170.9	0.001	111.2	1.000	-3.3
200	0.973	-14.6	2.541	161.6	0.002	83.0	0.997	-6.4
300	0.962	-21.5	2.519	152.9	0.002	85.2	0.996	-9.3
400	0.946	-28.5	2.479	143.5	0.003	79.4	0.995	-12.4
500	0.929	-35.0	2.419	135.5	0.003	78.2	0.991	-15.3
600	0.912	-41.6	2.373	127.2	0.003	80.0	0.989	-18.1
700	0.895	-47.8	2.336	118.7	0.003	83.4	0.987	-20.9
800	0.868	-53.8	2.284	110.0	0.003	91.3	0.985	-23.7
900	0.845	-59.8	2.213	101.6	0.003	95.9	0.983	-26.5
1000	0.823	-65.7	2.160	94.1	0.003	112.2	0.981	-29.3

Table 4 Noise data: $V_{DS} = 12\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 10\text{ mA}$

f (MHz)	F _{min} (dB)	Γ _{opt}		r _n
		(ratio)	(deg)	
800	2.00	0.66	43.3	0.97

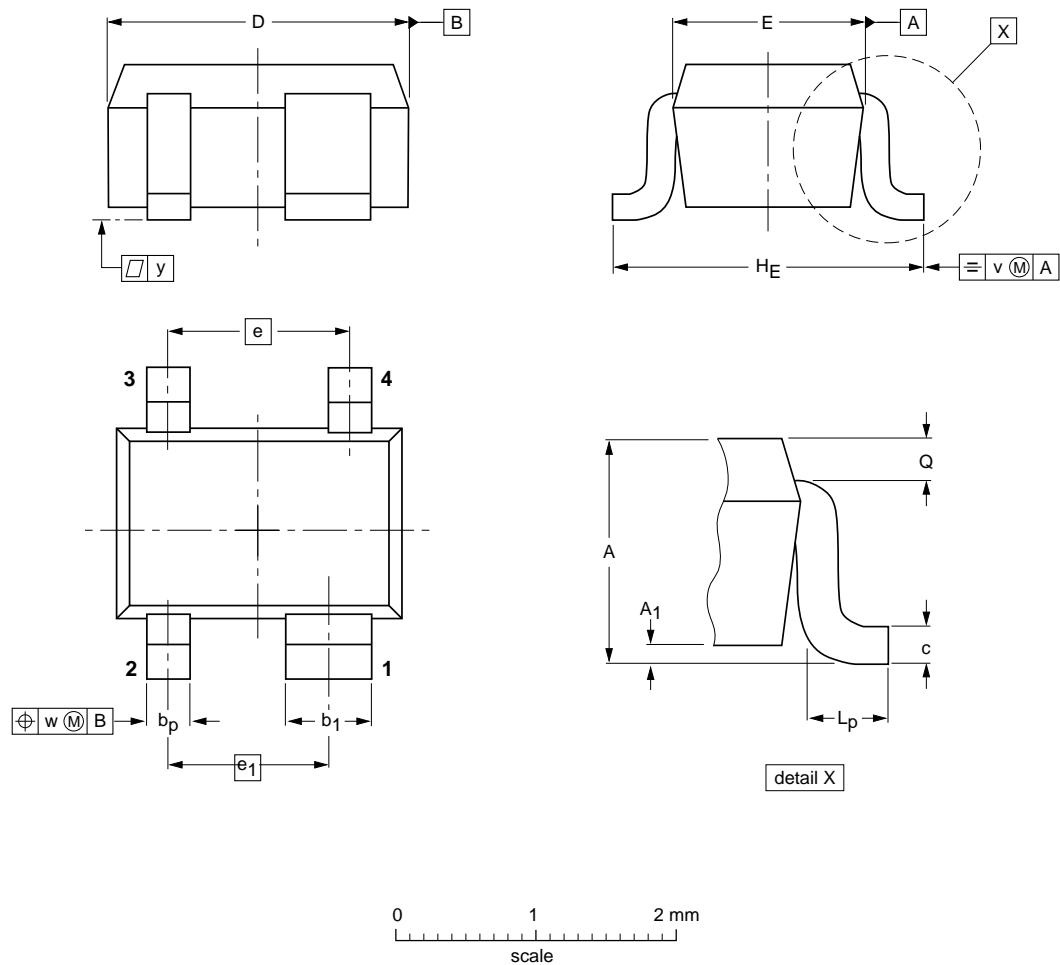
Dual-gate MOS-FET

BF1100WR

PACKAGE OUTLINE


Plastic surface-mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21 06-03-16

Dual-gate MOS-FET

BF1100WR

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

DEFINITIONS

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

DISCLAIMERS

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Dual-gate MOS-FETBF1100WR

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

NXP Semiconductors

provides High Performance Mixed Signal and Standard Product solutions that leverage its leading RF, Analog, Power Management, Interface, Security and Digital Processing expertise

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: <http://www.nxp.com>

For sales offices addresses send e-mail to: salesaddresses@nxp.com

© NXP B.V. 2010

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

R77/01/pp16

Date of release: 1995 Apr 25