

# DATA SHEET

## **BF1101; BF1101R; BF1101WR** N-channel dual-gate MOS-FETs

Product specification  
Supersedes data of 1999 Feb 01

1999 May 14



# N-channel dual-gate MOS-FETs

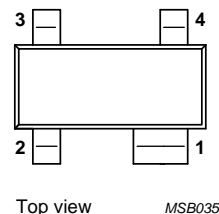
## BF1101; BF1101R; BF1101WR

### FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

### PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



BF1101R marking code: NCp.

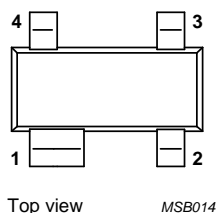
Fig.2 Simplified outline (SOT143R).

### APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage, such as television tuners and professional communications equipment.

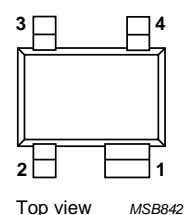
### DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1101, BF1101R and BF1101WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.



BF1101 marking code: NDp.

Fig.1 Simplified outline (SOT143B).



BF1101WR marking code: NC.

Fig.3 Simplified outline (SOT343R).

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	–	7	V
$I_D$	drain current		–	–	30	mA
$P_{tot}$	total power dissipation		–	–	200	mW
$ y_{fs} $	forward transfer admittance		25	30	–	mS
$C_{ig1-ss}$	input capacitance at gate 1		–	2.2	2.7	pF
$C_{rss}$	reverse transfer capacitance	$f = 1 \text{ MHz}$	–	25	35	fF
$F$	noise figure	$f = 800 \text{ MHz}$	–	1.7	2.5	dB
$X_{mod}$	cross-modulation	input level for $k = 1\%$ at 40 dB AGC	100	–	–	dB $\mu$ V
$T_j$	operating junction temperature		–	–	150	°C

### CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

## N-channel dual-gate MOS-FETs

BF1101; BF1101R; BF1101WR

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

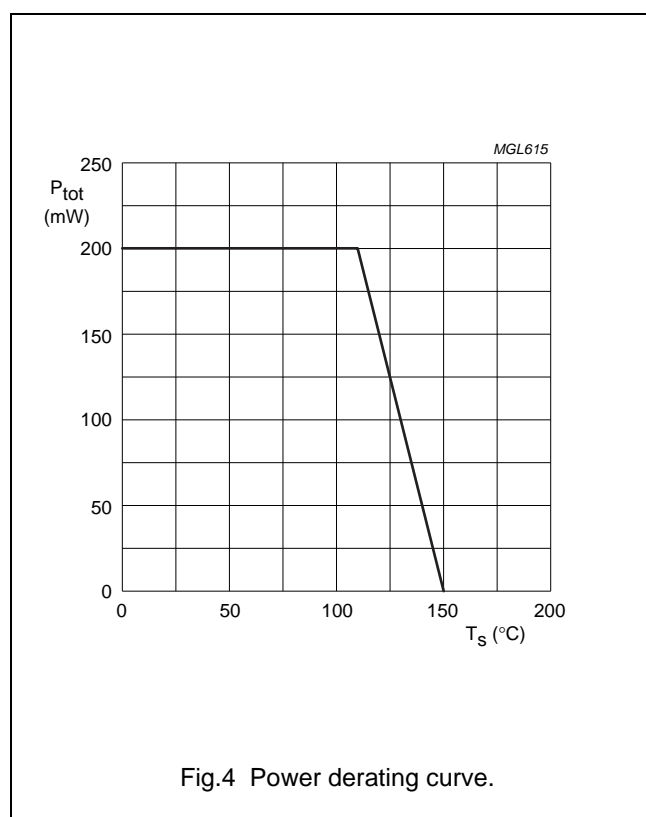
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage		–	7	V
$I_D$	drain current		–	30	mA
$I_{G1}$	gate 1 current		–	$\pm 10$	mA
$I_{G2}$	gate 2 current		–	$\pm 10$	mA
$P_{tot}$	total power dissipation	$T_s \leq 110\text{ }^{\circ}\text{C}$ ; note 1	–	200	mW
$T_{stg}$	storage temperature		–65	+150	$^{\circ}\text{C}$
$T_j$	operating junction temperature		–	+150	$^{\circ}\text{C}$

## Note

1.  $T_s$  is the temperature of the soldering point of the source lead.

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	200	K/W



## N-channel dual-gate MOS-FETs

## BF1101; BF1101R; BF1101WR

## STATIC CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$ ; $I_D = 10\text{ }\mu\text{A}$	7	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$ ; $I_{G1-S} = 10\text{ mA}$	7	16	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$ ; $I_{G2-S} = 10\text{ mA}$	7	16	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$ ; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$ ; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\text{ V}$ ; $V_{DS} = 5\text{ V}$ ; $I_D = 100\text{ }\mu\text{A}$	0.3	1.0	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = 5\text{ V}$ ; $V_{DS} = 5\text{ V}$ ; $I_D = 100\text{ }\mu\text{A}$	0.3	1.2	V
$I_{DSX}$	drain-source current	$V_{G2-S} = 4\text{ V}$ ; $V_{DS} = 5\text{ V}$ ; $R_{G1} = 120\text{ k}\Omega$ ; note 1	8	16	mA
$I_{G1-SS}$	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$ ; $V_{G1-S} = 5\text{ V}$	–	50	nA
$I_{G2-SS}$	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$ ; $V_{G2-S} = 4\text{ V}$	–	20	nA

## Note

1.  $R_{G1}$  connects  $G_1$  to  $V_{GG} = 5\text{ V}$ ; see Fig.21.

## DYNAMIC CHARACTERISTICS

Common source;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $V_{DS} = 5\text{ V}$ ;  $I_D = 12\text{ mA}$ ; unless otherwise specified.

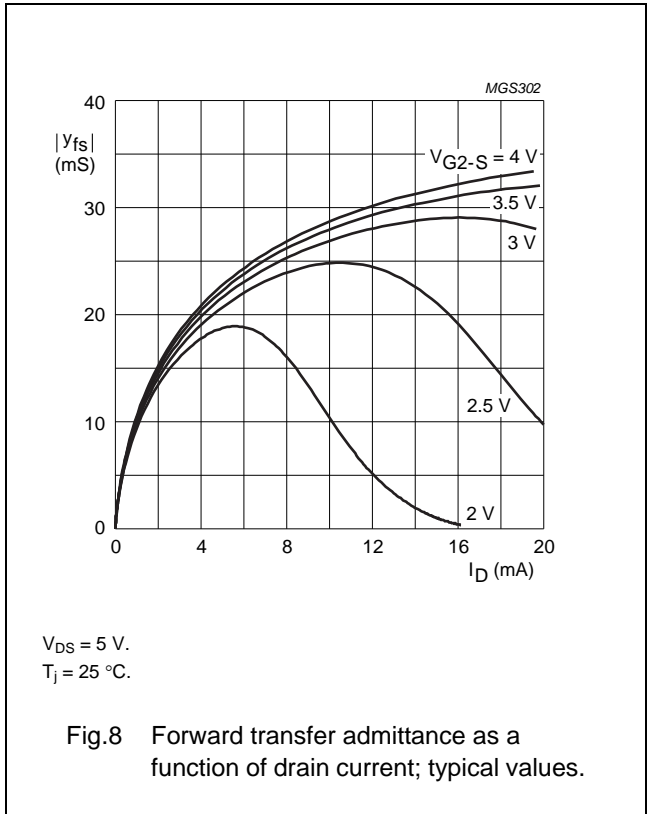
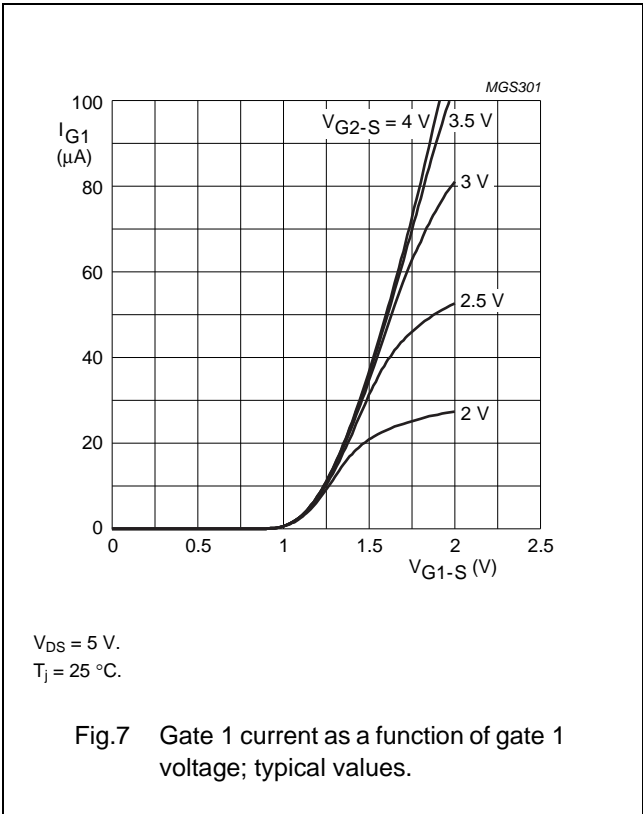
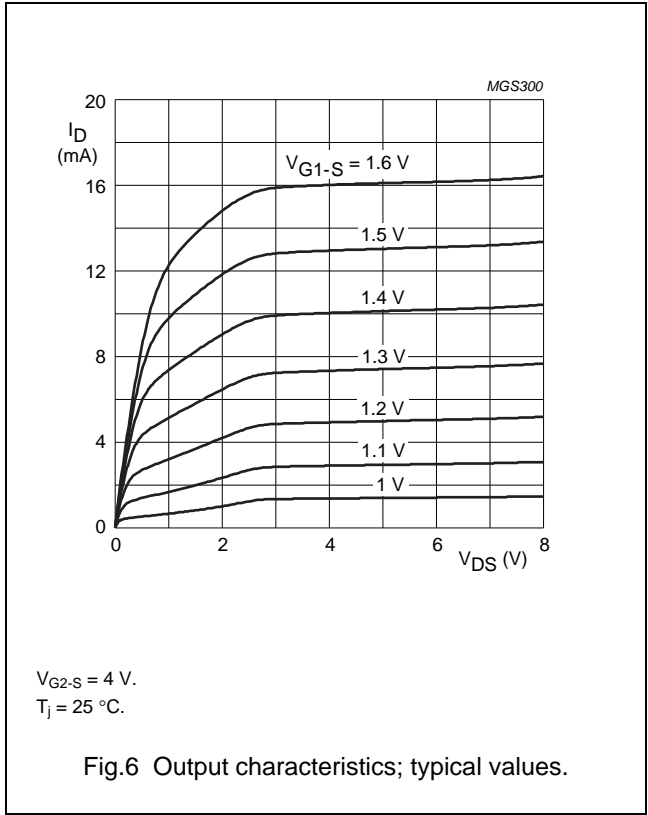
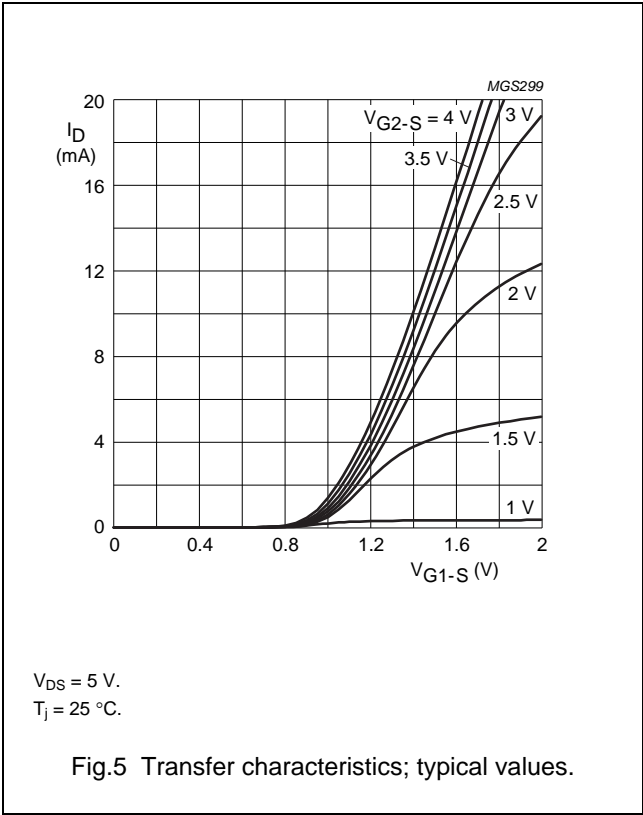
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ }^{\circ}\text{C}$	25	30	40	mS
$C_{ig1-ss}$	input capacitance at gate 1	$f = 1\text{ MHz}$	–	2.2	2.7	pF
$C_{ig2-ss}$	input capacitance at gate 2	$f = 1\text{ MHz}$	–	1.6	–	pF
$C_{oss}$	output capacitance	$f = 1\text{ MHz}$	–	1.2	–	pF
$C_{rss}$	reverse transfer capacitance	$f = 1\text{ MHz}$	–	25	35	fF
F	noise figure	$f = 800\text{ MHz}$ ; $Y_S = Y_{S\text{ opt}}$	–	1.7	2.5	dB
$X_{mod}$	cross-modulation	input level for $k = 1\%$ at 0 dB AGC; $f_w = 50\text{ MHz}$ ; $f_{unw} = 60\text{ MHz}$ ; note 1	85	–	–	dB $\mu\text{V}$
		input level for $k = 1\%$ at 40 dB AGC; $f_w = 50\text{ MHz}$ ; $f_{unw} = 60\text{ MHz}$ ; note 1	100	–	–	dB $\mu\text{V}$

## Note

1. Measured in test circuit of Fig.21.

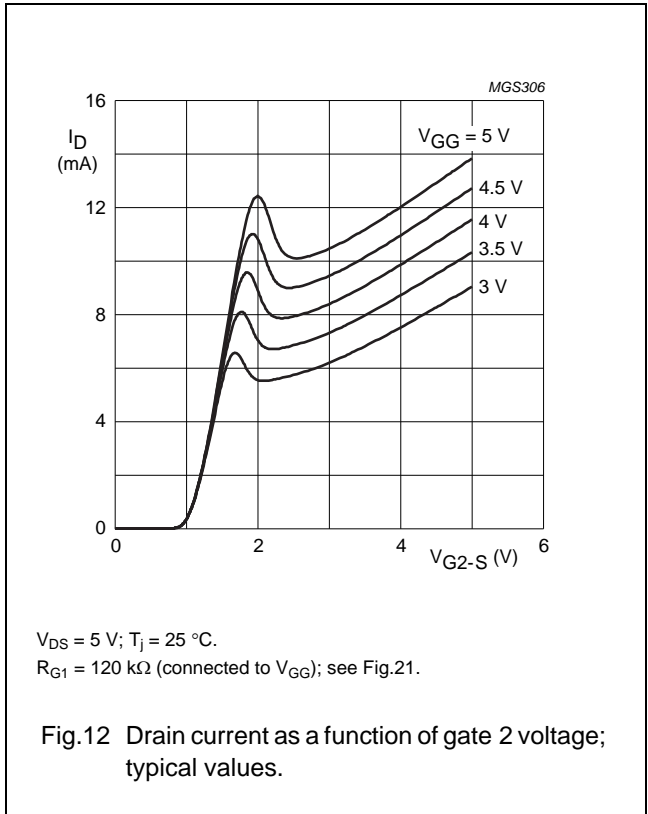
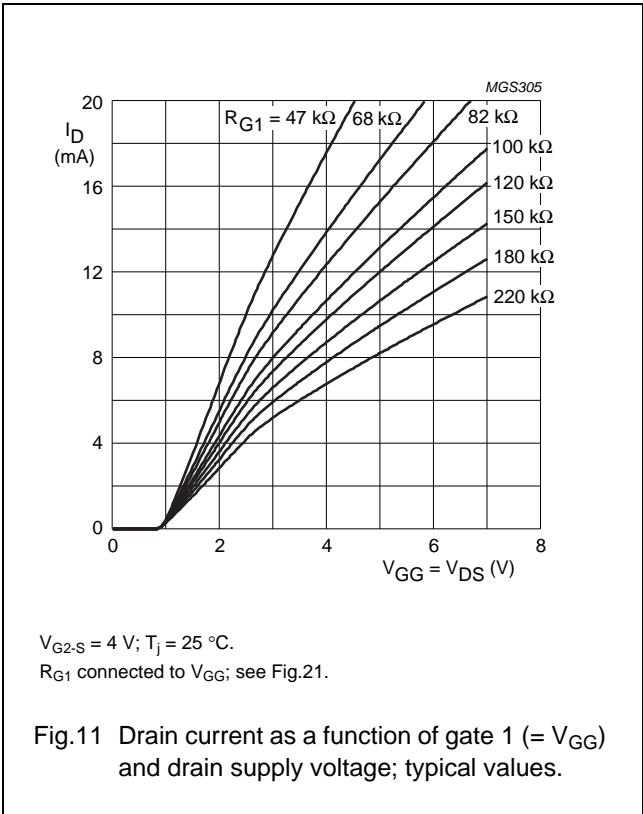
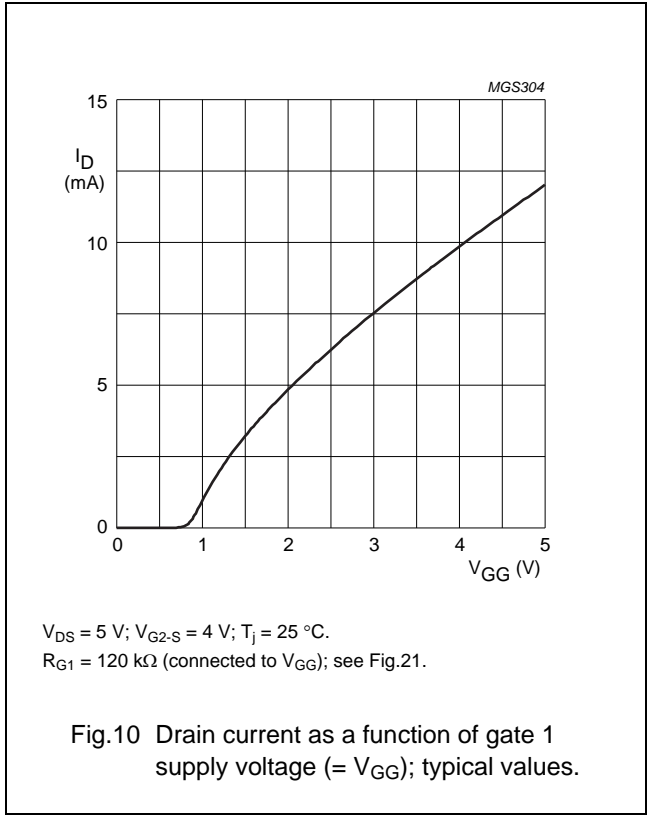
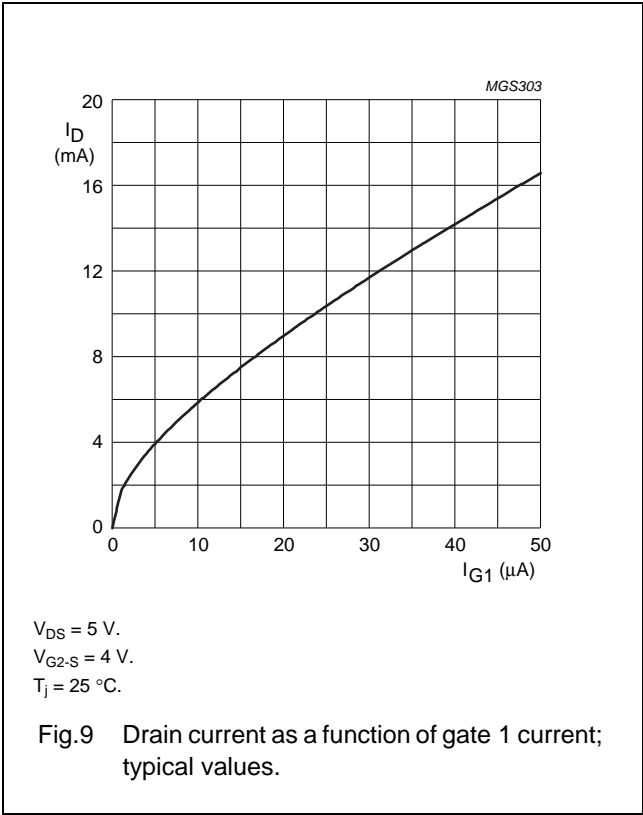
N-channel dual-gate MOS-FETs

BF1101; BF1101R; BF1101WR



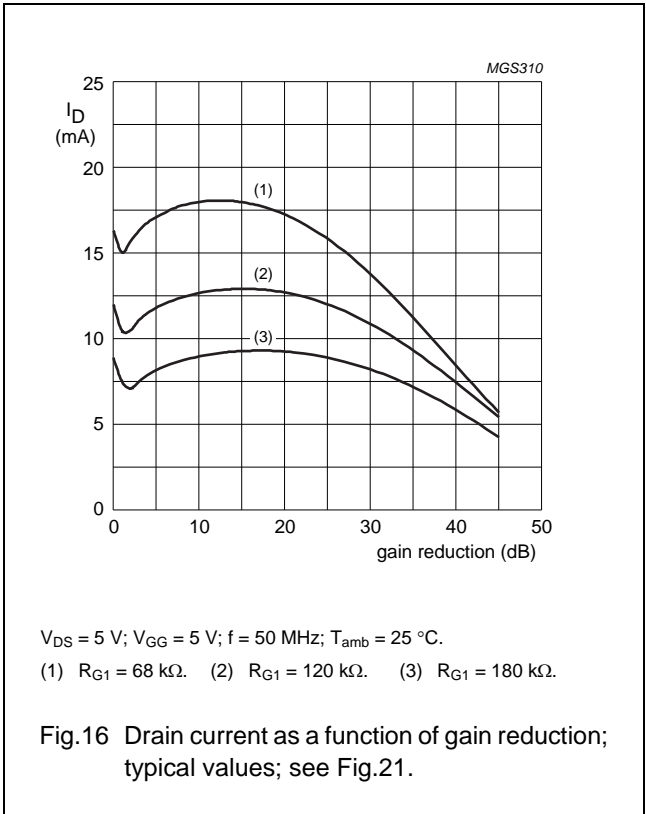
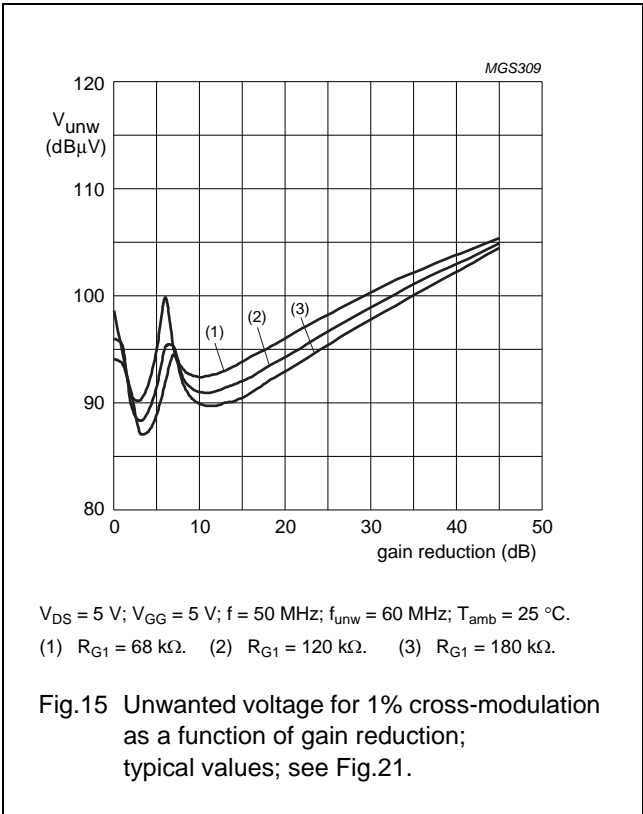
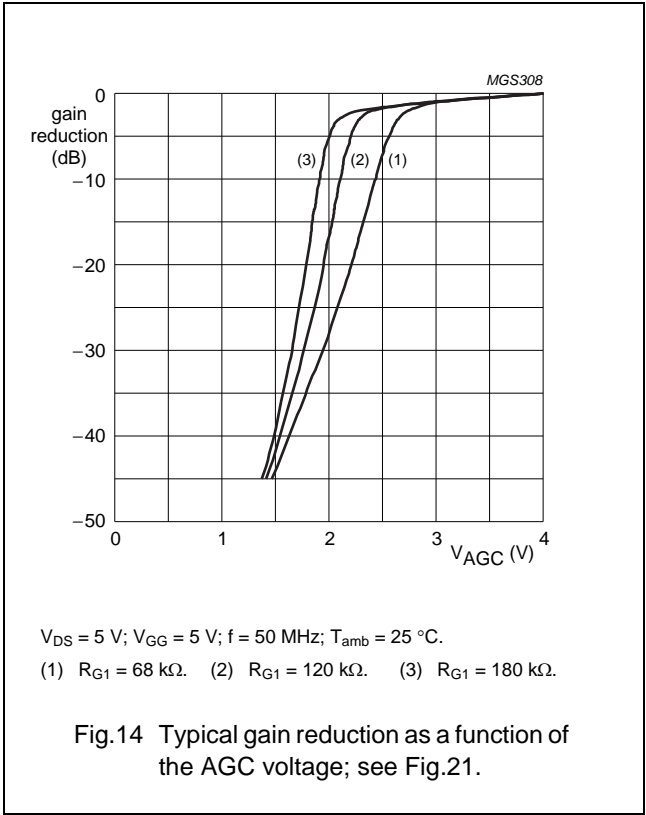
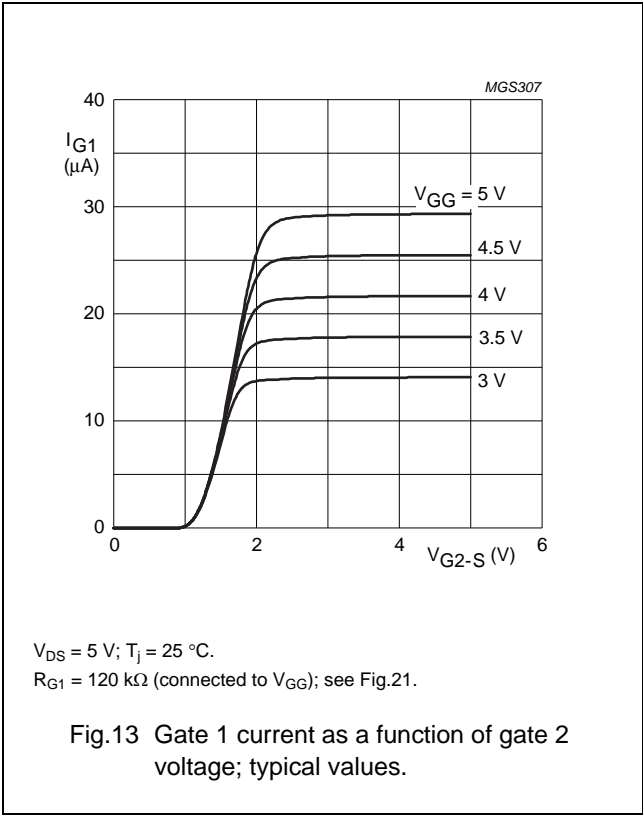
N-channel dual-gate MOS-FETs

BF1101; BF1101R; BF1101WR



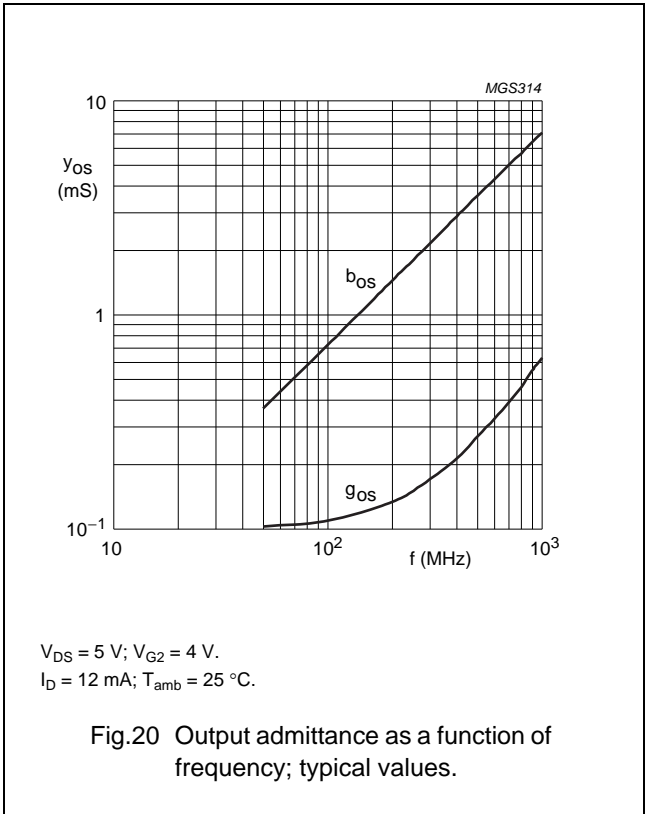
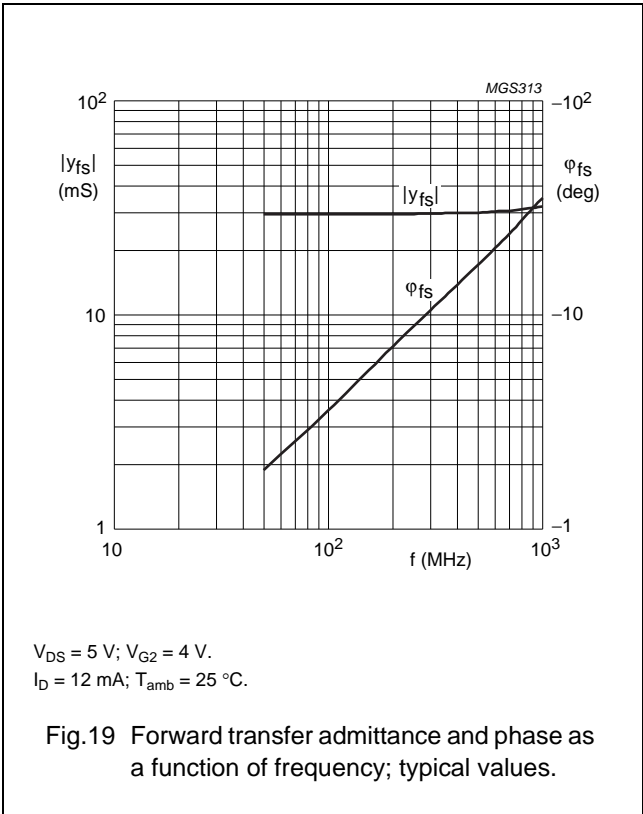
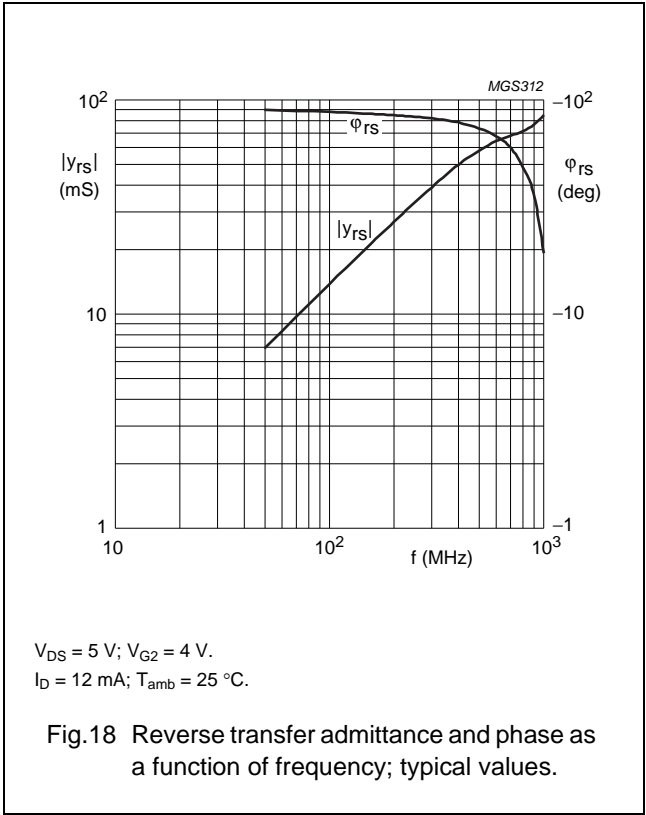
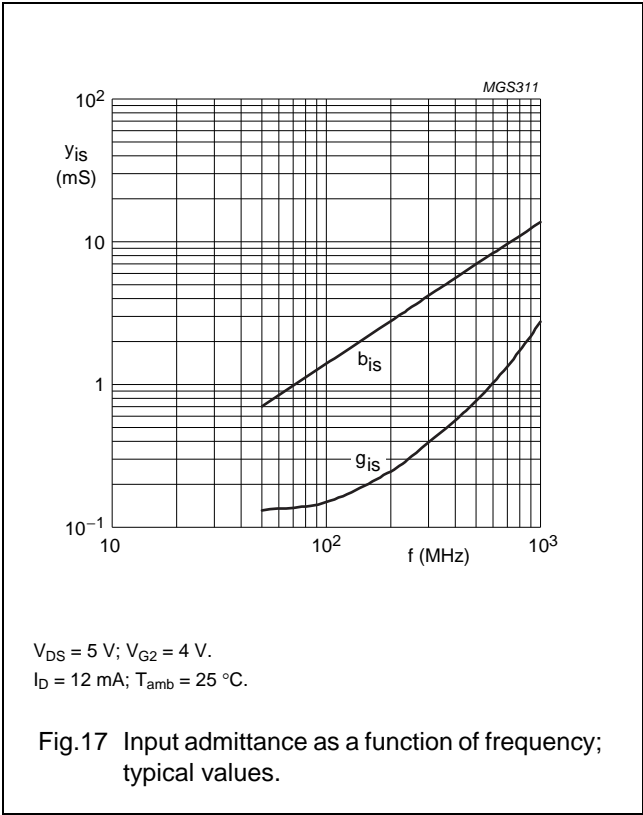
N-channel dual-gate MOS-FETs

BF1101; BF1101R; BF1101WR



N-channel dual-gate MOS-FETs

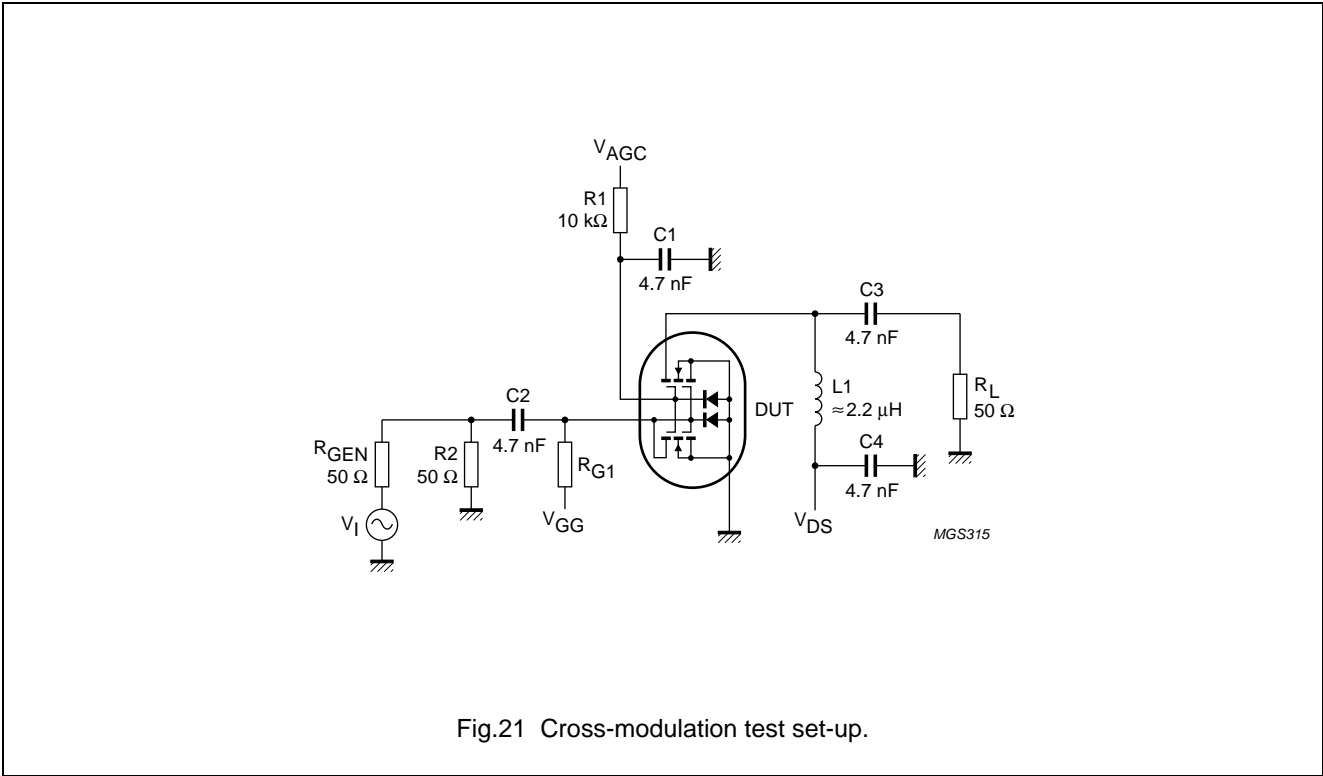
BF1101; BF1101R; BF1101WR





N-channel dual-gate MOS-FETs

BF1101; BF1101R; BF1101WR



**Table 1** Scattering parameters:  $V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 12\text{ mA}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$

f (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.987	−4.1	2.922	175.0	0.001	87.6	0.990	−2.2
100	0.985	−8.1	2.908	170.3	0.001	86.1	0.989	−4.3
200	0.976	−16.1	2.875	160.8	0.003	83.3	0.985	−8.5
300	0.963	−23.9	2.820	157.6	0.004	80.4	0.982	−12.6
400	0.949	−31.6	2.762	142.6	0.005	78.2	0.977	−16.8
500	0.933	−38.8	2.665	134.1	0.005	77.8	0.972	−20.8
600	0.916	−45.7	2.591	125.7	0.005	78.9	0.967	−24.7
700	0.897	−52.2	2.498	117.7	0.006	81.8	0.961	−28.5
800	0.877	−58.4	2.410	109.6	0.005	89.1	0.957	−32.2
900	0.856	−64.5	2.318	101.6	0.006	97.1	0.950	−35.8
1000	0.832	−70.3	2.214	94.2	0.006	110.4	0.946	−39.6

**Table 2** Noise data:  $V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 12\text{ mA}$ ;  $T_{amb} = 25\text{ }^{\circ}\text{C}$

f (MHz)	F <sub>min</sub> (dB)	Γ <sub>opt</sub>		R <sub>n</sub> (Ω)
		(ratio)	(deg)	
800	1.5	0.715	58.3	37.85

N-channel dual-gate MOS-FETs

BF1101; BF1101R; BF1101WR

PACKAGE OUTLINES

Plastic surface-mounted package; 4 leads

SOT143B

Technical drawing of the SOT143B package showing top, side, and lead detail views with dimensions A, A1, b<sub>p</sub>, b<sub>1</sub>, c, D, E, e, e<sub>1</sub>, H<sub>E</sub>, L<sub>p</sub>, Q, v, w, y.

0 1 2 mm  
scale

**DIMENSIONS (mm are the original dimensions)**

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

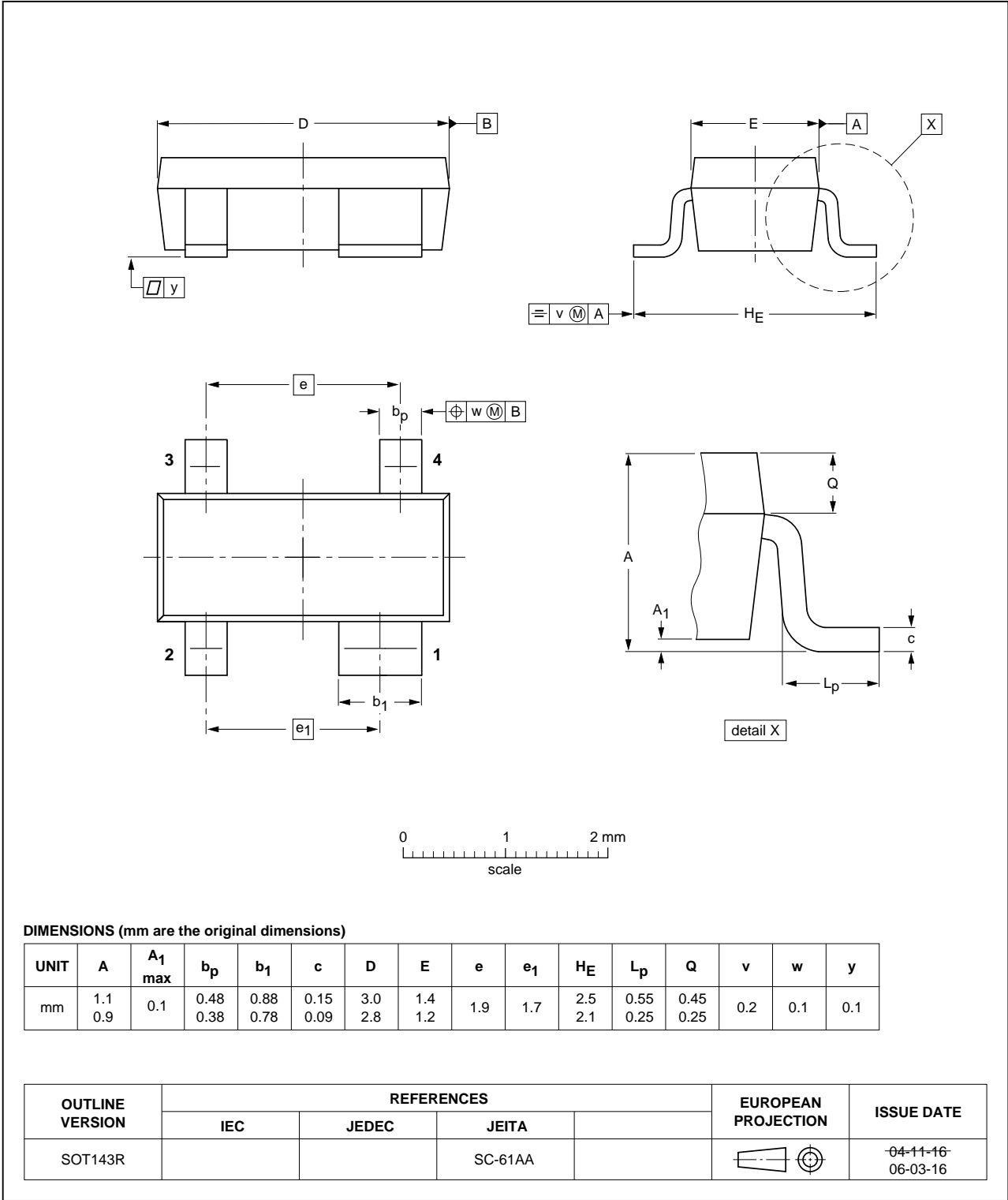
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143B						04-11-16 06-03-16

N-channel dual-gate MOS-FETs

BF1101; BF1101R; BF1101WR

Plastic surface-mounted package; reverse pinning; 4 leads

SOT143R

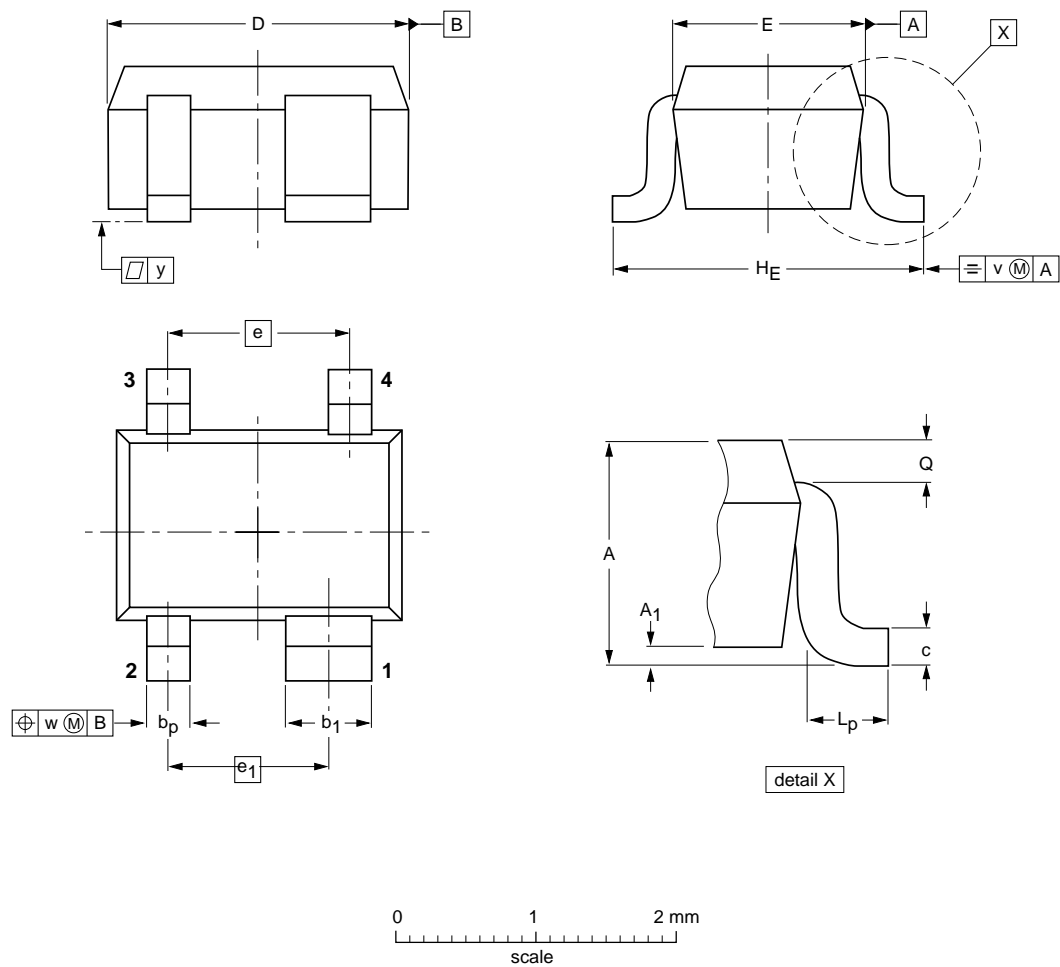


N-channel dual-gate MOS-FETs

BF1101; BF1101R; BF1101WR

Plastic surface-mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21 06-03-16

## N-channel dual-gate MOS-FETs

## BF1101; BF1101R; BF1101WR

## DATA SHEET STATUS

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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## N-channel dual-gate MOS-FETs

## BF1101; BF1101R; BF1101WR

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## **Customer notification**

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

## **Contact information**

For additional information please visit: <http://www.nxp.com>

For sales offices addresses send e-mail to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

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Printed in The Netherlands

R77/02/pp15

Date of release: 1999 May 14