

DATA SHEET

BF1211; BF1211R; BF1211WR N-channel dual-gate MOS-FETs

Product specification

2003 Dec 16



N-channel dual-gate MOS-FETs

BF1211; BF1211R; BF1211WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier
- Excellent low frequency noise performance
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

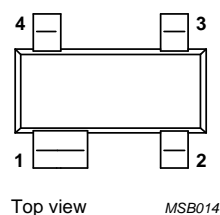
- Gain controlled low noise VHF and UHF amplifiers for 5 V digital and analog television tuner applications.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1211, BF1211R and BF1211WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

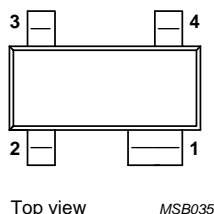
PINNING

| PIN | DESCRIPTION |
|-----|-------------|
| 1 | source |
| 2 | drain |
| 3 | gate 2 |
| 4 | gate 1 |



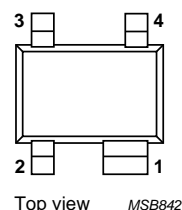
BF1211 marking code: LFP

Fig.1 Simplified outline (SOT143B).



BF1211R marking code: LHP

Fig.2 Simplified outline (SOT143R).



BF1211WR marking code: MK

Fig.3 Simplified outline (SOT343R).

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------|------------------------------|--|------|------|------|------------|
| V_{DS} | drain-source voltage | | – | – | 6 | V |
| I_D | drain current | | – | – | 30 | mA |
| P_{tot} | total power dissipation | | – | – | 180 | mW |
| $ y_{fs} $ | forward transfer admittance | | 25 | 30 | 40 | mS |
| C_{ig1-ss} | input capacitance at gate 1 | | – | 2.1 | 2.6 | pF |
| C_{rss} | reverse transfer capacitance | $f = 1\text{ MHz}$ | – | 15 | 30 | fF |
| F | noise figure | $f = 400\text{ MHz}$ | – | 0.9 | 1.6 | dB |
| X_{mod} | cross-modulation | input level for $k = 1\%$ at 40 dB AGC | 100 | 105 | – | dB μ V |
| T_j | junction temperature | | – | – | 150 | °C |

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CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|---|---------|
| | NAME | DESCRIPTION | VERSION |
| BF1211 | – | plastic surface mounted package; 4 leads | SOT143B |
| BF1211R | – | plastic surface mounted package; reverse pinning; 4 leads | SOT143R |
| BF1211WR | – | plastic surface mounted package; reverse pinning; 4 leads | SOT343R |

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------|--|---|------|----------|--------------------|
| V_{DS} | drain-source voltage | | – | 6 | V |
| I_D | drain current (DC) | | – | 30 | mA |
| I_{G1} | gate 1 current | | – | ± 10 | mA |
| I_{G2} | gate 2 current | | – | ± 10 | mA |
| P_{tot} | total power dissipation BF1211; BF1211R | $T_s \leq 116\text{ }^{\circ}\text{C}$; note 1 | – | 180 | mW |
| | BF1211WR | $T_s \leq 122\text{ }^{\circ}\text{C}$; note 1 | – | 180 | mW |
| T_{stg} | storage temperature | | –65 | +150 | $^{\circ}\text{C}$ |
| T_j | junction temperature | | – | 150 | $^{\circ}\text{C}$ |

Note

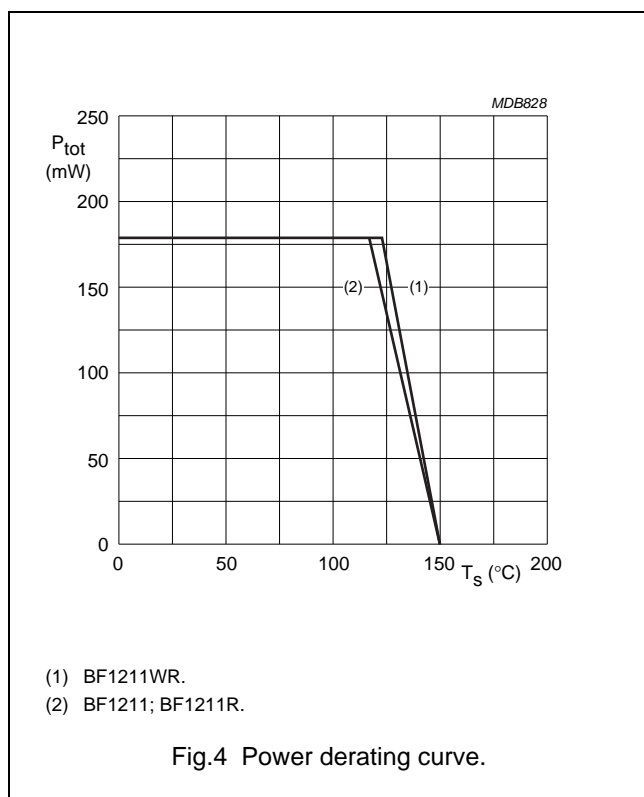
1. T_s is the temperature of the soldering point of the source lead.

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---------------|---|-------|------|
| $R_{th(j-s)}$ | thermal resistance from junction to soldering point | | |
| | BF1211; BF1211R | 185 | K/W |
| | BF1211WR | 155 | K/W |

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STATIC CHARACTERISTICS

$T_j = 25^\circ\text{C}$ unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|-----------------|---------------------------------|---|------|------|------|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{G1-S} = V_{G2-S} = 0\text{ V}$; $I_D = 10\text{ }\mu\text{A}$ | 6 | — | V |
| $V_{(BR)G1-SS}$ | gate 1-source breakdown voltage | $V_{G2-S} = V_{DS} = 0\text{ V}$; $I_{G1-S} = 10\text{ mA}$ | 6 | 10 | V |
| $V_{(BR)G2-SS}$ | gate 2-source breakdown voltage | $V_{G1-S} = V_{DS} = 0\text{ V}$; $I_{G2-S} = 10\text{ mA}$ | 6 | 10 | V |
| $V_{(F)S-G1}$ | forward source-gate 1 voltage | $V_{G2-S} = V_{DS} = 0\text{ V}$; $I_{S-G1} = 10\text{ mA}$ | 0.5 | 1.5 | V |
| $V_{(F)S-G2}$ | forward source-gate 2 voltage | $V_{G1-S} = V_{DS} = 0\text{ V}$; $I_{S-G2} = 10\text{ mA}$ | 0.5 | 1.5 | V |
| $V_{G1-S(th)}$ | gate 1-source threshold voltage | $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$ | 0.3 | 1 | V |
| $V_{G2-S(th)}$ | gate 2-source threshold voltage | $V_{G1-S} = 5\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$ | 0.35 | 1 | V |
| I_{DSX} | drain-source current | $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_{G1} = 75\text{ k}\Omega$; note 1 | 11 | 19 | mA |
| I_{G1-S} | gate 1 cut-off current | $V_{G2-S} = V_{DS} = 0\text{ V}$; $V_{G1-S} = 5\text{ V}$ | — | 50 | nA |
| I_{G2-S} | gate 2 cut-off current | $V_{G1-S} = V_{DS} = 0\text{ V}$; $V_{G2-S} = 4\text{ V}$ | — | 20 | nA |

Note

1. R_{G1} connects G_1 to $V_{GG} = 5\text{ V}$.

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DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ °C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 15\text{ mA}$; unless otherwise specified.

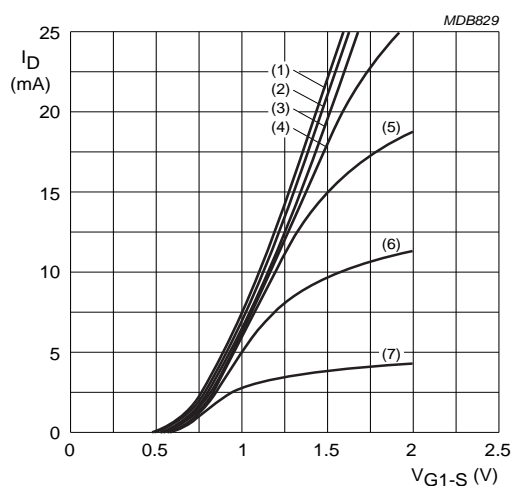
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------|------------------------------|--|------|------|------|------------|
| $ y_{fs} $ | forward transfer admittance | pulsed; $T_j = 25\text{ °C}$ | 25 | 30 | 40 | mS |
| C_{ig1-ss} | input capacitance at gate 1 | $f = 1\text{ MHz}$ | – | 2.1 | 2.6 | pF |
| C_{ig2-ss} | input capacitance at gate 2 | $f = 1\text{ MHz}$ | – | 1.1 | – | pF |
| C_{oss} | output capacitance | $f = 1\text{ MHz}$ | – | 0.9 | – | pF |
| C_{rss} | reverse transfer capacitance | $f = 1\text{ MHz}$ | – | 15 | 30 | fF |
| F | noise figure | $f = 11\text{ MHz}$; $G_S = 20\text{ mS}$; $B_S = 0$ | – | 3.5 | – | dB |
| | | $f = 400\text{ MHz}$; $Y_S = Y_{S(opt)}$ | – | 0.9 | 1.6 | dB |
| | | $f = 800\text{ MHz}$; $Y_S = Y_{S(opt)}$ | – | 1.3 | 2 | dB |
| G_{tr} | power gain | $f = 200\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 0.5\text{ mS}$; $B_L = B_{L(opt)}$ | – | 34 | – | dB |
| | | $f = 400\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 1\text{ mS}$; $B_L = B_{L(opt)}$ | – | 29 | – | dB |
| | | $f = 800\text{ MHz}$; $G_S = 3.3\text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 1\text{ mS}$; $B_L = B_{L(opt)}$ | – | 24 | – | dB |
| X_{mod} | cross-modulation | input level for $k = 1\%$; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 1 | | | | |
| | | at 0 dB AGC | 90 | – | – | dB μ V |
| | | at 10 dB AGC | – | 92 | – | dB μ V |
| | | at 40 dB AGC | 100 | 105 | – | dB μ V |

Note

1. Measured in test circuit Fig.21.

N-channel dual-gate MOS-FETs

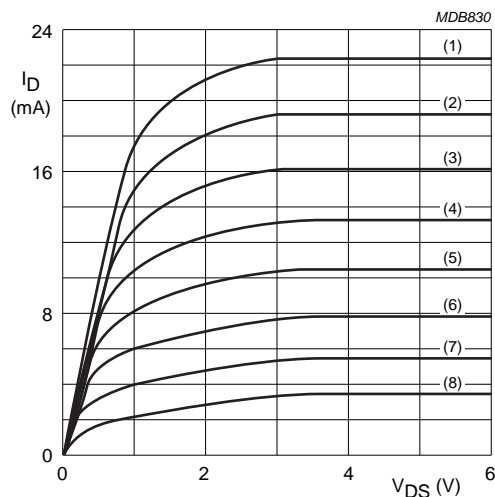
BF1211; BF1211R; BF1211WR



$V_{DS} = 5 \text{ V}$; $T_j = 25^\circ\text{C}$.

- | | | |
|----------------------------------|----------------------------------|--------------------------------|
| (1) $V_{G2-S} = 4 \text{ V}$. | (4) $V_{G2-S} = 2.5 \text{ V}$. | (7) $V_{G2-S} = 1 \text{ V}$. |
| (2) $V_{G2-S} = 3.5 \text{ V}$. | (5) $V_{G2-S} = 2 \text{ V}$. | |
| (3) $V_{G2-S} = 3 \text{ V}$. | (6) $V_{G2-S} = 1.5 \text{ V}$. | |

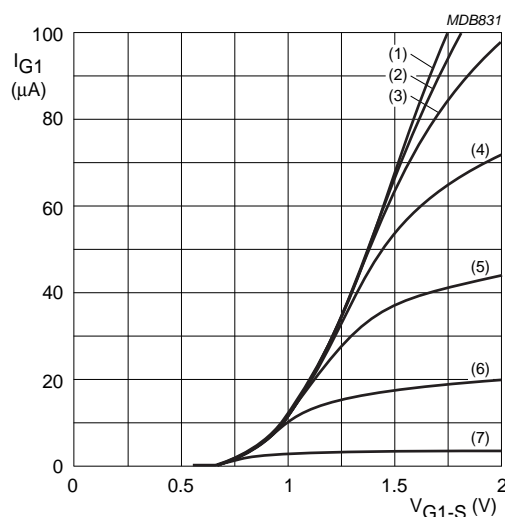
Fig.5 Transfer characteristics; typical values.



$V_{G2-S} = 4 \text{ V}$; $T_j = 25^\circ\text{C}$.

- | | | |
|----------------------------------|----------------------------------|----------------------------------|
| (1) $V_{G1-S} = 1.5 \text{ V}$. | (4) $V_{G1-S} = 1.2 \text{ V}$. | (7) $V_{G1-S} = 0.9 \text{ V}$. |
| (2) $V_{G1-S} = 1.4 \text{ V}$. | (5) $V_{G1-S} = 1.1 \text{ V}$. | (8) $V_{G1-S} = 0.8 \text{ V}$. |
| (3) $V_{G1-S} = 1.3 \text{ V}$. | (6) $V_{G1-S} = 1 \text{ V}$. | |

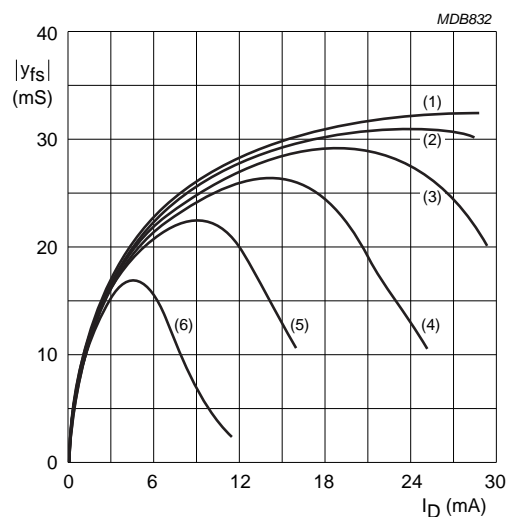
Fig.6 Output characteristics; typical values.



$V_{DS} = 5 \text{ V}$; $T_j = 25^\circ\text{C}$.

- | | | |
|----------------------------------|----------------------------------|--------------------------------|
| (1) $V_{G2-S} = 4 \text{ V}$. | (4) $V_{G2-S} = 2.5 \text{ V}$. | (7) $V_{G2-S} = 1 \text{ V}$. |
| (2) $V_{G2-S} = 3.5 \text{ V}$. | (5) $V_{G2-S} = 2 \text{ V}$. | |
| (3) $V_{G2-S} = 3 \text{ V}$. | (6) $V_{G2-S} = 1.5 \text{ V}$. | |

Fig.7 Gate 1 current as a function of gate 1 voltage; typical values.



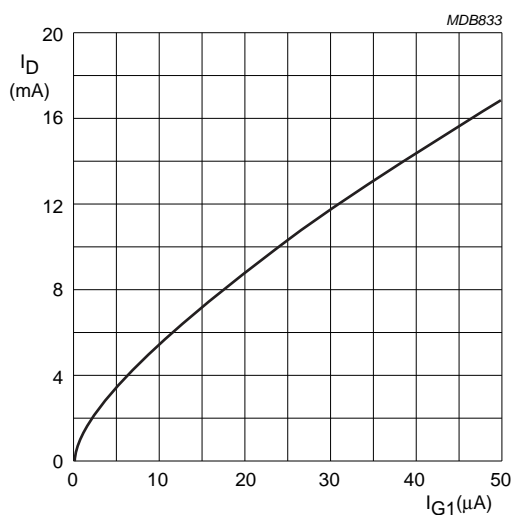
$V_{DS} = 5 \text{ V}$; $T_j = 25^\circ\text{C}$.

- | | | |
|----------------------------------|----------------------------------|----------------------------------|
| (1) $V_{G2-S} = 4 \text{ V}$. | (3) $V_{G2-S} = 3 \text{ V}$. | (5) $V_{G2-S} = 2 \text{ V}$. |
| (2) $V_{G2-S} = 3.5 \text{ V}$. | (4) $V_{G2-S} = 2.5 \text{ V}$. | (6) $V_{G2-S} = 1.5 \text{ V}$. |

Fig.8 Forward transfer admittance as a function of drain current; typical values.

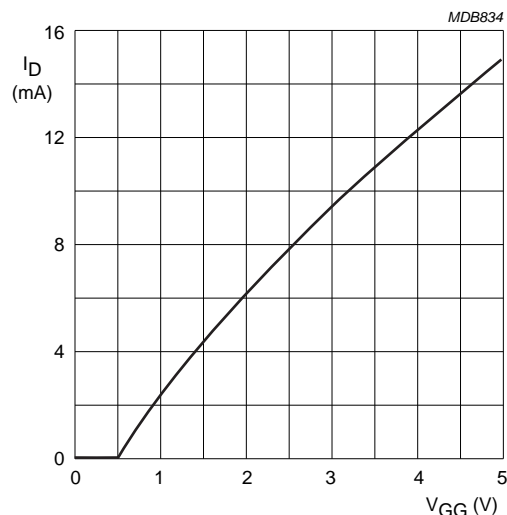
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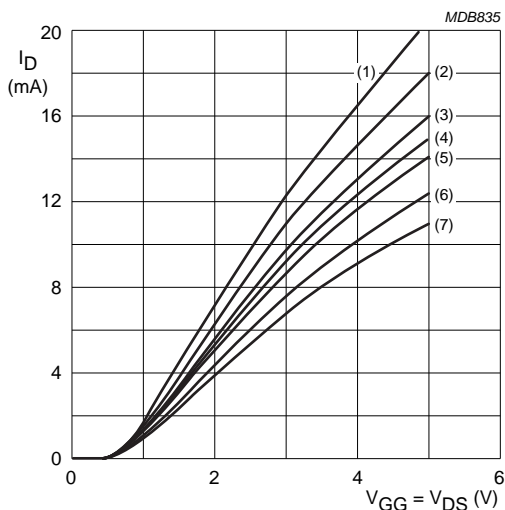
$V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$.
 $T_j = 25\text{ }^{\circ}\text{C}$.

Fig.9 Drain current as a function of gate 1 current; typical values.



$V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$.
 $R_{G1} = 75\text{ k}\Omega$ (connected to V_{GG}); see Fig.21.

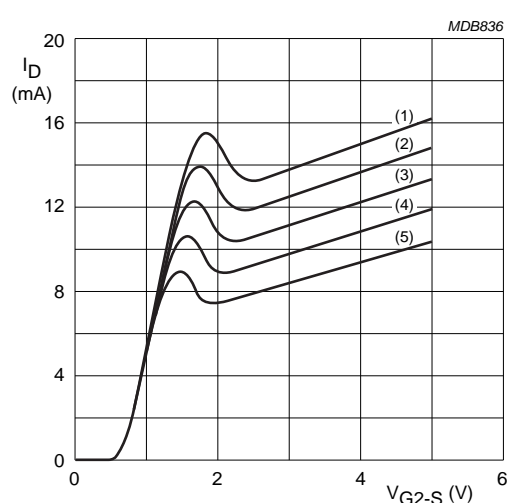
Fig.10 Drain current as a function of gate 1 supply voltage (V_{GG}); typical values.



$V_{G2-S} = 4\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; R_{G1} connected to V_{GG} ; see Fig.21.

- | | | |
|------------------------------------|-------------------------------------|-------------------------------------|
| (1) $R_{G1} = 47\text{ k}\Omega$. | (4) $R_{G1} = 75\text{ k}\Omega$. | (7) $R_{G1} = 120\text{ k}\Omega$. |
| (2) $R_{G1} = 56\text{ k}\Omega$. | (5) $R_{G1} = 82\text{ k}\Omega$. | |
| (3) $R_{G1} = 68\text{ k}\Omega$. | (6) $R_{G1} = 100\text{ k}\Omega$. | |

Fig.11 Drain current as a function of gate 1 (V_{GG}) and drain supply voltage; typical values.



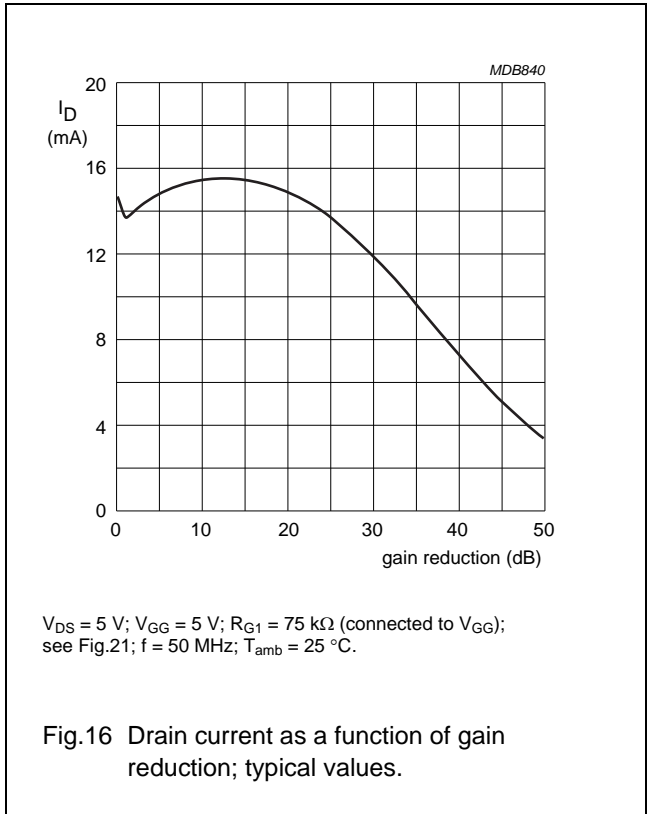
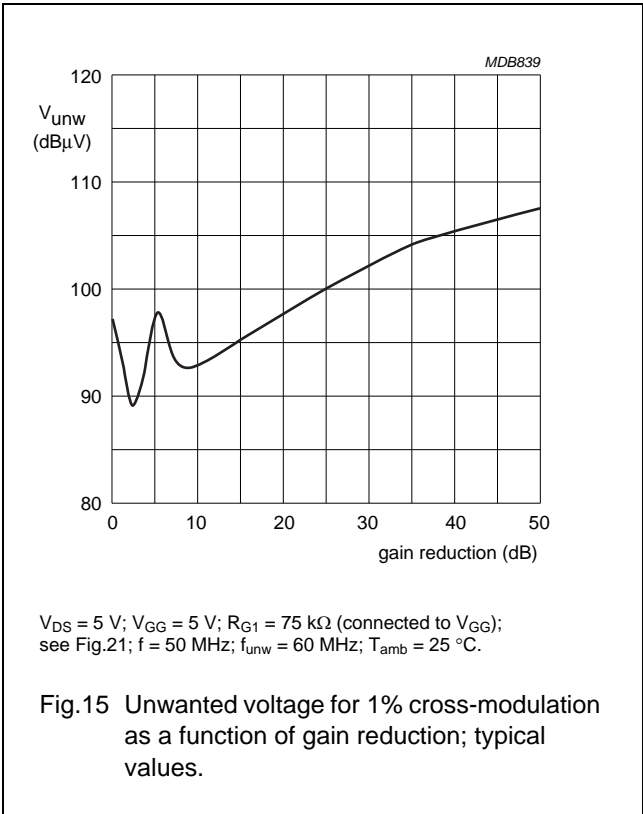
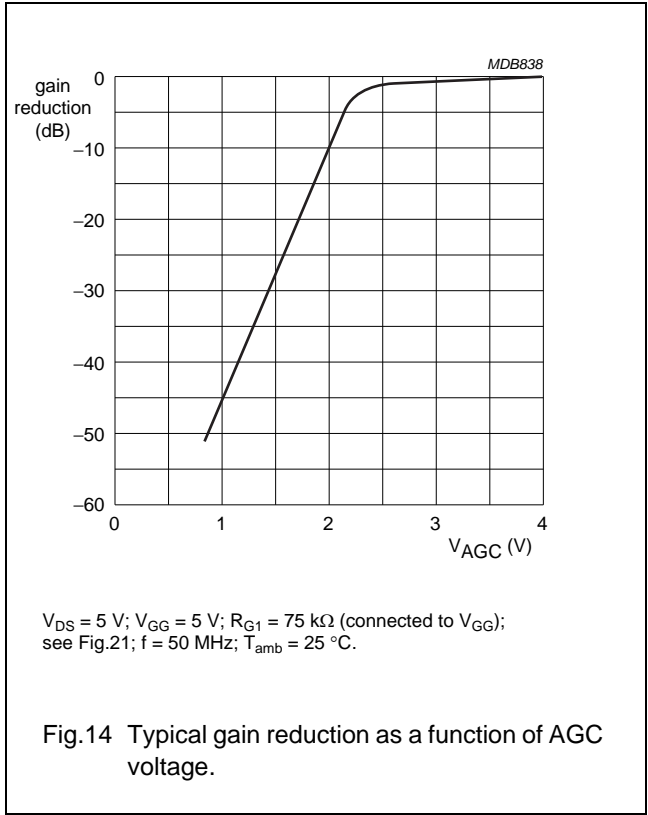
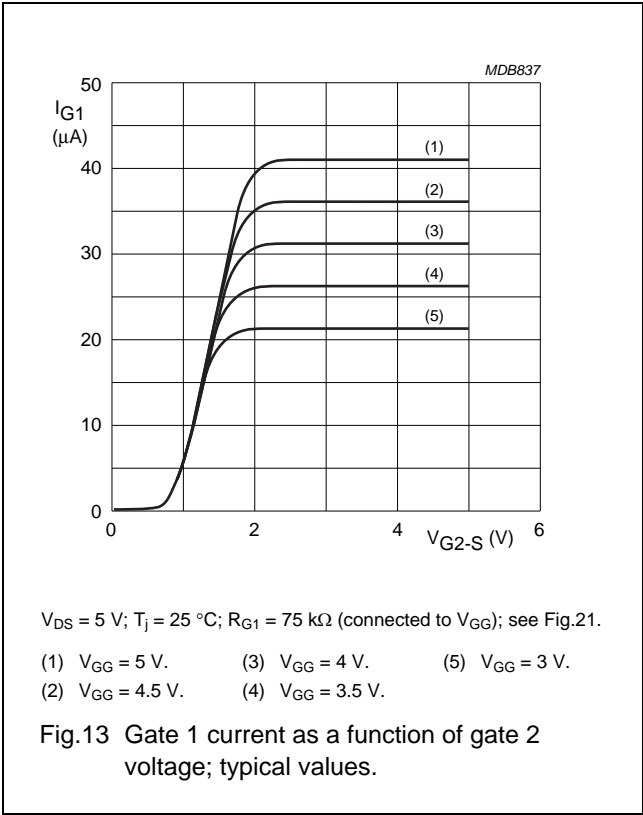
$V_{DS} = 5\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; $R_{G1} = 75\text{ k}\Omega$ (connected to V_{GG}); see Fig.21.

- | | |
|-------------------------------|-------------------------------|
| (1) $V_{GG} = 5\text{ V}$. | (4) $V_{GG} = 3.5\text{ V}$. |
| (2) $V_{GG} = 4.5\text{ V}$. | (5) $V_{GG} = 3\text{ V}$. |
| (3) $V_{GG} = 4\text{ V}$. | |

Fig.12 Drain current as a function of gate 2 voltage; typical values.

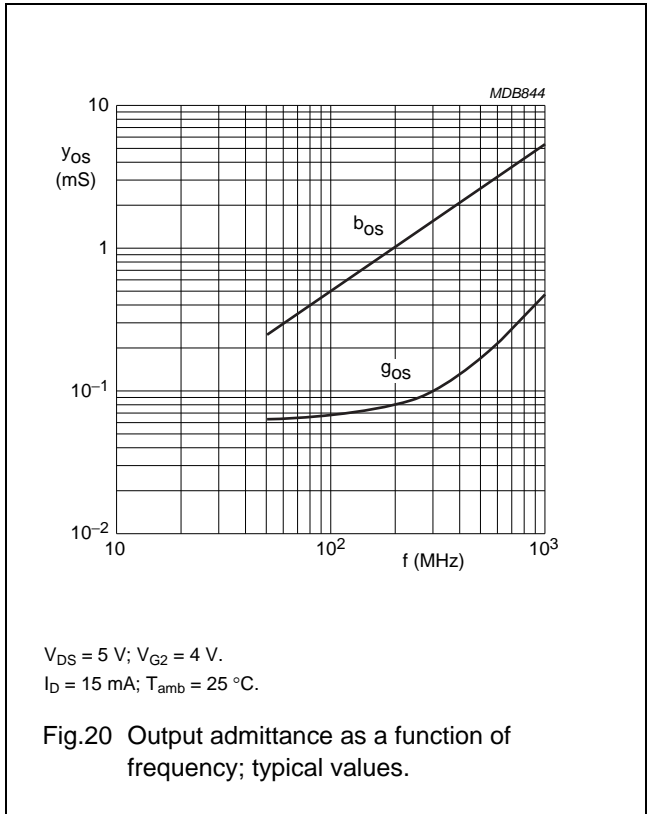
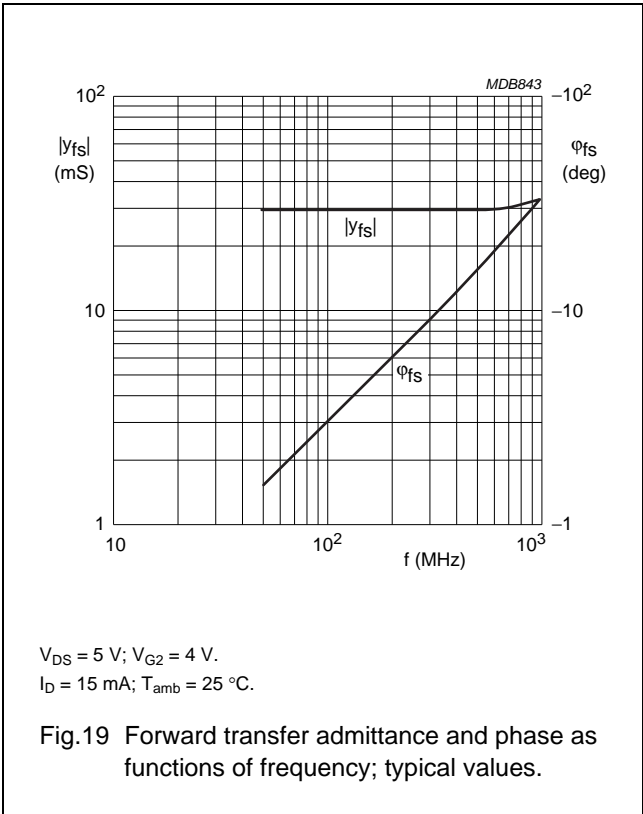
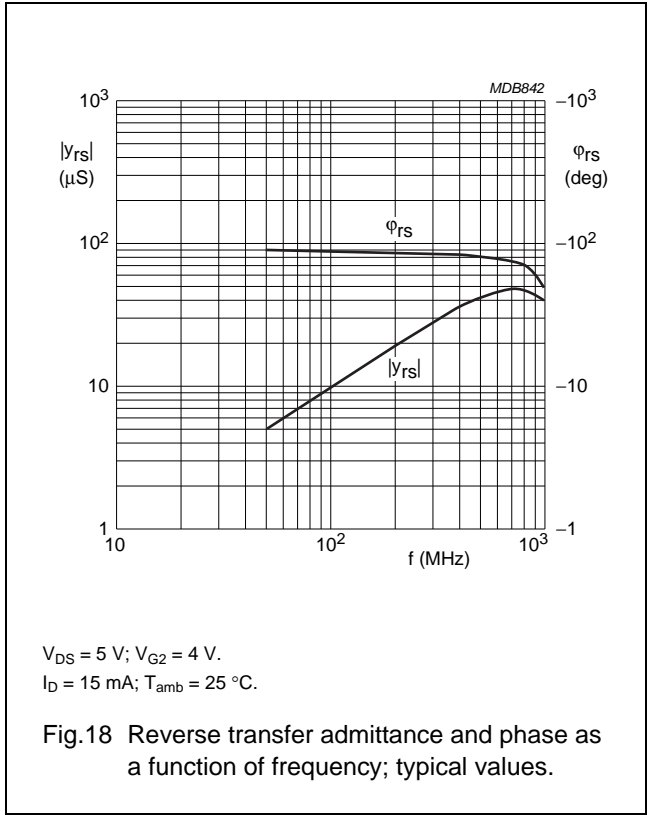
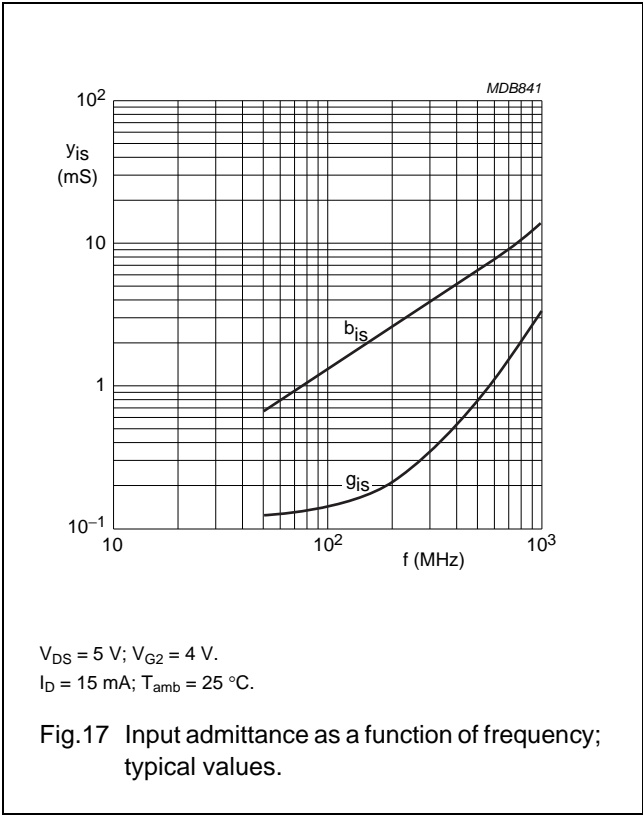
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BF1211; BF1211R; BF1211WR



N-channel dual-gate MOS-FETs

BF1211; BF1211R; BF1211WR

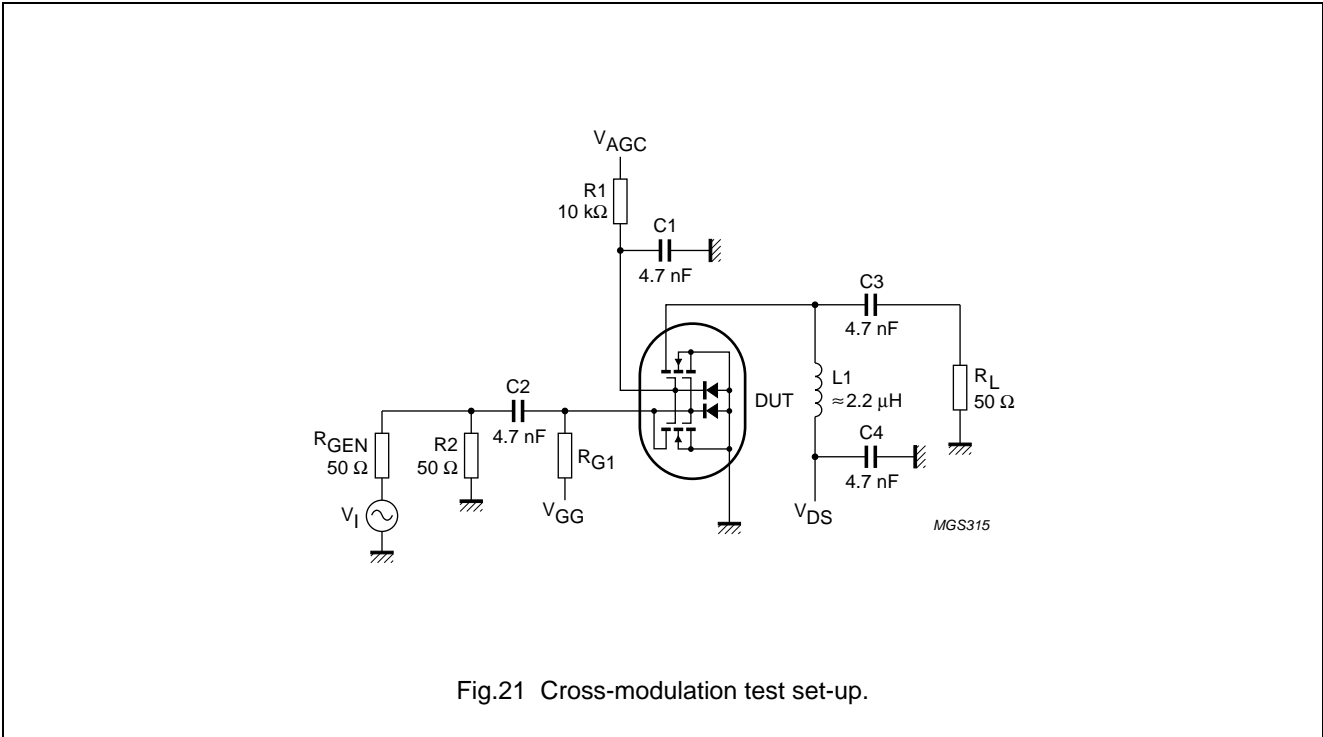


Table 1 Scattering parameters: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

| f (MHz) | S ₁₁ | | S ₂₁ | | S ₁₂ | | S ₂₂ | |
|------------|----------------------|----------------|----------------------|----------------|----------------------|----------------|----------------------|----------------|
| | MAGNITUDE (ratio) | ANGLE (deg) | MAGNITUDE (ratio) | ANGLE (deg) | MAGNITUDE (ratio) | ANGLE (deg) | MAGNITUDE (ratio) | ANGLE (deg) |
| 50 | 0.987 | −3.86 | 2.928 | 175.8 | 0.0005 | 89.3 | 0.993 | −1.58 |
| 100 | 0.985 | −7.73 | 2.921 | 171.6 | 0.0010 | 86.9 | 0.993 | −3.14 |
| 200 | 0.979 | −15.25 | 2.807 | 163.2 | 0.0015 | 91.1 | 0.993 | −6.31 |
| 300 | 0.965 | −22.84 | 2.846 | 155.0 | 0.0028 | 77.4 | 0.988 | −9.41 |
| 400 | 0.949 | −30.15 | 2.784 | 146.7 | 0.0034 | 74.0 | 0.985 | −12.48 |
| 500 | 0.929 | −30.25 | 2.704 | 138.9 | 0.0037 | 71.4 | 0.981 | −15.54 |
| 600 | 0.904 | −44.24 | 2.639 | 130.9 | 0.0040 | 69.6 | 0.976 | −18.59 |
| 700 | 0.876 | −51.16 | 2.558 | 123.0 | 0.0039 | 69.0 | 0.971 | −21.65 |
| 800 | 0.846 | −58.16 | 2.486 | 115.1 | 0.0037 | 70.0 | 0.965 | −24.27 |
| 900 | 0.816 | −65.15 | 2.402 | 107.2 | 0.0032 | 74.5 | 0.960 | −27.79 |
| 1000 | 0.791 | −72.22 | 2.315 | 99.9 | 0.0028 | 87.1 | 0.956 | −30.94 |

Table 2 Noise data: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 15\text{ mA}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

| f (MHz) | F _{min} (dB) | Γ _{opt} | | R _n (Ω) |
|------------|--------------------------|------------------|-------|-----------------------|
| | | (ratio) | (deg) | |
| 400 | 0.9 | 0.693 | 16.75 | 29.85 |
| 800 | 1.3 | 0.707 | 37.33 | 29.90 |

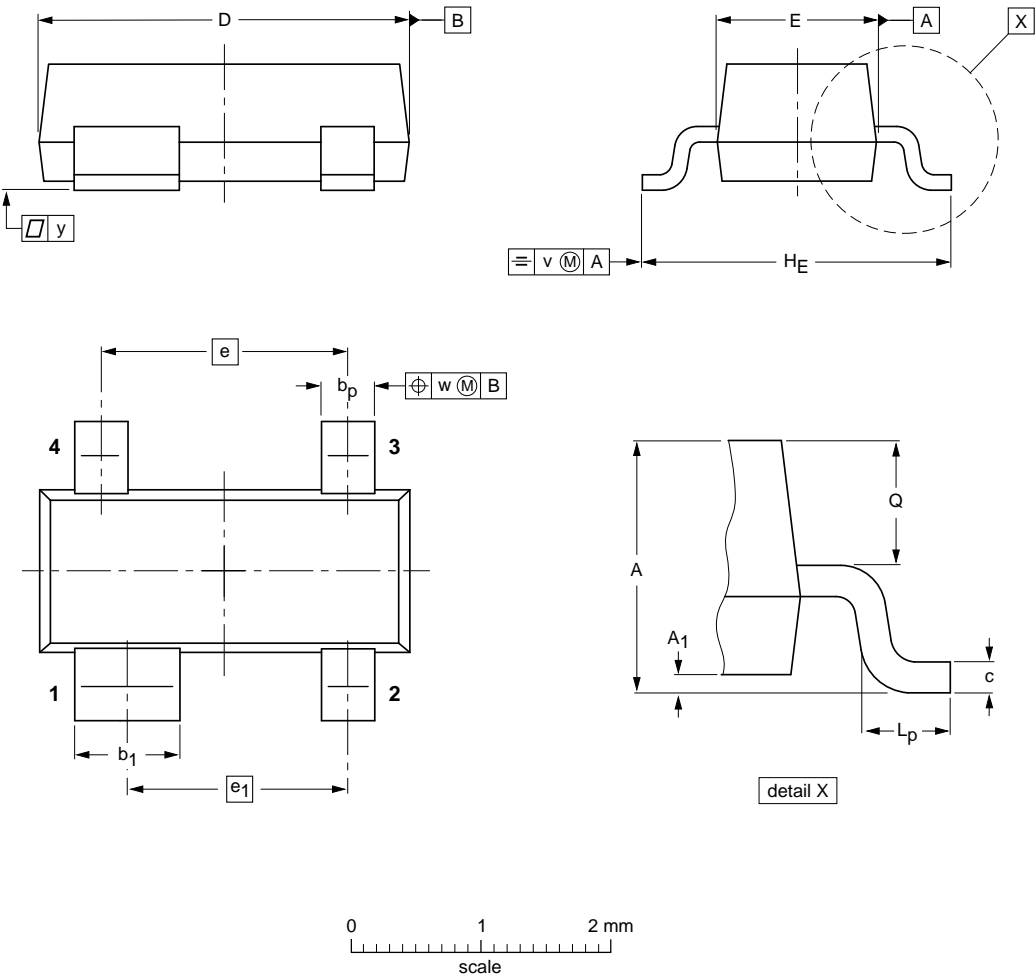
N-channel dual-gate MOS-FETs

BF1211; BF1211R; BF1211WR

PACKAGE OUTLINES

Plastic surface-mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

| UNIT | A | A ₁ max | b _p | b ₁ | c | D | E | e | e ₁ | H _E | L _p | Q | v | w | y |
|------|------------|-----------------------|----------------|----------------|--------------|------------|------------|-----|----------------|----------------|----------------|--------------|-----|-----|-----|
| mm | 1.1 0.9 | 0.1 | 0.48 0.38 | 0.88 0.78 | 0.15 0.09 | 3.0 2.8 | 1.4 1.2 | 1.9 | 1.7 | 2.5 2.1 | 0.45 0.15 | 0.55 0.45 | 0.2 | 0.1 | 0.1 |

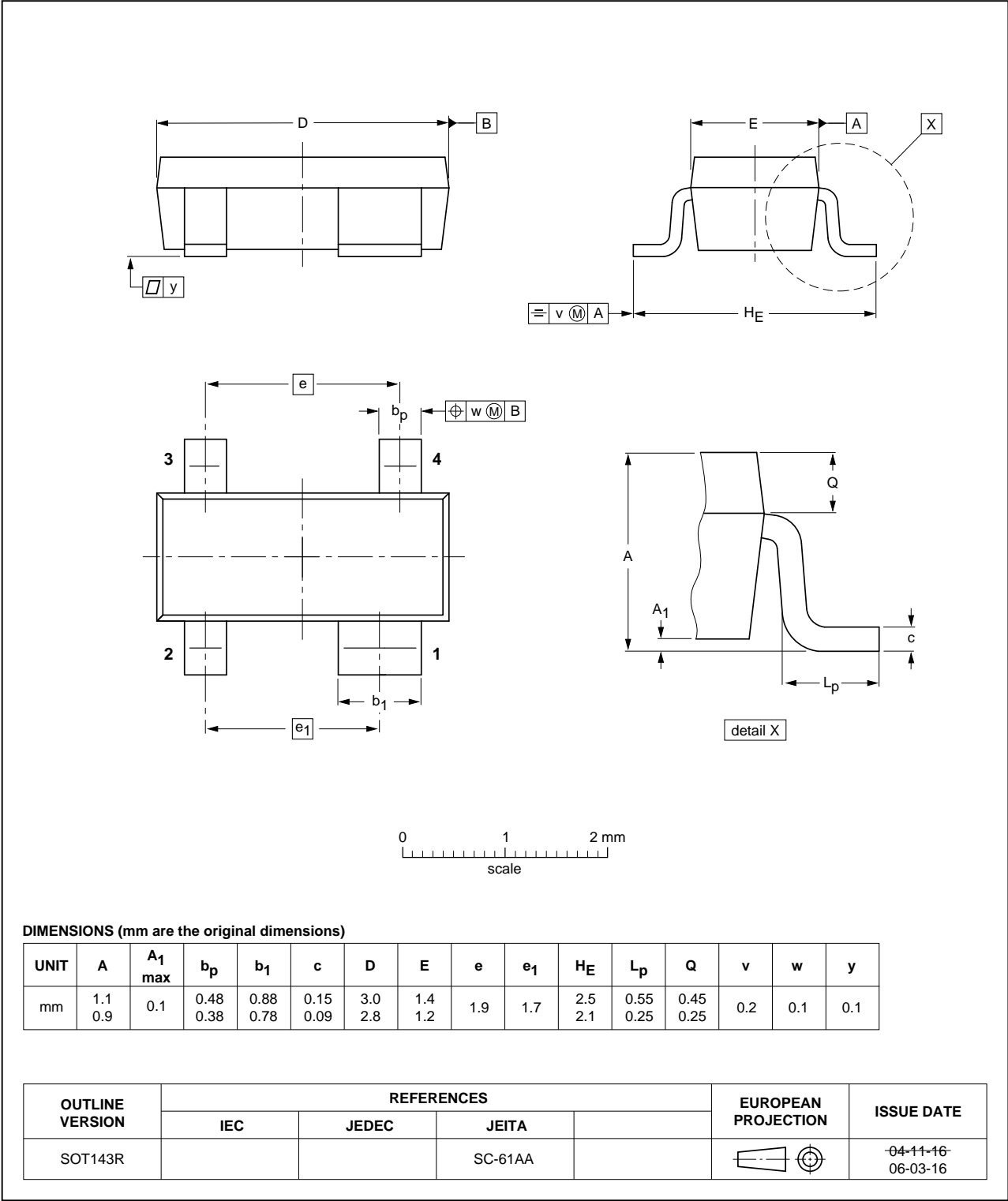
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|-------|-------|--|------------------------|----------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT143B | | | | | | 04-11-16 06-03-16 |

N-channel dual-gate MOS-FETs

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Plastic surface-mounted package; reverse pinning; 4 leads

SOT143R

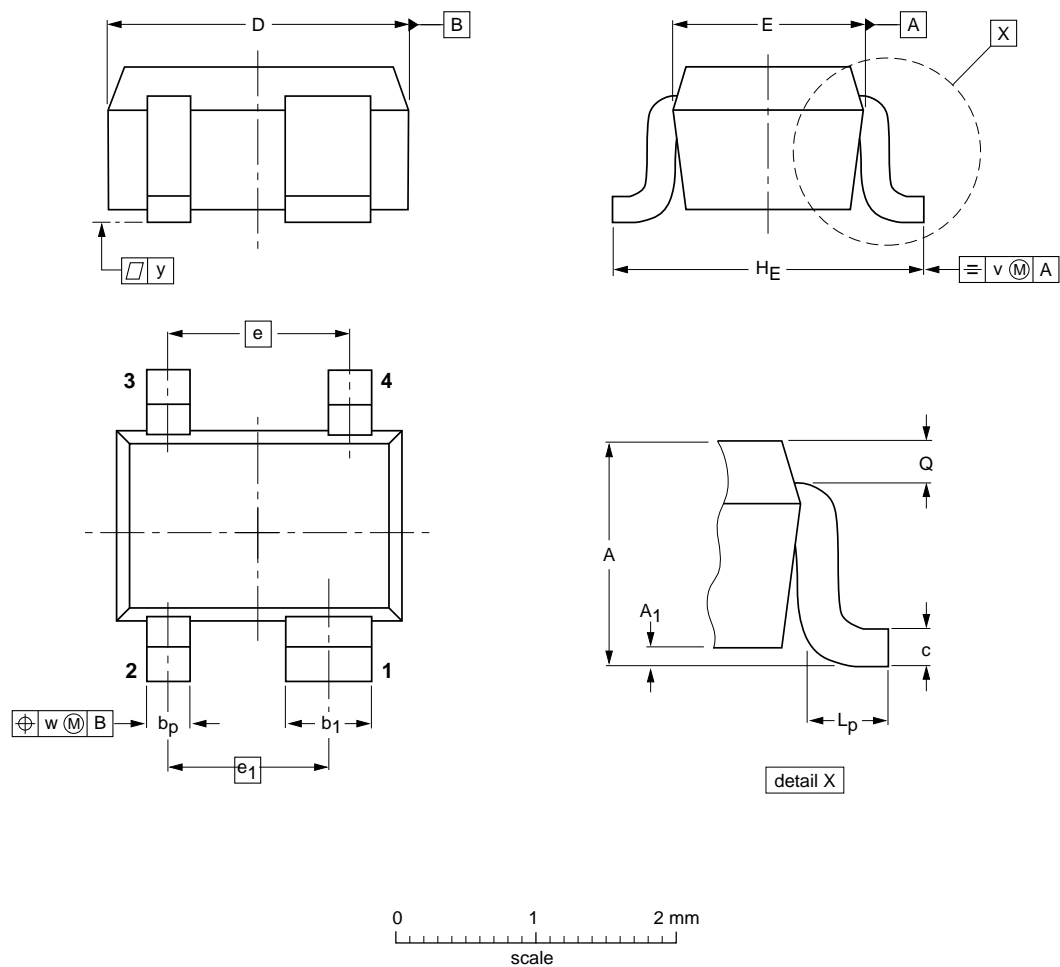


N-channel dual-gate MOS-FETs

BF1211; BF1211R; BF1211WR

Plastic surface-mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

| UNIT | A | A ₁ max | b _p | b ₁ | c | D | E | e | e ₁ | H _E | L _p | Q | v | w | y |
|------|------------|-----------------------|----------------|----------------|--------------|------------|--------------|-----|----------------|----------------|----------------|--------------|-----|-----|-----|
| mm | 1.1 0.8 | 0.1 | 0.4 0.3 | 0.7 0.5 | 0.25 0.10 | 2.2 1.8 | 1.35 1.15 | 1.3 | 1.15 | 2.2 2.0 | 0.45 0.15 | 0.23 0.13 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|-------|------|--|------------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT343R | | | | | | 97-05-21 06-03-16 |

N-channel dual-gate MOS-FETs

BF1211; BF1211R; BF1211WR

DATA SHEET STATUS

| DOCUMENT STATUS ⁽¹⁾ | PRODUCT STATUS ⁽²⁾ | DEFINITION |
|--------------------------------|-------------------------------|---|
| Objective data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary data sheet | Qualification | This document contains data from the preliminary specification. |
| Product data sheet | Production | This document contains the product specification. |

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

DEFINITIONS

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

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N-channel dual-gate MOS-FETsBF1211; BF1211R; BF1211WR

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This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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