

# DATA SHEET

## **CBT6832D**

16-bit controlled enable rate  
1-of-2 multiplexer/demultiplexer  
with precharged outputs and charge pump  
undershoot protection for live insertion

Product specification  
Supersedes data of 2000 May 18

2000 Sep 01

# 16-bit controlled enable rate 1-of-2 multiplexer/demultiplexer with precharged outputs and charge pump undershoot protection for live insertion

# CBT6832D

## FEATURES

- 5  $\Omega$  typical  $r_{on}$
- Pull-up on B port
- Undershoot protection on A port only:  $-2.0$  V
- Near zero propagation delay
- Controlled enable rate
- $V_{CC}$  operating range:  $+4.5$  V to  $+5.5$  V
- $> 100$  MHz bandwidth (or clock rate) at 20 pF load capacitance
- 56-pin TSSOP package
- Bias voltage pre-charges the B output when the channel is disabled
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

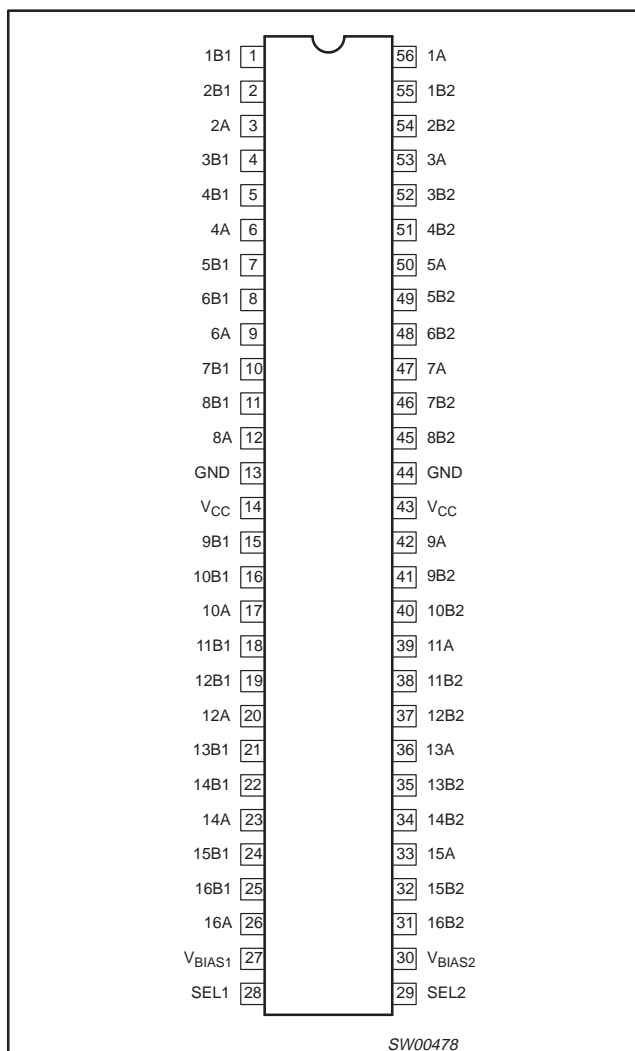
## APPLICATION

- Provides PCI-X hot-plugging

## DESCRIPTION

The CBT6832D is a 16-bit controlled enable rate 1-of-2 multiplexer/demultiplexer with precharged outputs and charge pump undershoot protection for live insertion. Advantages of the CBT6832 include a propagation delay of 250 ps, resulting from 5  $\Omega$  channel resistance, and low I/O capacitance. A port demultiplexes to either 1B and 2B, or to both. The switch is bi-directional.

## PIN CONFIGURATION



## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$ ; $GND = 0$ V	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Bn or Bn to An	$C_L = 50$ pF; $V_{CC} = 5$ V	0.25	ns
$C_{IN}$	Input capacitance	$V_I = 0$ V or $V_{CC}$	4.5	pF
$C_{OFF\ B}$	B capacitance, switch off	Outputs disabled; $V_O = 0$ V	8	pF
$C_{OFF\ A}$	A capacitance, switch off	Outputs disabled; $V_O = 0$ V	13	pF
$C_{ON\ 1}$	One channel enabled capacitance	One B enabled; $V_O = 0$ V	21	pF
$C_{ON\ 2}$	Both channels enabled capacitance	Both B channels enabled; $V_O = 0$ V	34	pF

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
56-Pin Plastic TSSOP Type II	$0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	CBT6832D DGG	SOT364-1

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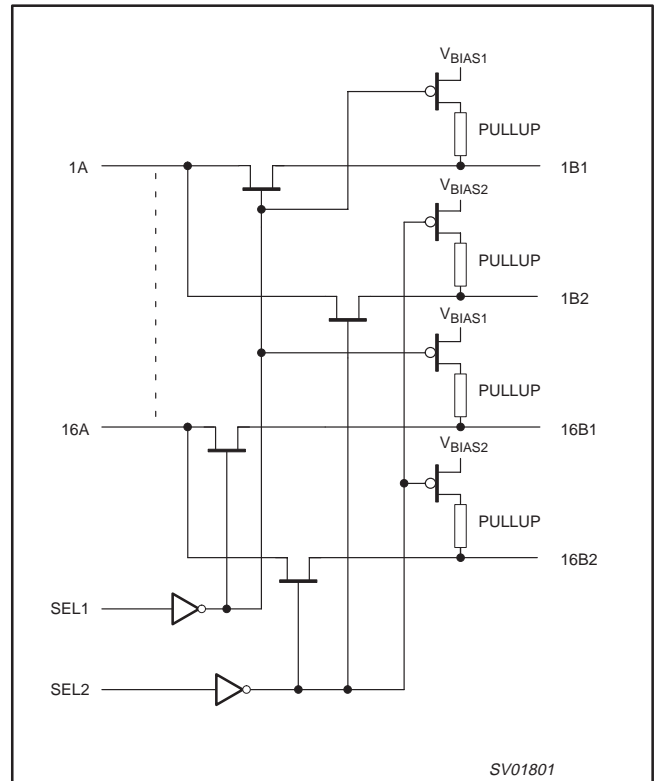
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
3, 6, 9, 12, 17, 20, 23, 26, 33, 36, 39, 42, 47, 50, 53, 56	1A1–16A1	Inputs
1, 2, 4, 5, 7, 8, 10, 11, 15, 16, 18, 19, 21, 22, 24, 25	1B1–16B1	Outputs
31, 32, 34, 35, 37, 38, 40, 41, 45, 46, 48, 49, 51, 52, 54, 55	1B2–16B2	Outputs
27, 30	$V_{BIAS1}$ , $V_{BIAS2}$	Precharge bias voltage inputs
28, 29	SEL1, SEL2	Select-control inputs
13, 44	GND	Ground (0 V)
14, 43	$V_{CC}$	Positive supply voltage

## FUNCTION TABLE

SEL1	SEL2	FUNCTION
L	H	nA to nB1
H	L	nA to nB2
L	L	nA to nB1 and nB2
H	H	nB1, nB2 = $V_{BIAS}$

## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
$V_{OUT}$	DC output voltage <sup>3</sup>	output in Off or High state	-0.5 to +7.0	V
$I_{OUT}$	DC output current	output in Low state	120	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$\theta_{JA}$	Power dissipation		95	°C/W

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level Input voltage		0.8	V
$T_{amb}$	Operating free-air temperature range	0	+70	°C

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## DC ELECTRICAL CHARACTERISTICS

Over operating temperature range  $T_{amb} = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ;  $V_{CC} = 5\text{ V} \pm 10\%$ ;  $V_{BIAS} = 1.3\text{ V}$  to  $V_{CC}$ , unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	Input HIGH voltage	Guaranteed logic HIGH level	2.0			V
V <sub>IL</sub>	Input LOW voltage	Guaranteed logic LOW level	−0.5		0.8	V
I <sub>IH</sub>	Input HIGH current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub>			±5	μA
I <sub>IL</sub>	Input LOW current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = GND			±5	μA
I <sub>OZH</sub>	High impedance output current	A = 0 V or V <sub>CC</sub> MAX, V <sub>BIAS1</sub> = V <sub>BIAS2</sub> = V <sub>CC</sub> MAX			±1	μA
I <sub>OZL</sub>	Low impedance output current	B = 0 V or V <sub>CC</sub> MAX, V <sub>BIAS1</sub> = V <sub>BIAS2</sub> = V <sub>CC</sub> MAX	−0.2		−2	mA
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5 V; I <sub>I</sub> = −18 mA		−0.7	−1.8	V
r <sub>on</sub>	Switch on resistance <sup>2</sup>	V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 0 V; I <sub>I</sub> = 48 mA		5	8	Ω
		V <sub>CC</sub> = 4.5 V; V <sub>I</sub> = 2.4 V; I <sub>I</sub> = −15 mA		10	15	Ω
Capacitance <sup>3</sup> (T <sub>amb</sub> = +25°C; f = 1 MHz)						
C <sub>IN</sub>	Input capacitance	V <sub>I</sub> = 0 V		4.5		pF
C <sub>OFF B</sub>	B capacitance, switch off	V <sub>I</sub> = 0 V		8		pF
C <sub>OFF A</sub>	A capacitance, switch off	V <sub>I</sub> = 0 V		13		pF
C <sub>ON 1</sub>	Capacitance, switch on (one B)	V <sub>I</sub> = 0 V		21		pF
C <sub>ON 2</sub>	Capacitance, both B channels enabled	V <sub>I</sub> = 0 V		34		pF
Power supply						
I <sub>CC</sub>	Quiescent supply current enabled	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = V <sub>CC</sub> or GND			200	μA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>5</sup>	V <sub>CC</sub> = 5.5 V, one input at 3.4 V, other inputs at V <sub>CC</sub> or GND			2.5	mA

### NOTES:

1. All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_{amb} = +25^{\circ}\text{C}$  ambient and maximum loading.
2. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.
3. These parameters are determined by device characterization, but is not production tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. Per TTL driven input ( $V_I = 3.4\text{ V}$ , control inputs only); A and B pins do not contribute to  $I_{CC}$ .
6. This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. this parameter is not tested, but is guaranteed by design.

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AC CHARACTERISTICS

$V_{CC} = 5.0\text{ V} \pm 0.5\text{ V}$ ;  $GND = 0\text{ V}$ ;  $C_L = 50\text{ pF}$ ,  $R_L = 500\text{ }\Omega$

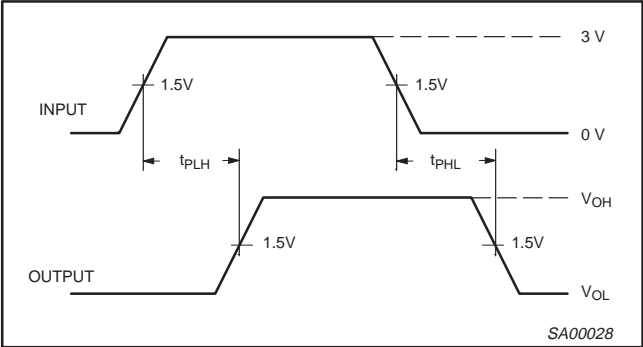
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
$t_{PLH}$ $t_{PHL}$	Propagation delay <sup>1</sup> A to B			0.25		ns
$t_{PZH}$ $t_{PZL}$	Bus enable time SEL to A, B		10 5		30 25	ns
$t_{PHZ}$ $t_{PLZ}$	Bus disable time SEL to A, B		0.5 0.5		6 7	ns

NOTE:

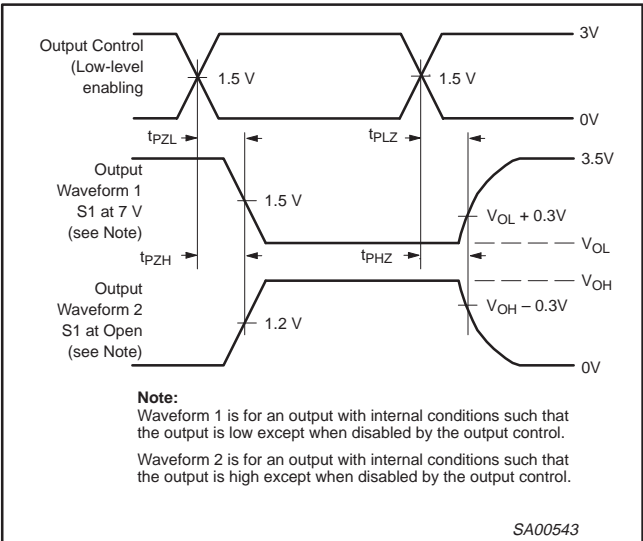
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

AC WAVEFORMS

$V_M = 1.5\text{ V}$ ,  $V_{IN} = GND\text{ to }3.0\text{ V}$



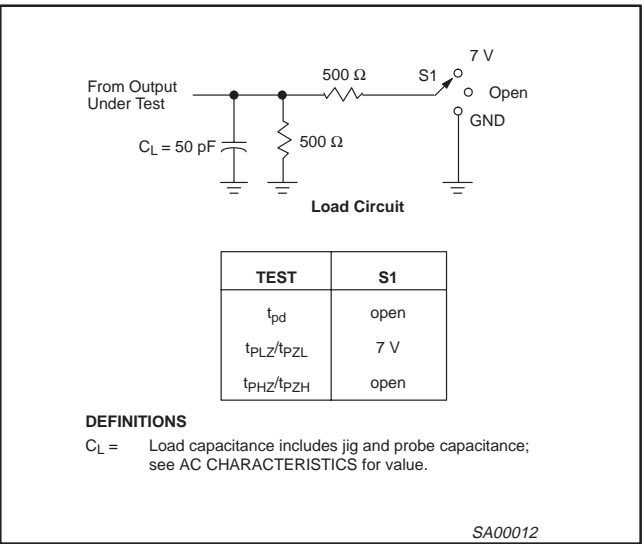
Waveform 1. Input (An) to Output (Bn) Propagation Delays



**Note:**  
Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS

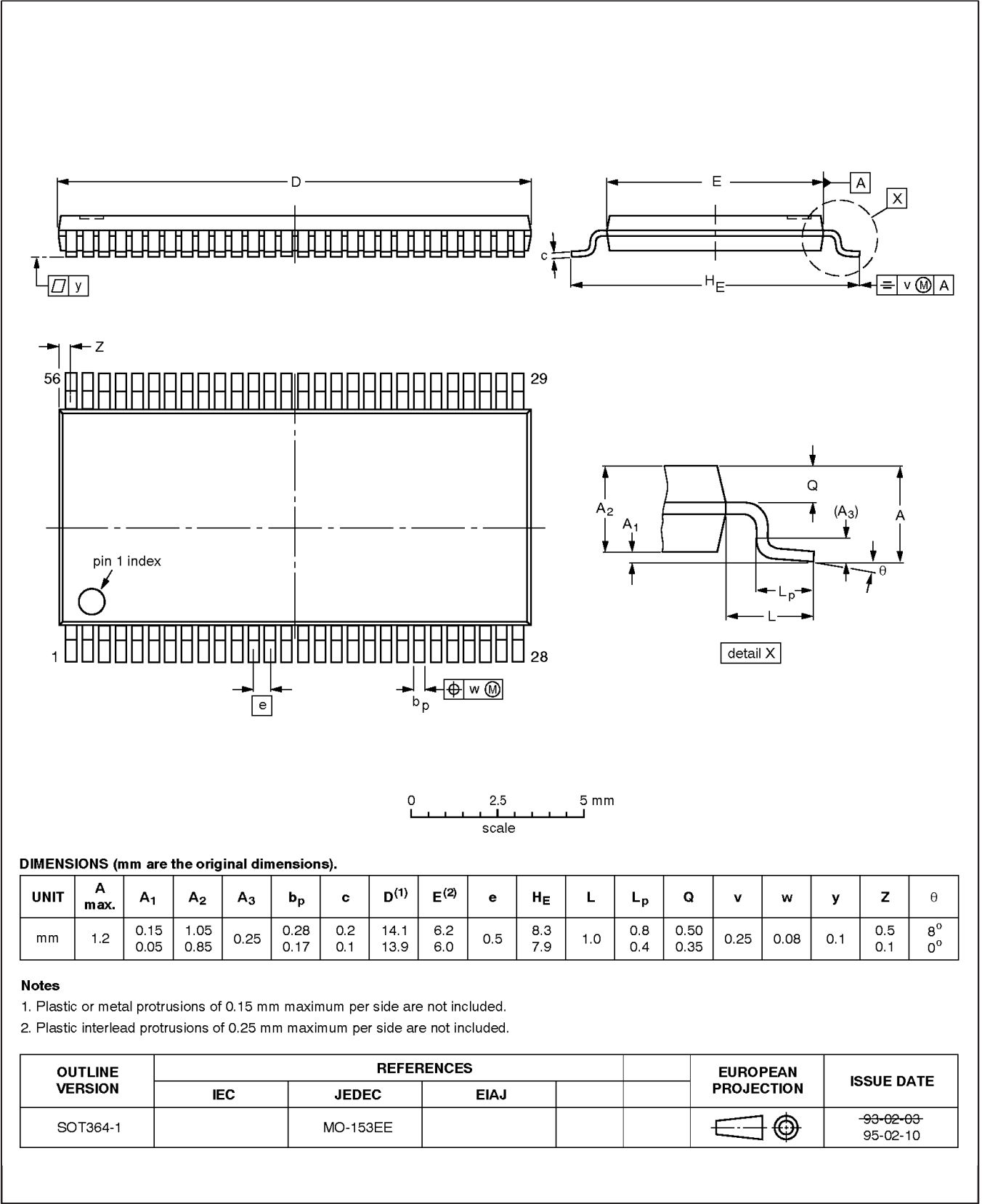


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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



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## NOTES

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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