

# DATA SHEET

## **GTL16612**

18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL  
bidirectional universal translator (3-State)

Product data  
Supersedes data of 2000 Jun 19

2002 Dec 13

# 18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL bidirectional universal translator (3-State)

**GTL16612**

## FEATURES

- 18-bit bidirectional bus interface
- Translates between GTL/GTL<sup>+</sup> logic levels (B ports) and LVTTTL/TTL logic levels (A ports)
- 5 V I/O tolerant on the LVTTTL/TTL side (A ports)
- No bus current loading when LVTTTL/TTL output is tied to 5 V bus
- 3-State buffers
- Output capability: +64 mA/-32 mA on the LVTTTL/TTL side (A ports); +40 mA on the GTL/GTL<sup>+</sup> side (B ports)
- TTL input levels on control pins
- Power-up reset
- Power-up 3-State
- Positive edge triggered clock inputs
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101

## DESCRIPTION

The GTL16612 is a high-performance BiCMOS product designed for V<sub>CC</sub> operation at 3.3 V with I/O compatibility up to 5 V.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is High. When LEAB is Low, the A data is latched if CPAB is held at a High or Low logic level. If LEAB is Low, the A-bus data is stored in the latch/flip-flop on the Low-to-High transition of CPAB. When  $\overline{OEAB}$  is Low, the outputs are active. When  $\overline{OEAB}$  is High, the outputs are in the high-impedance state. The clocks can be controlled with the clock-enable inputs ( $\overline{CEBA}/\overline{CEAB}$ ).

Data flow for B-to-A is similar to that of A-to-B but uses  $\overline{OEBA}$ , LEBA and CPBA.

## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T <sub>amb</sub> = 25 °C	TYPICAL	UNIT
			3.3 V	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay An to Bn or Bn to An	C <sub>L</sub> = 50 pF	1.9	ns
C <sub>IN</sub>	Input capacitance (Control pins)	V <sub>I</sub> = 0 V or V <sub>CC</sub>	4	pF
C <sub>I/O</sub>	I/O pin capacitance	Outputs disabled; V <sub>I/O</sub> = 0 V or V <sub>CC</sub>	8	pF
I <sub>CCZ</sub>	Total supply current	Outputs disabled	12	mA

## ORDERING INFORMATION

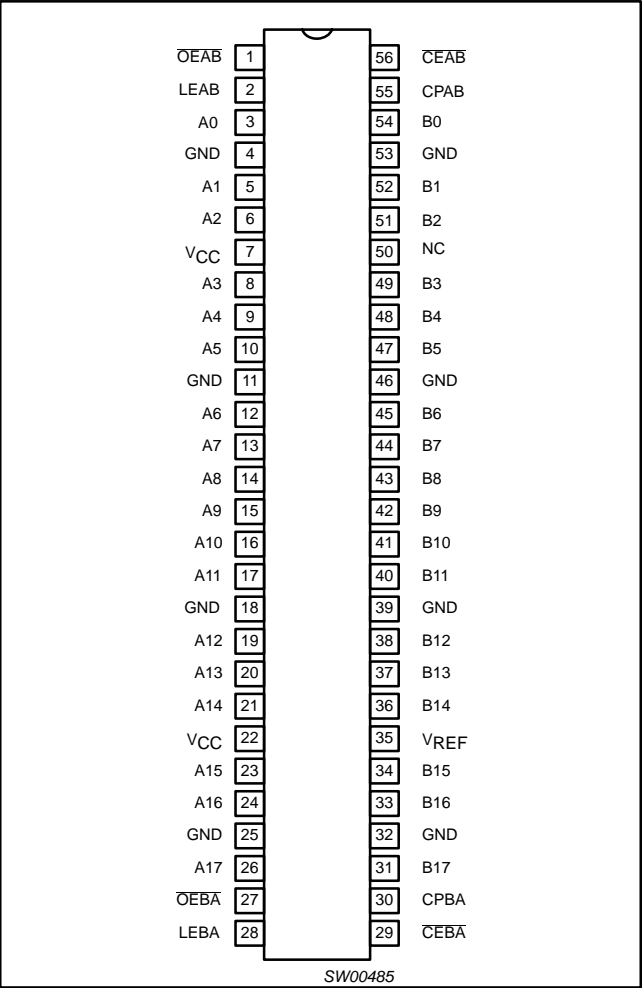
PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
56-Pin Plastic SSOP	-40 to +85 °C	GTL16612DL	SOT371-1
56-Pin Plastic TSSOP	-40 to +85 °C	GTL16612DGG	SOT364-1

Standard packing quantities and other packaging data is available at [www.philipslogic.com/packaging](http://www.philipslogic.com/packaging).

18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL bidirectional  
universal translator (3-State)

GTL16612

PIN CONFIGURATION



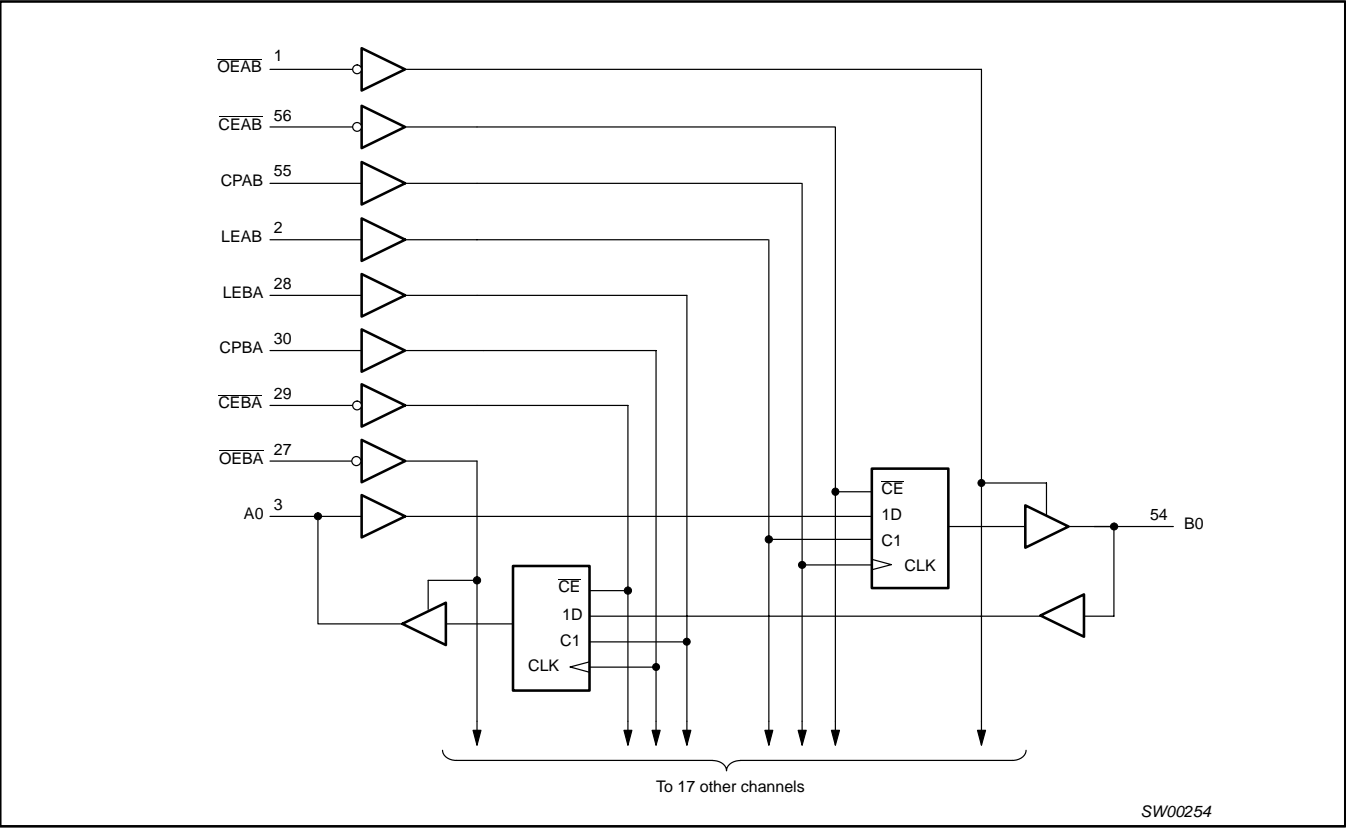
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 27	$\overline{OEAB}/\overline{OEBA}$	A-to-B/ B-to-A Output enable input (active Low)
29, 56	$\overline{CEBA}/\overline{CEAB}$	B-to-A/A-to-B clock enable
2, 28	$\overline{LEAB}/\overline{LEBA}$	A-to-B/B-to-A Latch enable input
55,30	$\overline{CPAB}/\overline{CPBA}$	A-to-B/B-to-A Clock input (active rising edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22	V <sub>CC</sub>	Positive supply voltage
35	V <sub>REF</sub>	GTL reference voltage
50	NC	No connection

18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

LOGIC SYMBOL (Positive Logic)



FUNCTION TABLE

INPUTS					OUTPUT B
CEAB <sup>1</sup>	OEAB <sup>1</sup>	LEAB <sup>1</sup>	CPAB <sup>1</sup>	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B <sub>O</sub> <sup>2</sup>
H	L	L	X	X	B <sub>O</sub> <sup>2</sup>
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	H	X	B <sub>O</sub> <sup>2</sup>
L	L	L	L	X	B <sub>O</sub> <sup>3</sup>

- X = Don't care  
H = High voltage level  
L = Low voltage level  
↑ = Low to High  
Z = High impedance "off" state
- A-to-B data flow is shown: B-to-A flow is similar but uses OEBA, LEBA, CPBA, and CEBA.
  - Output level before the indicated steady-state input conditions were established.
  - Output level before the indicated steady-state input conditions were established, provided that CPAB was Low before LEAB went Low.

# 18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

## ABSOLUTE MAXIMUM RATINGS 1, 2

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>	A port	-0.5 to +7.0	V
		B port	-0.5 to +4.6	
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0; A port	-50	mA
V <sub>O</sub>	DC output voltage <sup>3</sup>	Output in Off or High state; A port	-0.5 to +7.0	V
		Output in Off or High state; B port	-0.5 to +4.6	V
I <sub>OL</sub>	Current into any output in the LOW state	A port	128	mA
		B port	80	mA
I <sub>OH</sub>	Current into any output in the HIGH state	A port	-64	mA
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	3.3 V RANGE LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage		3.0	3.6	V
V <sub>TT</sub>	Termination voltage	GTL	1.14	1.26	V
		GTL <sup>+</sup>	1.35	1.65	
V <sub>REF</sub>	GTL reference voltage	GTL	0.74	0.87	V
		GTL <sup>+</sup>	0.9	1.10	
V <sub>I</sub>	Input voltage	B port	0	V <sub>TT</sub>	V
		Except B port	0	5.5	
V <sub>IH</sub>	HIGH-level input voltage	B port	V <sub>REF</sub> +50 mV		V
		Except B port	2.0		
V <sub>IL</sub>	LOW-level input voltage	B port		V <sub>REF</sub> -50 mV	V
		Except A port		0.8	
I <sub>OH</sub>	HIGH-level output current	A port		-32	mA
I <sub>OL</sub>	LOW-level output current	B port		40	mA
		A port		64	
T <sub>amb</sub>	Operating free-air temperature range		-40	+85	°C

# 18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

## DC ELECTRICAL CHARACTERISTICS (3.3 V $\pm$ 0.3 V RANGE)

SYMBOL	PARAMETER		TEST CONDITIONS		LIMITS			UNIT	
					Temp = -40 to +85 °C				
					MIN	TYP <sup>1</sup>	MAX		
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = 3.0 V; I <sub>IK</sub> = -18 mA			-0.85	-1.2	V	
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = 3.0 to 3.6 V; I <sub>OH</sub> = -100 μA	A port	V <sub>CC</sub> -0.2	V <sub>CC</sub>		V	
			V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -32 mA		2.0	2.3			
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 100 μA	A port		0.07	0.2	V	
			V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA			0.25	0.4		
			V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 32 mA			0.3	0.5		
			V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 64 mA			0.4	0.55		
			V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 40 mA	B port		0.4	0.5	V	
I <sub>I</sub>	Input leakage current		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins		0.1	±1	μA	
			V <sub>CC</sub> = 0 or 3.6 V; V <sub>I</sub> = 5.5 V			0.1	10		
			V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V	I/O Data pins <sup>4</sup> A port		0.1	20	μA	
			V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub>			0.5	10		
			V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0			0.1	-5		
			V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>TT</sub> or GND	B port			±5	μA	
I <sub>OFF</sub>	Output off current		V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5 V			0.1	±100	μA	
I <sub>HOLD</sub>	Bus Hold current, A outputs		V <sub>CC</sub> = 3 V; V <sub>I</sub> = 0.8 V		75	130		μA	
			V <sub>CC</sub> = 3 V; V <sub>I</sub> = 2.0 V		-75	-140			
I <sub>EX</sub>	Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub>		V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 3.0 V	A port		10	125	μA	
I <sub>PU/PD</sub>	Power up/down 3-State output current <sup>3</sup>		V <sub>CC</sub> ≤ 1.2 V; V <sub>O</sub> = 0.5 V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> OE = Don't care			1.0	±100	μA	
I <sub>CCH</sub>	A-Port	V <sub>CC</sub> = 3.6 V	Outputs high		V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		5.0	9.0	mA
I <sub>CCL</sub>			Outputs low				10.5	18.5	
I <sub>CCZ</sub> <sup>5</sup>	Disabled			6.0		11.5			
I <sub>CCH</sub>	B-Port		Outputs high				9.7	17.5	
I <sub>CCL</sub>			Outputs low				7.0	12.0	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>		V <sub>CC</sub> = 3 V to 3.6 V; One input at V <sub>CC</sub> -0.6 V, Other inputs at V <sub>CC</sub> or GND			0.04	0.2	mA	

### NOTES:

1. All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
2. This is the increase in supply current for each LVTTTL input at the specified voltage level other than V<sub>CC</sub> or GND.
3. This parameter is valid for any V<sub>CC</sub> between 0 V and 1.2 V with a transition time of up to 10 msec. From V<sub>CC</sub> = 1.2 V to V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V a transition time of 100  $\mu$ sec is permitted. This parameter is valid for T<sub>amb</sub> = 25°C only.
4. Unused pins at V<sub>CC</sub> or GND.
5. I<sub>CCZ</sub> is measured with outputs pulled up to V<sub>CC</sub> or pulled down to ground.

# 18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

## AC CHARACTERISTICS (A PORT)

GND = 0 V;  $t_r = t_f = 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ ;  $T_{amb} = -40$  to  $+85$  °C.

GTL16612 An Port			GTL			GTL+			UNIT
			V <sub>CC</sub> = 3.3 V ±0.3 V			V <sub>CC</sub> = 3.3 V ±0.3 V			
			V <sub>REF</sub> = 0.8 V			V <sub>REF</sub> = 1.0 V			
SYMBOL	PARAMETER	WAVEFORM	MIN	TYP <sup>1</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	
t <sub>PLH</sub>	Bn to An	2	1.6	3.0	5.0	1.6	3.0	5.0	ns
t <sub>PHL</sub>	Bn to An	2	3.0	4.9	6.3	3.0	4.9	6.3	ns
t <sub>PLH</sub>	LEBA to An	3	1.6	2.7	4.2	1.6	2.7	4.2	ns
t <sub>PHL</sub>	LEBA to An	3	1.6	2.8	4.3	1.6	2.8	4.3	ns
t <sub>PLH</sub>	CPBA to An	1	1.9	3.4	4.7	1.9	3.4	4.7	ns
t <sub>PHL</sub>	CPBA to An	1	1.8	3.8	5.2	1.8	3.8	5.2	ns
t <sub>PZH</sub>	OEBA̅ to An	5	1.5	2.6	4.2	1.5	2.6	4.2	ns
t <sub>PHZ</sub>	OEBA̅ to An	5	1.4	2.9	4.8	1.4	2.9	4.8	ns
t <sub>PZL</sub>	OEBA̅ to An	6	1.3	2.4	3.8	1.3	2.4	3.8	ns
t <sub>PLZ</sub>	OEBA̅ to An	6	1.2	2.2	3.5	1.2	2.2	3.5	ns

### NOTE:

1. Typical values are at  $V_{CC} = 3.3$  V,  $T_{amb} = +25$  °C.

## AC CHARACTERISTICS (B PORT)

GND = 0 V;  $t_r = t_f = 2.5$  ns;  $C_L = 30$  pF;  $R_L = 25$   $\Omega$ ;  $T_{amb} = -40$  to  $+85$  °C.

GTL16612 Bn Port			GTL			GTL+			UNIT
			V <sub>CC</sub> = 3.3 V ±0.3 V			V <sub>CC</sub> = 3.3 V ±0.3 V			
			V <sub>REF</sub> = 0.8 V			V <sub>REF</sub> = 1.0 V			
SYMBOL	PARAMETER	WAVEFORM	MIN	TYP <sup>1</sup>	MAX	MIN	TYP <sup>1</sup>	MAX	
t <sub>PLH</sub>	An to Bn	2	1.4	2.4	3.7	1.3	2.4	3.7	ns
t <sub>PHL</sub>	An to Bn	2	1.3	2.5	4.0	1.4	2.6	4.2	ns
t <sub>PLH</sub>	LEAB to Bn	3	1.7	3.0	4.4	1.8	3.0	4.6	ns
t <sub>PHL</sub>	LEAB to Bn	3	2.1	3.5	5.4	2.3	3.6	5.5	ns
t <sub>PLH</sub>	CPAB to Bn	1	1.8	3.1	4.5	1.9	3.1	4.8	ns
t <sub>PHL</sub>	CPAB to Bn	1	2.3	3.6	5.4	2.4	3.8	5.8	ns
t <sub>PLH</sub>	$\overline{OEAB}$ to Bn	7	1.1	2.1	3.3	1.4	2.0	3.5	ns
t <sub>PHL</sub>	$\overline{OEAB}$ to Bn	7	1.6	2.8	4.4	1.0	2.9	4.5	ns

### NOTE:

1. Typical values are at  $V_{CC} = 3.3$  V,  $T_{amb} = +25$  °C.

# 18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

## AC SETUP REQUIREMENTS (3.3 V $\pm$ 0.3 V RANGE)

A Port: GND = 0 V; Input  $t_r = t_f = 2.5$  ns;  $C_L = 50$  pF;  $R_L = 500$   $\Omega$ ;  $T_{amb} = -40$  to  $+85$  °C;  $V_{REF} = 0.8$  V or 1.0 V.

B Port: GND = 0 V; Input  $t_r = t_f = 2.5$  ns;  $C_L = 30$  pF;  $R_L = 25$   $\Omega$ ;  $V_{REF} = 0.8$  V or 1.0 V.

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		
			MIN	MAX	
$t_s(H)$	Setup time, High or Low Bn to CPBA	4	1.5		ns
$t_s(L)$		4	1.5		ns
$t_s(H)$	Setup time, High or Low An to CPAB	4	2.0		ns
$t_s(L)$		4	3.0		ns
$t_h(H)$	Hold time, High or Low Bn to CPBA, or An to CPAB	4	1.0		ns
$t_h(L)$		4	1.0		ns
$t_s(H)$	Setup time, High or Low Bn to LEBA, or An to LEAB	4	1.0		ns
$t_s(L)$		4	1.0		ns
$t_h(H)$	Hold time, High or Low Bn to LEBA, or An to LEAB	4	1.5		ns
$t_h(L)$		4	1.5		ns
$t_s(H)$	Setup time, High or Low $\overline{CEAB}$ to CPAB, or $\overline{CEBA}$ to CPBA	4	1.0		ns
$t_s(L)$		4	1.0		ns
$t_h(H)$	Hold time, High or Low $\overline{CEAB}$ to CPAB, or $\overline{CEBA}$ to CPBA	4	1.5		ns
$t_h(L)$		4	1.0		ns
$t_w(H)$	Pulse width, High or Low CPBA or CPAB	4	2.0		ns
$t_w(L)$		4	2.0		ns
$t_w(H)$	Pulse width, High LEBA or LEAB	3	1.5		ns



# 18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL bidirectional universal translator (3-State)

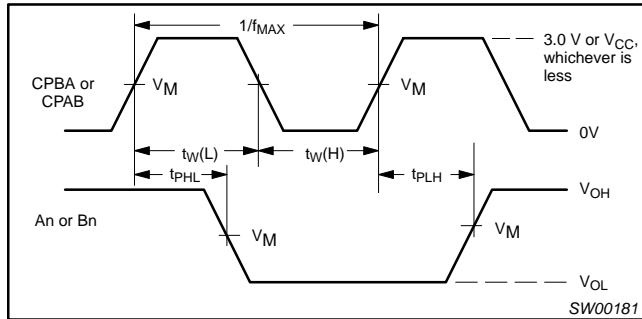
GTL16612

## AC WAVEFORMS

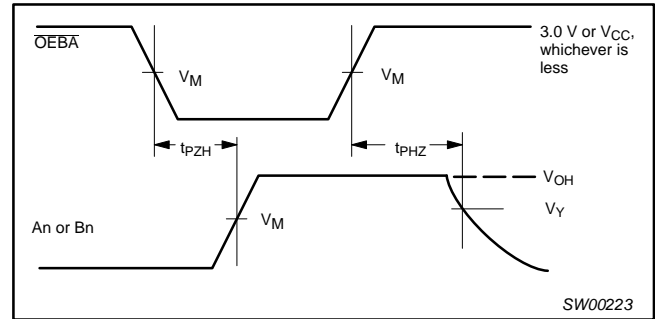
$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 3.0\text{ V}$ .  $V_M = 1.5\text{ V}$  for A ports and control pins;  $V_M = 0.8\text{ V}$  for B ports in GTL mode;  $V_M = 1.0\text{ V}$  for B ports in GTL+ mode.

$V_X = V_{OL} + 0.3\text{ V}$  at  $V_{CC} \geq 3.0\text{ V}$ .

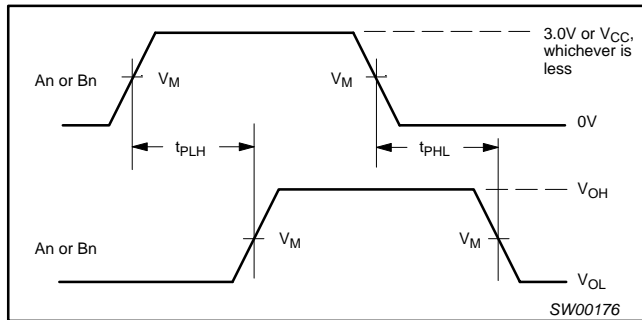
$V_Y = V_{OH} - 0.3\text{ V}$  at  $V_{CC} \geq 3.0\text{ V}$ .



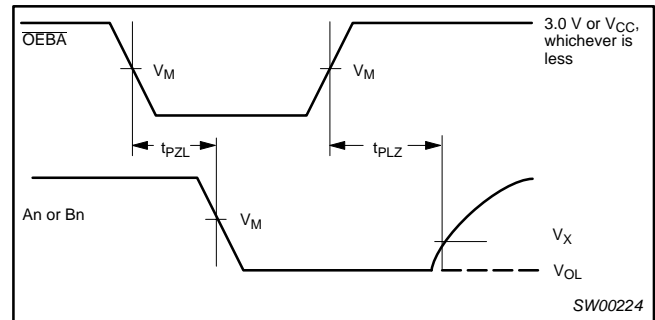
**Waveform 1.** Propagation delay, clock input to output, clock pulse width, and maximum clock frequency



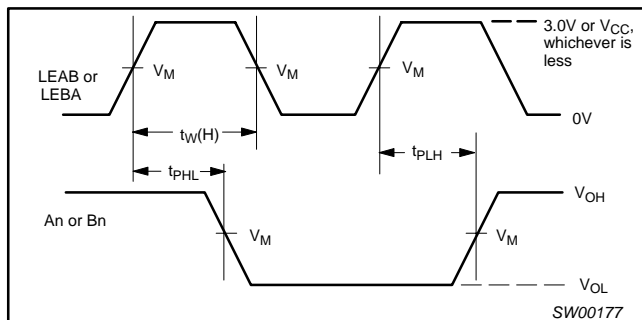
**Waveform 5.** 3-State output enable time to high level and output disable time from high level



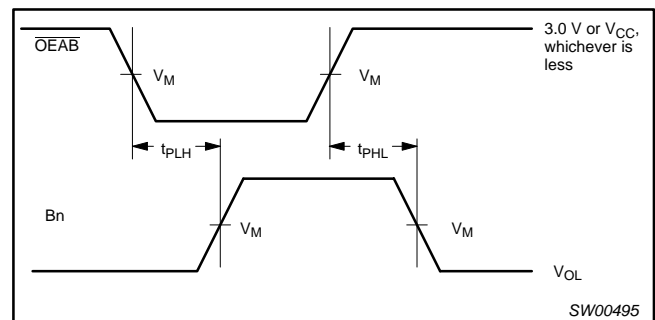
**Waveform 2.** Propagation delay, transparent mode



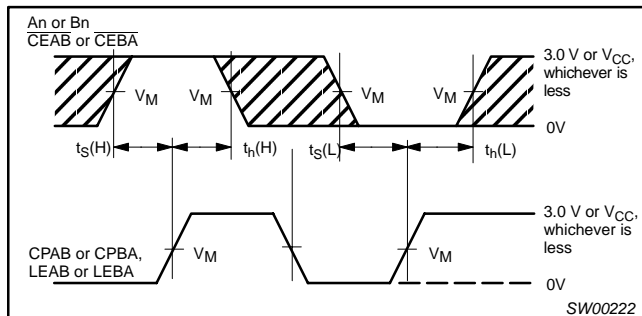
**Waveform 6.** 3-State output enable time to low level and output disable time from low level



**Waveform 3.** Propagation delay, enable to output, and enable pulse width



**Waveform 7.** Output enable time on open collector output with pullup

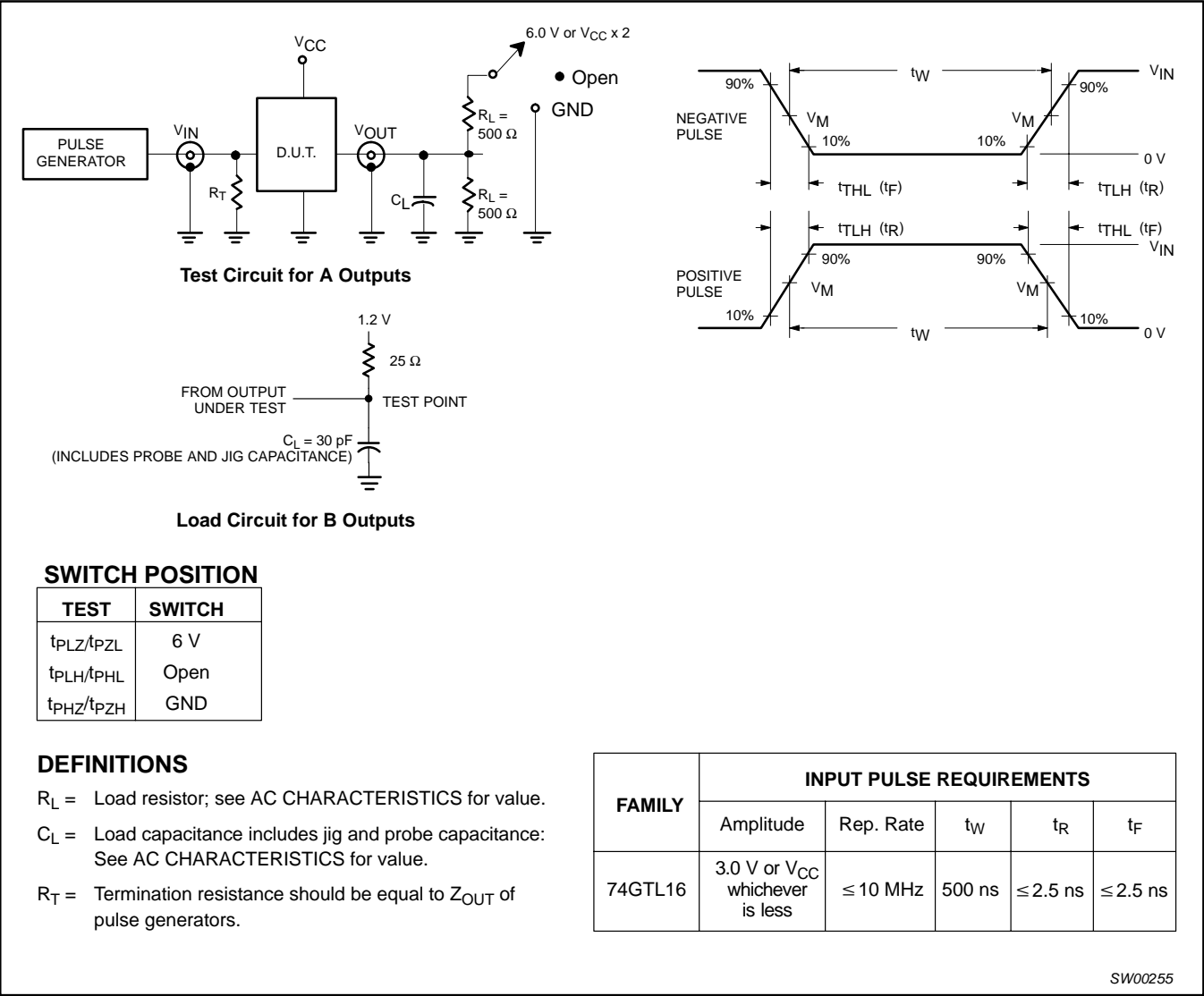


**Waveform 4.** Data setup and hold times

18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

TEST CIRCUIT

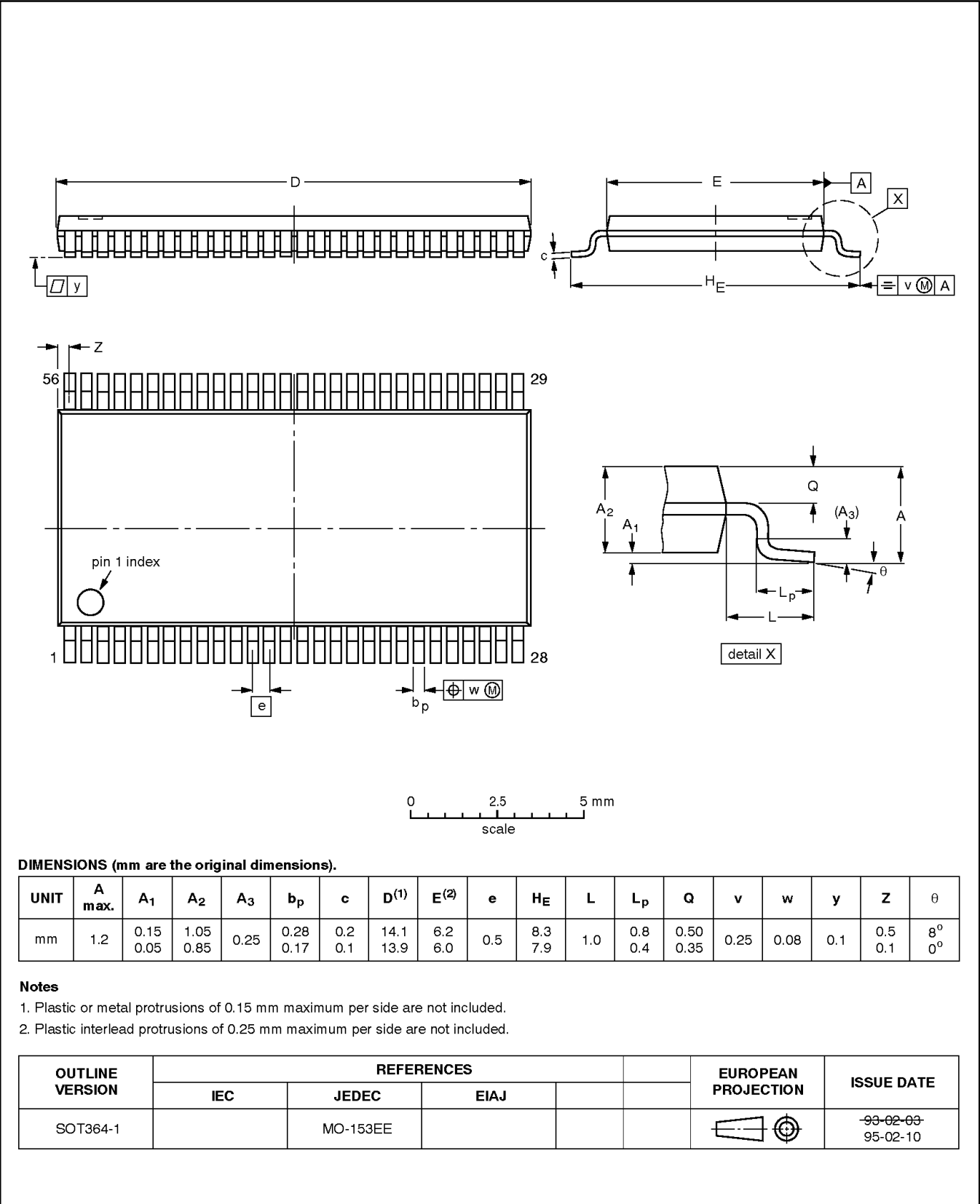


18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL bidirectional universal translator (3-State)

GTL16612

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



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**18-bit GTL/GTL<sup>+</sup> to LVTTTL/TTL bidirectional  
universal translator (3-State)**

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**GTL16612****REVISION HISTORY**

Rev	Date	Description
_4	20021213	Product data (9397 750 10862); ECN 853-2166 29245 of 03 December 2002 Modifications: <ul style="list-style-type: none"><li>• New package release.</li></ul>
_3	20000619	Product data (9397 750 07217); ECN 853-2166 23903 of 19 June 2000.

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GTL16612

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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