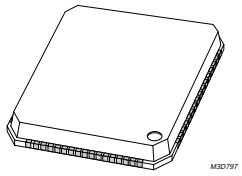


PIP201-12M

DC to DC converter powertrain

Rev. 01 — 24 January 2002 **Preliminary data**

1. Description

The PIP201-12M is designed for use as the power output stage of a synchronous buck DC to DC converter. It contains a MOSFET control IC and two power MOSFET transistors. By combining the power MOSFETs and the driver circuit into a single component, stray inductances are virtually eliminated, resulting in higher switching frequency, lower switching losses and a compact, efficient design.

2. Features

- Optimized for conversion from 12 V
- Output current up to 20 A
- Operating frequency up to 1 MHz
- High efficiency
- Low-profile, surface mount package ($10 \times 10 \times 0.85$ mm)
- Compatible with any single or multi-phase PWM controller.

3. Applications

- Microprocessor voltage regulators
- Memory voltage regulators
- Low-voltage, high-current DC to DC converters.

4. Ordering information

Table 1: Ordering information

Type number	Package		
	Name	Description	Version
PIP201-12M	MLF68	plastic, heatsink very thin quad flat package; no leads; 68 terminals; body $10 \times 10 \times 0.85$ mm	SOT687

PHILIPS

5. Block diagram

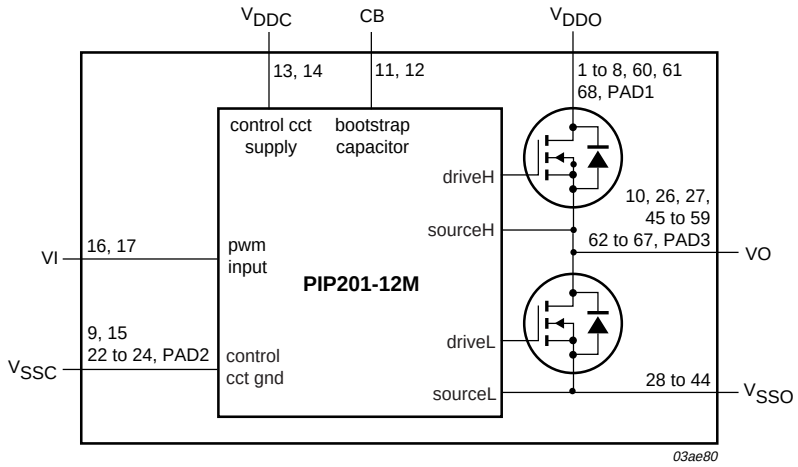


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

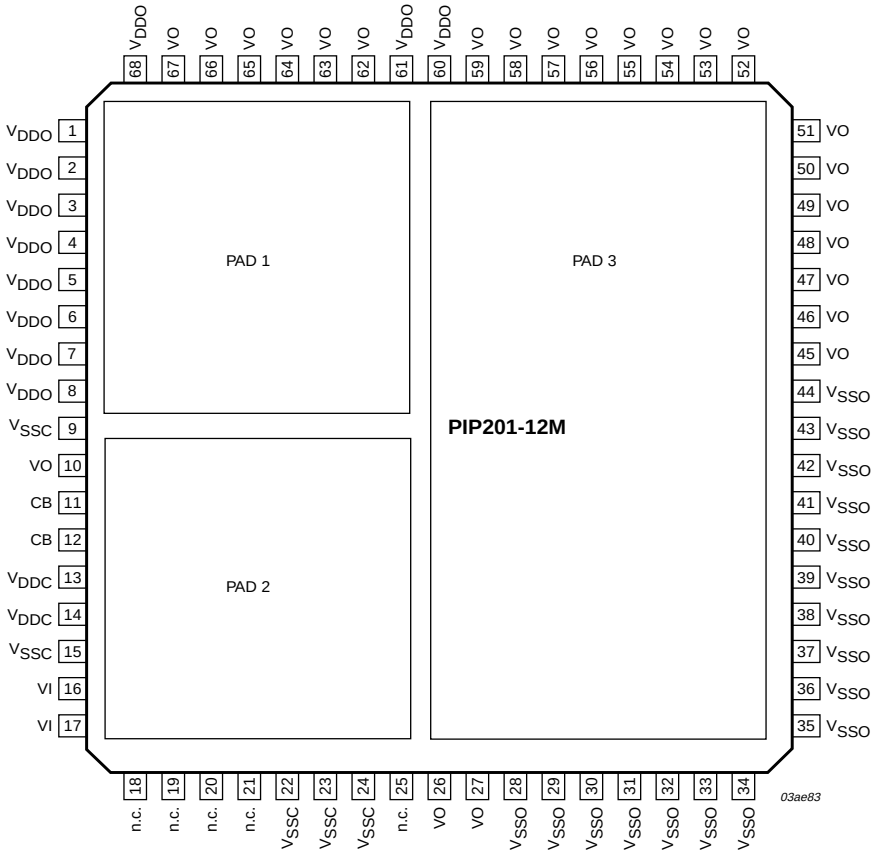


Fig 2. Pin configuration (Top view).

6.2 Pin description

Table 2: Pin description

Symbol	Pin		I/O	Description
V_{DDO}	1 to 8, 60, 61, 68	[1]	–	output stage supply voltage
V_{SSC}	9, 15, 22 to 24	[2]	–	control circuit supply ground
VO	10, 26, 27, 45 to 59, 62 to 67	[3]	O	output
CB	11, 12		I/O	bootstrap capacitor connection
V_{DDC}	13, 14		–	control circuit supply voltage

Table 2: Pin description...*continued*

Symbol	Pin	I/O	Description
VI	16, 17	I	pulse width modulated input
n.c.	18 to 21, 25	–	not connected
V_{SSO}	28 to 44	–	output stage supply ground

[1] All pins connected to PAD1
[2] All pins connected to PAD2
[3] All pins connected to PAD3.

7. Functional description

7.1 Application requirements

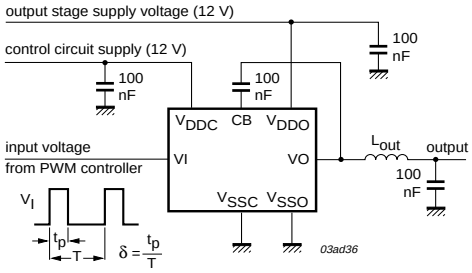


Fig 3. Simplified functional block diagram of a synchronous DC-DC converter output stage.

In order to understand the functions performed by the PIP201-12M, consider the requirements of a synchronous DC to DC converter output stage, driven from a PWM controller (Figure 3).

When the input voltage is HIGH, the upper MOSFET must be on and the lower MOSFET must be off. Current flows from the supply (V_{DDO}), through the upper MOSFET and the inductor (L_{out}), to the output.

When the input voltage is LOW and current is flowing in the inductor, the upper MOSFET must be off and the lower MOSFET must be on. Current flows from the power ground (V_{SSO}), through the lower MOSFET and the inductor (L_{out}), to the output.

Finally, when switching between states, both MOSFETs must not be on at the same time.

7.2 MOSFET driver function

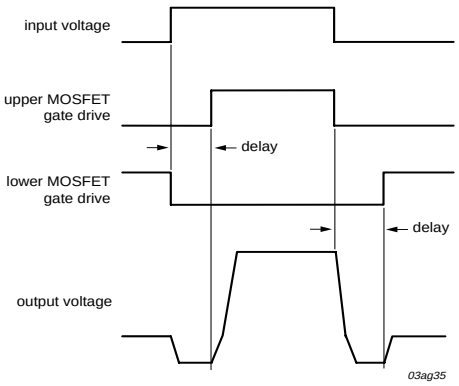


Fig 4. Input, output and gate drive waveforms of a synchronous DC-DC converter output stage.

The input, output and gate drive waveforms are shown in Figure 4. When the input voltage goes HIGH, the gate drive to the lower MOSFET immediately goes LOW. This causes the output current to flow through the source-drain diode of the lower MOSFET. This causes output voltage to fall from zero to approximately –0.7 V.

After a delay, if the input voltage is still HIGH, the gate drive to the upper MOSFET goes HIGH. This causes the output voltage to rise to the output stage supply voltage, V_{DDO}.

When the input voltage goes LOW, the gate drive to the upper MOSFET immediately goes LOW. The output voltage falls from V_{DDO}, until it is clamped by the source-drain diode of the synchronous FET at approximately –0.7 V.

After a delay, if the input voltage is still LOW, the gate drive to the lower MOSFET goes HIGH. The lower MOSFET turns on, and the output voltage rises from –0.7 V to zero.

7.3 Three-state function

If the input voltage remains between the upper and lower switching thresholds for longer than 144 ns (typical), both MOSFETs are turned off. This prevents the output capacitor bank from discharging through the lower MOSFET.

8. Limiting values

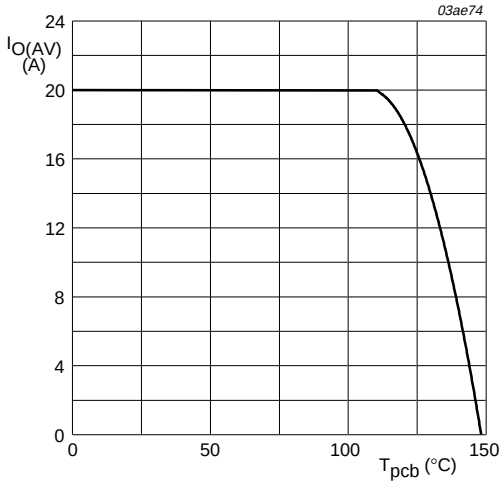
Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDC}	control circuit supply voltage			–0.5	13	V
V_{DDO}	output stage supply voltage			–0.5	25	V
V_I	input voltage			–0.5	5.25	V
V_O	output voltage			–0.5	V_{DDO} + 0.5	V
V_{CB}	bootstrap voltage			–0.5	V_O + 13	V
$I_{O(AV)}$	average output current	V_{DDC} = 12 V; $T_{pcb} \leq$ 112 °C; Figure 5		-	20	A
I_{ORM}	repetitive peak output current	V_{DDC} = 12 V; $t_p \leq$ 10 µs	[1]	-	200	A
P_{tot}	total power dissipation	T_{pcb} = 25 °C	[2]	-	25	W
		T_{pcb} = 90 °C	[2]	-	12	W
T_{stg}	storage temperature			–55	+150	°C
T_j	operating junction temperature			–55	+150	°C

[1] Pulse width and repetition rate limited by maximum value of T_j.

[2] Assumes a thermal resistance from junction to printed-circuit board of 5 K/W.



V_{DDC} = 12 V; V_{DDO} = 12 V; f_i = 500 kHz; V_O = 1.6 V.

Fig 5. Average output current as a function of printed-circuit board temperature.

9. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}pcb)}$	thermal resistance from junction to printed-circuit board		-	4	5	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	device mounted on FR4 printed-circuit board; copper area around device 25 × 25 mm				
		no thermal vias	-	25	-	K/W
		with thermal vias	-	20	-	K/W

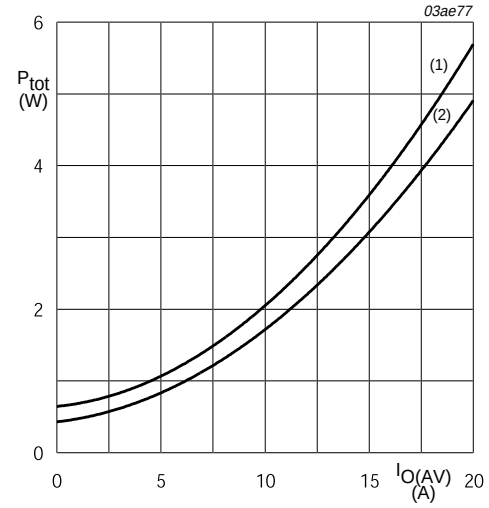
10. Characteristics

Table 5: Characteristics

V_{DDC} = 12 V; T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V_{IH}	HIGH-level input voltage	25 °C ≤ T_j ≤ 150 °C	[1]	2.55	2.8	3.05	V
V_{IL}	LOW-level input voltage	25 °C ≤ T_j ≤ 150 °C	[1]	1.95	2.1	2.25	V
I_{LI}	input leakage current	0 V ≤ V_I ≤ V_{DDC}		-	10	100	nA
I_{DDC}	control circuit supply current	f_i = 0 Hz		-	1.5	3	mA
		f_i = 500 kHz; Figure 10		-	45	60	mA
P_{tot}	total power dissipation	V_{DDO} = 12 V; $I_{O(AV)}$ = 12.5 A; f_i = 500 kHz; V_O = 1.6 V; T_{pcb} = 90 °C; Figure 6.		-	2.7	-	W
Dynamic characteristics							
$t_{d(on)(IH-OH)}$	turn-on delay time input HIGH to output HIGH	V_{DDO} = 12 V; $I_{O(AV)}$ = 12.5 A		-	77	85	ns
$t_{d(off)(IL-OL)}$	turn-off delay time input LOW to output LOW			-	30	45	ns
$t_{o(r)}$	output rise time			-	18	25	ns
$t_{o(f)}$	output fall time			-	12	20	ns
$t_{d(3\text{-state})}$	3-state enable delay time			115	144	173	ns

[1] If the input voltage remains between V_{IH} and V_{IL} (2.5 V typ) for longer than $t_{d(3\text{-state})}$, then both MOSFETs are turned off.

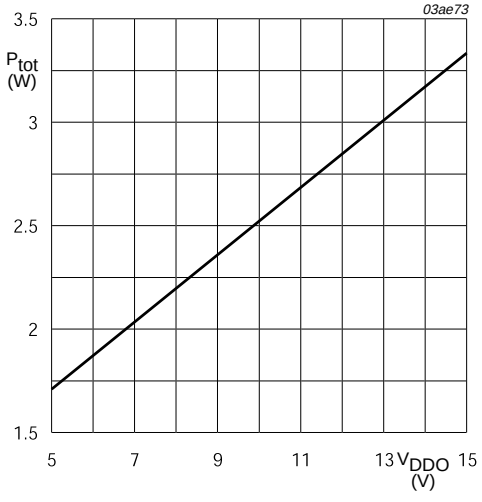


V_{DDC} = 12 V; V_{DDO} = 12 V; V_O = 1.6 V

(1) f_i = 500 kHz

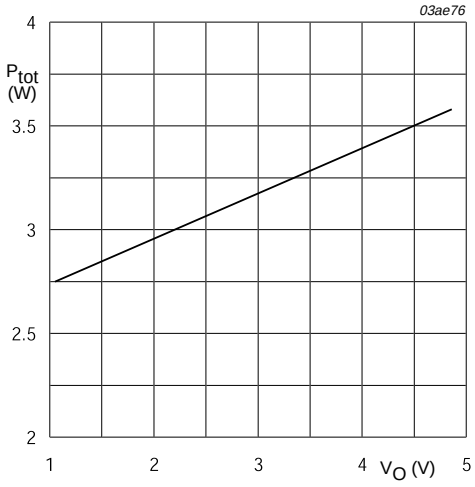
(2) f_i = 250 kHz.

Fig 6. Total power dissipation as a function of average output current; typical values.



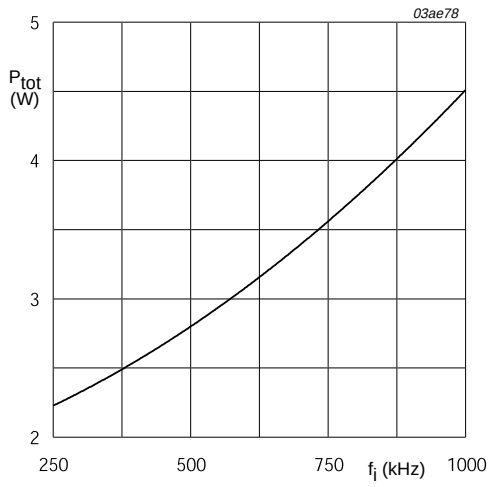
V_{DDC} = 12 V; V_O = 1.6 V; f_i = 500 kHz; $I_{O(AV)}$ = 12.5 A.

Fig 7. Total power dissipation as a function of output stage supply voltage; typical values.



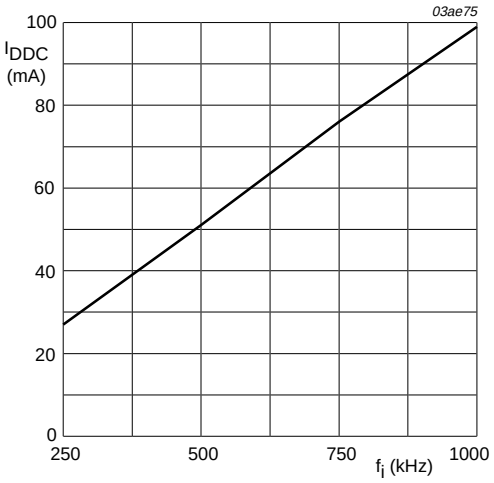
V_{DDC} = 12 V; V_{DDO} = 12 V; f_i = 500kHz; $I_{O(AV)}$ = 12.5 A.

Fig 8. Total power dissipation as a function of output voltage; typical values.



V_{DDC} = 12 V; V_{DDO} = 12 V; V_O = 1.6V; $I_{O(AV)}$ = 12.5 A.

Fig 9. Total power dissipation as a function of input frequency; typical values.



V_{DDC} = 12 V; V_{DDO} = 12 V; V_O = 1.6 V; $I_{O(AV)}$ = 12.5 A; f_i = 500 kHz.

Fig 10. Control circuit supply current as a function of input frequency; typical values.

11. Application information

11.1 Typical application

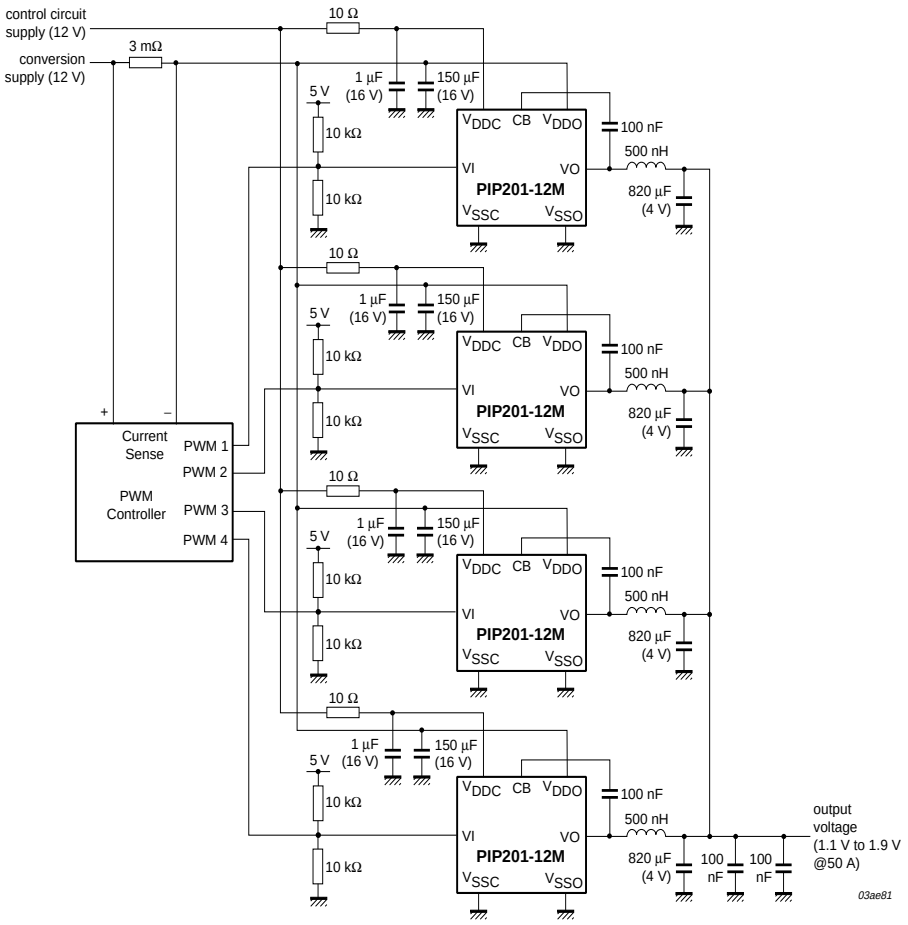


Fig 11. Typical application circuit using the PIP201-12M in a four-phase converter.

A typical four-phase buck converter is shown in Figure 11. This system uses four PIP201-12M devices to deliver a continuous output current of 50 A at an operating frequency of 500 kHz.

The dissipation in each PIP201-12M can be read from Figure 6. At 500 KHz and 12.5 A output current, the dissipation in each PIP201-12M is 2.7 W. In a typical computer motherboard application, the thermal resistance of each PIP201-12M from junction to ambient is 20 K/W. Assuming a maximum ambient temperature of 55 °C, the maximum junction temperature ($T_{j(max)}$) is given by:

$$T_{j(max)} = P_{tot} \times R_{th(j-a)} + T_{amb} = 2.7 \times 20 + 55 = 109°C \quad (1)$$

The thermal resistance between the junction and the printed-circuit board is 5 K/W. Therefore, the maximum printed-circuit board temperature ($T_{pcb(max)}$) is given by:

$$T_{pcb(max)} = T_{j(max)} - P_{tot} \times R_{th(j-pcb)} = 127 - 2.7 \times 5 = 95.5°C \quad (2)$$

11.2 Advantages of an integrated driver

One problem in the design of low-voltage, high-current DC to DC converters using discrete components, is stray inductance between the various circuit elements.

Stray inductance in the gate drive circuit increases the switching times of the MOSFETs and causes high-frequency oscillation of the gate voltage.

Stray inductance in the high-current loop between V_{DDO} and V_{SSO} causes switching losses and electromagnetic interference. In discrete designs, high-frequency electric and magnetic fields radiate from PCB tracks and couple into adjacent circuits.

By integrating the power MOSFETs and their drive circuits into a single package, stray inductance is virtually eliminated, resulting in a compact, efficient design.

In discrete designs, the delays in the MOSFET drivers must be long enough to ensure no cross-conduction even when using the slowest MOSFETs. Use of an integrated driver allows the propagation delays in the MOSFET drivers to be precisely matched to the MOSFETs. This minimizes switching losses and eliminates cross-conduction whilst allowing the circuit to operate at a higher frequency.

11.3 Switching frequency

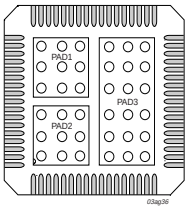
A high operating frequency reduces the size and number of capacitors needed to filter the output current, and also reduces the size of the output inductors. The disadvantage is higher dissipation due to switching and MOSFET driver losses. For example, doubling the operating frequency of the circuit in Figure 11 from 500 kHz to 1 MHz would increase the power dissipation in each PIP201-12M from 2.7 W to 4.5 W, at an output current of 12.5 A in each PIP201-12M.

The maximum switching frequency is limited by thermal considerations, the dissipation in the four PIP201-12M devices and the thermal resistance from junction to ambient.

11.4 Thermal design

The PIP201-12M has three pads on its underside. These are designated PAD1, PAD2 and PAD3 (Figure 2). PAD1 is connected to V_{DDO}, PAD2 is connected to V_{SSC} and PAD3 is connected to VO. In addition to providing low inductance electrical connections, these pads conduct heat away efficiently from the MOSFETs and control IC to the printed-circuit board. The thermal resistance from junction to printed-circuit board is approximately 5 K/W. In order to take full advantage of the low thermal resistance of this package, the printed-circuit board must be designed so that heat is conducted away efficiently from the package. This can be achieved by maximizing the area of copper around each pad, and by incorporating thermal vias to conduct the heat to inner and/or bottom layers of the printed-circuit board. An example of a thermal via pattern is shown in Figure 12. In a typical computer

motherboard application, with no forced air cooling, the use of thermal via holes typically reduces the thermal resistance from 25 K/W to 20 K/W. The additional use of a small fan can reduce this further to approximately 15 K/W.



All holes 0.5 mm diameter, 1 mm spacing.

Fig 12. Printed-circuit board thermal via pattern.

The thermal resistance of a particular design can be measured by passing a known current through the source-drain diode of the lower MOSFET. The direction of current flow is into V_{SSO} and out of VO. The volt drop between V_{SSO} and VO is then measured and used to calculate the power dissipation in the PIP201-12M. The case temperature of the PIP201-12M can be measured using an infra-red thermometer. The thermal resistance can then be calculated using the following equation:

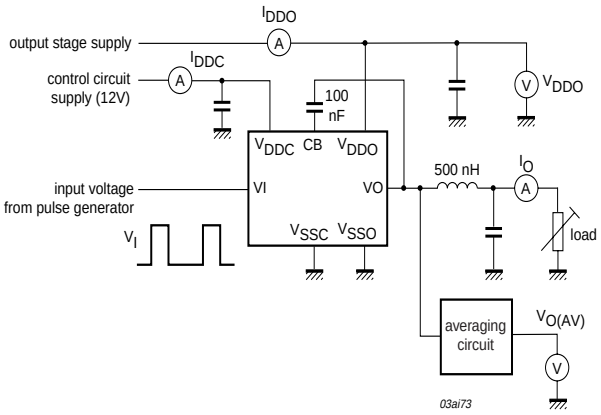
$$R_{th(j-pcb)} = \frac{T_{case} - T_{amb}}{I \times V_F} \quad (3)$$

where T_{case} is the measured case temperature, T_{amb} is the ambient temperature, I is the MOSFET current and V_F is the volt drop between V_{SSO} and VO.

In a multi-phase design, the thermal resistance of each PIP201-12M should be measured with current flowing in all phases.

12. Test information

Figure 13 shows the test circuit used to measure power loss in the PIP201-12M. The output voltage is measured using an averaging circuit. This eliminates losses in the output inductor and the pcb tracks. The calculated power loss, using this method, includes the losses in the ESR of the input filter capacitors. This must be subtracted from the total loss to give the net loss in the PIP201-12M.



$$P_{DDO} = V_{DDO} \times I_{DDO}$$

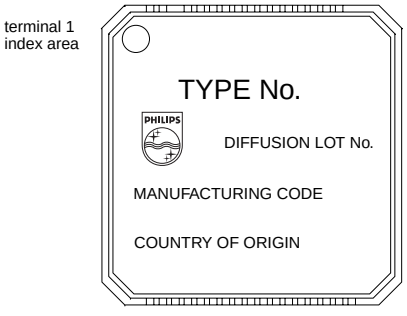
$$P_{DDC} = V_{DDC} \times I_{DDC}$$

$$P_O = V_{O(AV)} \times I_O$$

$$P_{tot} = P_{DDO} + P_{DDC} - P_O$$

Fig 13. Power loss (P_{tot}) test circuit.

13. Marking



TYPE No: PIP201-12M

DIFFUSION LOT No: 7 characters

MANUFACTURING CODE: see Figure 15

COUNTRY OF ORIGIN: Korea

Fig 14. SOT687 marking.

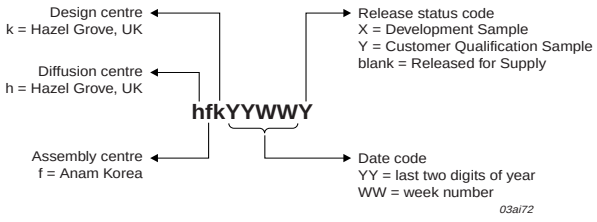
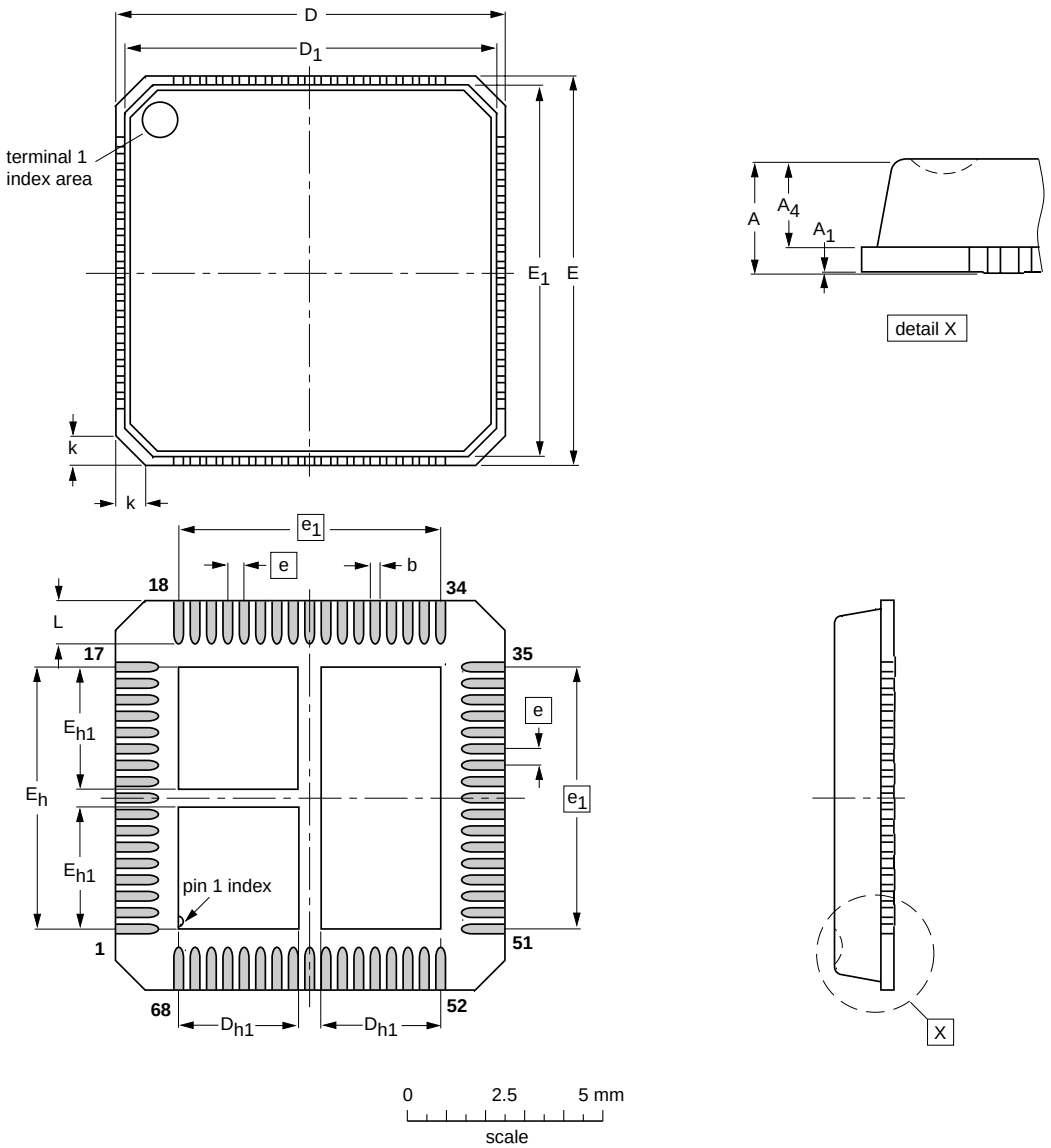


Fig 15. Interpretation of manufacturing code.

14. Package outline

HVQFN68: plastic, heatsink very thin quad flat package; no leads; 68 terminals; body 10 x 10 x 0.85 mm **SOT687**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_4	b	D	D_1	D_{h1}	E	E_1	E_h	E_{h1}	e	e_1	k	L
mm	1.0	0.05 0	0.80 0.65	0.30 0.18	10.15 9.85	9.75	3.8 3.5	10.15 9.85	9.75	7.85 7.55	3.8 3.5	0.50	8.0	0.60 0.24	0.75 0.50

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT687						01-12-04

Fig 16. SOT687; plastic, heatsink, very thin quad flat package; no leads; 68 terminals; body 10 × 10 × 0.85 mm.

15. Soldering

15.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C small/thin packages.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15.5 Package related soldering information

Table 6: Suitability of surface mount IC packages for wave and reflow soldering methods

Package	Soldering method	
	Wave	Reflow[1]
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

[1] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[2] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[3] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[4] Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

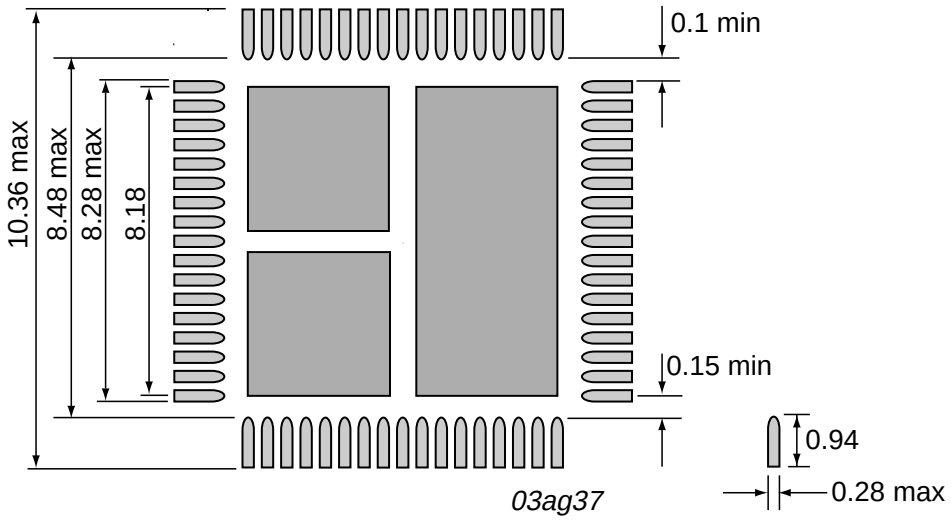
[5] Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

16. Mounting

As shown in Figure 16, the terminals on the underside of the package are rectangular in shape with a rounded edge on the inside. Electrical connection between the package and the printed-circuit board is made by printing solder paste onto the PCB footprint followed by component placement and reflow soldering. The PCB footprint shown in Figure 17 is designed to form reliable solder joints.

In addition to the dimensions shown, a gap of at least 0.1 mm is recommended between each of the metal pads on the underside of the package, and also between the metal pads and the edge terminations. These clearances may need to be increased to prevent solder bridging. The use of solder resist between each pad is recommended.

Good surface flatness of the PCB footprint is desirable to ensure accuracy of placement after soldering. Printed-circuit boards that are finished with a roller tin process tend to leave small lumps of tin in the corners of each land. Levelling with a hot air knife improves flatness. Alternatively, an electro-less silver or silver immersion process produces completely flat PCB pads.



All dimensions in mm.

Fig 17. PCB footprint for SOT687 package (reflow soldering).

17. Revision history

Table 7: Revision history

Rev	Date	CPCN	Description
01	20020124	-	Preliminary data (9397 750 09032); initial version.

18. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

19. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

20. Disclaimers

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