DATA SHEET

TEA6843HL
New In Car Entertainment (NICE) extended car radio

Product specification

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Philips
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PHILIPS

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New In Car Entertainment (NICE) extended car radio

TEA6843HL

1 FEATURES

- FM mixer for conversion of FM RF from 65 to 108 MHz to IF of 10.7 MHz; the mixer provides inherent image rejection
- FM RF mixer can be set to receive weather band radio up to 162.55 MHz
- Buffer output for weather band flag
- AM mixer 1 for conversion of AM RF to AM IF1 of 10.7 MHz
- LC tuner oscillator providing mixer frequencies for FM mixer and AM mixer 1
- AM mixer 2 for conversion of AM IF1 to AM IF2 of 450 kHz
- Crystal oscillator providing mixer frequencies for AM mixer 2 and reference for synthesizer PLL, IF count, timing for inaudible Radio Data System (RDS) update and reference frequency for car audio signal processor ICs
- Fast synthesizer PLL tuning system with local control for inaudible RDS updating
- Timing function for RDS update algorithm and control signal output for car audio signal processor ICs (TEA688x, SAA77xx) or car radio integrated signal processor IC (TEF689x)
- Digital auto alignment circuit for conversion of LC oscillator tuning voltage to controlled alignment voltage of FM antenna tank circuit
- AGC PIN diode drive circuit for FM RF AGC; AGC detection at FM mixer input; the AGC PIN diode current can be set to a fixed value to allow local function for search tuning; AGC threshold is a programmable and keyed function switchable via the I^2C-bus
- FM IF linear amplifiers with high dynamic input range
- FM quadrature demodulator with automatic centre frequency adjustment and Total Harmonic Distortion (THD) compensation and level driven soft mute; soft mute characteristic is adjustable via the I^2C-bus
- Level detector for AM and FM with temperature compensated output voltage; starting point and slope of level output is programmable via the I^2C-bus
- AM RF PIN diode drive circuit; AGC threshold detection at AM mixer 1 and IF2 AGC input; threshold is programmable via the I^2C-bus; AM IF2 AGC and demodulator
- AM AF output switchable to provide AM IF2 for AM stereo decoder
- AM noise blanker with blanking at AM IF2
- Several test modes available for fast IC and system tests.

2 GENERAL DESCRIPTION

The TEA6843HL is a single IC with car radio tuner for AM, FM and Weather Band (WB) intended for microcontroller tuning with the I^2C-bus. It provides the following functions:

- AM double conversion receiver for LW, MW and SW (31 m, 41 m and 49 m bands) with IF1 = 10.7 MHz and IF2 = 450 kHz
- FM single conversion receiver with integrated image rejection for IF = 10.7 MHz capable of selecting US FM, US weather, Europe FM, East Europe FM and Japan FM bands
- The tuning system includes FM mixer, AM mixer 1, AM mixer 2, crystal oscillator, VCO and PLL synthesizer on one chip.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA6843HL	LQFP80	plastic low profile quad flat package; 80 leads; body $12 \times 12 \times 1.4$ mm	SOT315-1

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DDA(n)}$	analog supply voltage 1 to 4 and 6		8	8.5	9	V
$I_{DDA(tot)}$	total analog supply currents 1 to 4 and 6 and mixer bias currents	FM mode; data byte 5: bit TMS3 = 1	45	60	69	mA
		AM mode; data byte 5: bit TMS3 = 1	39	50	59	mA
V_{DDA5}	analog supply voltage 5		4.75	5	5.25	V
I_{DDA5}	analog supply current 5	FM mode; data byte 5: bit 5 = 0, bit 6 = 0	6.5	9.3	11.2	mA
		AM mode; data byte 5: bit 5 = 1, bit 6 = 1	12.7	17.4	22.1	mA
V_{DDD}	digital supply voltage		4.75	5	5.25	V
I_{DDD}	digital supply current	FM mode	18	23	28	mA
		AM mode	18	23	28	mA
$f_{AM(ant)}$	AM input frequency	LW	0.144	–	0.288	MHz
		MW	0.522	–	1.710	MHz
		SW	5.85	–	9.99	MHz
$f_{FM(ant)}$	FM input frequency		65	–	108	MHz
$f_{FM(WB)(ant)}$	FM weather band input frequency		162.4	–	162.55	MHz
T_{amb}	ambient temperature		–40	–	+85	°C

5 BLOCK DIAGRAM

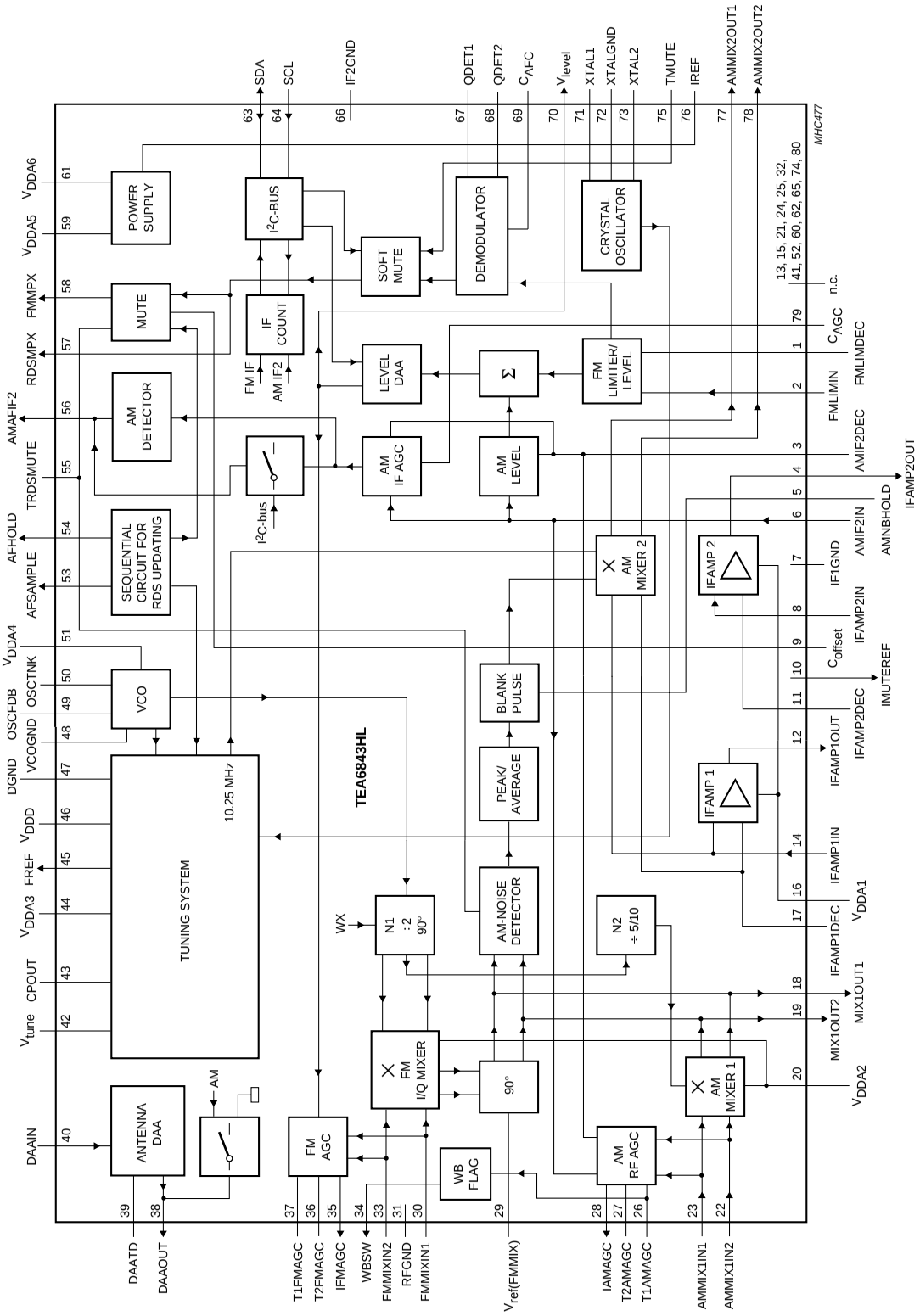


Fig.1 Block diagram

6 PINNING

SYMBOL	PIN	DESCRIPTION
FMLIMDEC	1	FM limiter decoupling
FMLIMIN	2	FM limiter input (10.7 MHz)
AMIF2DEC	3	decoupling for AM IF2 input
IFAMP2OUT	4	IF amplifier 2 output (10.7 MHz)
AMNBHOLD	5	AM noise blanker threshold
AMIF2IN	6	AM IF2 input (450 kHz) for demodulator AGC and AM level detector
IF1GND	7	AM IF1 ground
IFAMP2IN	8	IF amplifier 2 input (10.7 MHz)
C_{offset}	9	DC feedback for offset compensation RDS mute
IMUTEREF	10	mute reference current output for testing
IFAMP2DEC	11	IF amplifier 2 decoupling and AGC capacitor for AM noise blanker
IFAMP1OUT	12	IF amplifier 1 output (10.7 MHz)
n.c.	13	not connected
IFAMP1IN	14	IF amplifier 1 and AM mixer 2 input (10.7 MHz)
n.c.	15	not connected
V_{DDA1}	16	analog supply voltage 1 (8.5 V) for IF amplifier 1 and 2
IFAMP1DEC	17	AM mixer 2 and FM IF amplifier 1 decoupling
MIX1OUT1	18	FM mixer and AM mixer 1 IF output 1 (10.7 MHz)
MIX1OUT2	19	FM mixer and AM mixer 1 IF output 2 (10.7 MHz)
V_{DDA2}	20	analog supply voltage 2 (8.5 V) for FM mixer and AM mixer 1
n.c.	21	not connected
AMMIX1IN2	22	AM mixer 1 input 2
AMMIX1IN1	23	AM mixer 1 input 1
n.c.	24	not connected
n.c.	25	not connected
T1AMAGC	26	1st time constant of AM front-end AGC
T2AMAGC	27	2nd time constant of AM front-end AGC
IAMAGC	28	PIN diode drive current output of AM front-end AGC
$V_{ref(FMMIX)}$	29	reference voltage for FM I/Q mixer
FMMIXIN1	30	FM RF mixer input 1
RFGND	31	RF ground
n.c.	32	not connected
FMMIXIN2	33	FM RF mixer input 2
WBSW	34	buffered weather band flag output
IFMAGC	35	PIN diode drive current output of FM front-end AGC
T2FMAGC	36	2nd time constant of FM front-end AGC
T1FMAGC	37	1st time constant of FM front-end AGC
DAAOUT	38	output of digital auto alignment circuit for antenna tank circuit
DAATD	39	temperature compensation diode for digital auto alignment circuit for antenna tank circuit
DAAIN	40	input of digital auto alignment circuit for antenna tank circuit

SYMBOL	PIN	DESCRIPTION
n.c.	41	not connected
V_{tune}	42	tuning voltage
CPOUT	43	charge pump output
V_{DDA3}	44	analog supply voltage 3 (8.5 V) for tuning PLL
FREF	45	reference frequency output for signal processor IC
V_{DDD}	46	digital supply voltage (5 V)
DGND	47	digital ground
VCOGND	48	VCO ground
OSCFDB	49	VCO feedback
OSCTNK	50	VCO tank circuit
V_{DDA4}	51	analog supply voltage 4 (8.5 V) for VCO
n.c.	52	not connected
AFSAMPLE	53	AF sample flag output for car audio signal processor IC
AFHOLD	54	AF hold flag output for car audio signal processor IC
TRDSMUTE	55	time constant for RDS update mute
AMAFIF2	56	AM demodulator AF output or IF2 output for AM stereo (multiplexed by I^2C-bus)
RDSMPX	57	MPX output for RDS decoder and signal processor (not muted)
FMMPX	58	FM demodulator MPX output
V_{DDA5}	59	analog supply voltage 5 (5 V) for on-chip power supply
n.c.	60	not connected
V_{DDA6}	61	analog supply voltage 6 (8.5 V) for on-chip power supply
n.c.	62	not connected
SDA	63	I^2C-bus data line input and output
SCL	64	I^2C-bus clock line input
n.c.	65	not connected
IF2GND	66	AM IF2 ground
QDET1	67	quadrature demodulator tank 1
QDET2	68	quadrature demodulator tank 2
C_{AFC}	69	FM demodulator AFC capacitor
V_{level}	70	level voltage output for AM and FM
XTAL1	71	crystal oscillator 1
XTALGND	72	crystal oscillator ground
XTAL2	73	crystal oscillator 2
n.c.	74	not connected
TMUTE	75	time constant for mute control voltage
IREF	76	reference current for power supply
AMMIX2OUT1	77	AM mixer 2 output 1 (450 kHz)
AMMIX2OUT2	78	AM mixer 2 output 2 (450 kHz)
C_{AGC}	79	AM IF AGC capacitor
n.c.	80	not connected

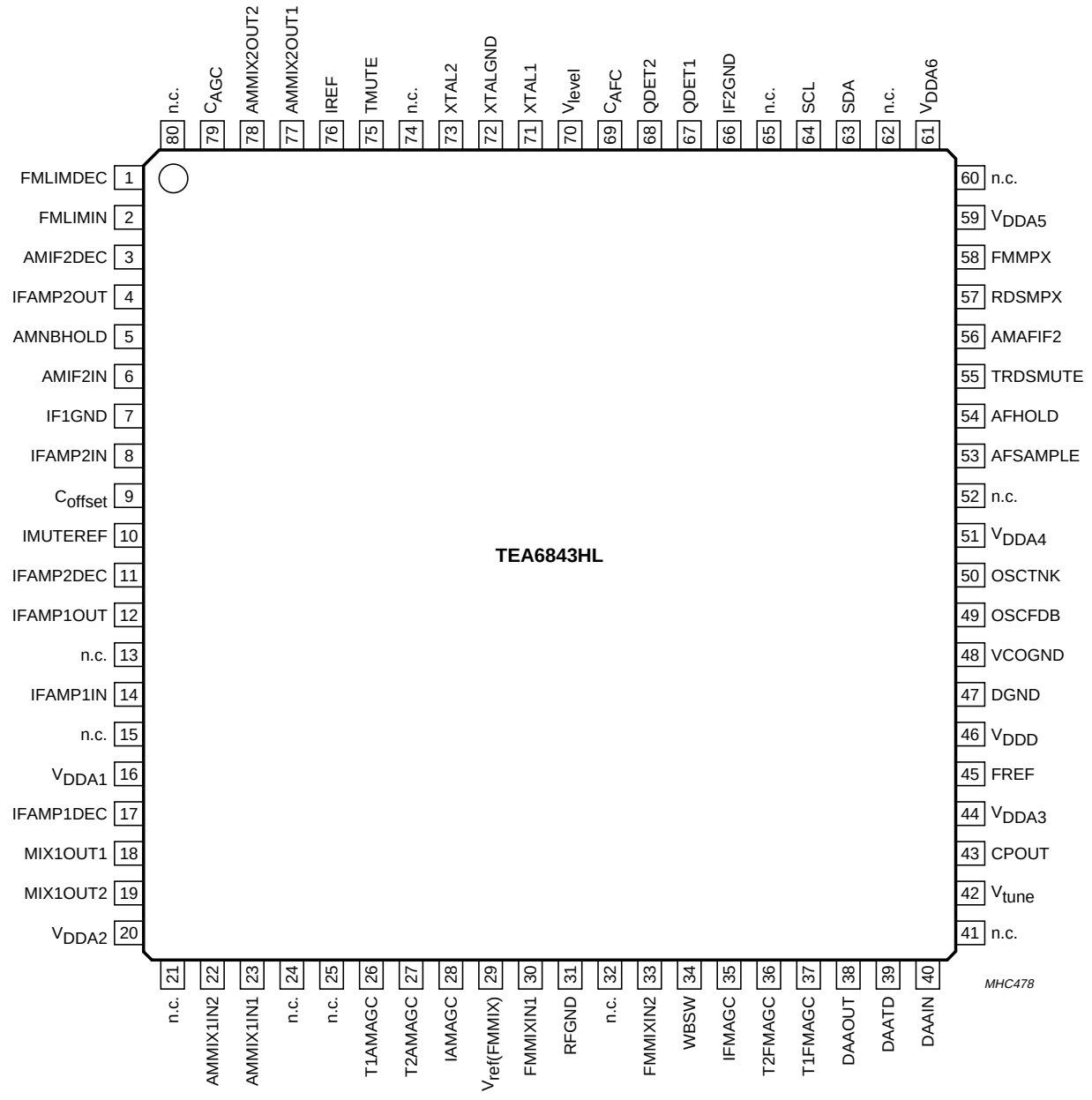


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

7.1 Oscillators

7.1.1 VCO

The L and C tuned VCO provides the local oscillator signal for both FM and AM mixer 1. It has a frequency range of 151.2 to 248.2 MHz.

7.1.2 CRYSTAL OSCILLATOR

The crystal oscillator provides a 20.5 MHz signal that is used for:

- Reference frequency for frequency synthesizer PLL
- Local oscillator for AM mixer 2
- Reference frequency for the IF counter
- Timing signal for the RDS update algorithm
- Reference frequency (75.368 kHz) for the TEA688x (car audio signal processor - CASP) or TEF689x (car radio integrated signal processor - CRISP).

7.1.3 PLL

Fast synthesizer PLL tuning system with local control for inaudible RDS updating.

7.2 FM signal channel

7.2.1 DAA

FM RF Digital Auto Alignment (DAA) circuitry for the conversion of the VCO tuning voltage to a controlled alignment voltage for the FM antenna tank circuit.

7.2.2 FM I/Q MIXER

FM quadrature mixer converts FM RF (65 to 162.55 MHz) to IF of 10.7 MHz. The FM mixer provides inherent image rejection and high RF sensitivity.

It is capable of tuning the US FM, US weather, Europe FM, Japan FM and East Europe FM bands:

- US FM = 87.9 to 107.9 MHz
- US weather FM = 162.4 to 162.55 MHz
- Europe FM = 87.5 to 108 MHz
- Japan FM = 76 to 91 MHz
- East Europe FM = 65.8 to 74 MHz.

7.2.3 FM KEYED AGC

The AGC threshold is programmable and the keyed AGC function is switchable via the I^2C-bus.

If the keyed AGC function is activated, the AGC function is keyed by the narrow band level (IF).

The AGC PIN diode drive can be set via the I^2C-bus to local function for search tuning.

7.2.4 FM IF AMPLIFIERS

The two FM IF amplifiers provide 10 dB and 8.5 dB amplification with high linearity and dynamic range.

7.2.5 FM DEMODULATOR

The FM quadrature demodulator includes automatic centre frequency adjustment and THD compensation.

7.2.6 FM MPX SOFT MUTE

Muting depth and start of muting are adjustable via the I^2C-bus.

7.3 AM signal channel

7.3.1 AM TUNER

The AM tuner is realized in a double conversion technique and is capable of selecting LW, MW and SW bands.

AM mixer 1 converts AM RF to IF1 of 10.7 MHz, while AM mixer 2 converts IF1 of 10.7 MHz to IF2 of 450 kHz:

- LW = 144 to 288 kHz
- MW = 522 to 1710 kHz (European and US AM band)
- SW = 5.85 to 9.99 MHz (including the 31 m, 41 m and 49 m bands).

7.3.2 AM RF AGC AND IF2 AGC

The AM RF includes a PIN diode drive circuit. The threshold detection points for AM AGC are performed at AM mixer 1 and AM IF2. AGC thresholds are programmable at AM mixer 1 input via the I^2C-bus.

7.3.3 AM AF OR IF2 SWITCH

The AM output provides either a demodulated AM Audio Frequency (AF) or the corresponding AM IF2 signal. The IF2 signal can be used for AM stereo decoder processing.

7.3.4 AM SOFT MUTE

The AM detector output is either not muted or signal strength dependent soft muted audio. The soft mute function can be switched off via the I^2C-bus.

7.3.5 AM NOISE BLANKER

The detection point for the AM noise blanker is the output stage of AM mixer 1, while blanking is realized at the output of the mixer 2.

Trigger sensitivity can be modified by changing the resistor value at pin AMNBHOLD.

7.4 FM and AM level detector

FM and AM level detectors provide the temperature compensated output voltage. The starting points and slopes of the level detector outputs are programmable via the I^2C-bus.

7.5 Buffer output for weather band flag

In weather band mode the output is HIGH.

7.6 Test mode

The test mode of the IC is activated by connecting pin FREF through a 100 kΩ resistor to V_{DDA1}.

The test mode is intended for IC test during IC and radio manufacturing.

In test mode the settling time of the AM IF2 AGC is reduced to less than 100 ms in the nominal application.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1 for IF amplifier 1 and 2		–0.3	+10	V
V_{DDA2}	analog supply voltage 2 for FM mixer and AM mixer 1		–0.3	+10	V
V_{DDA3}	analog supply voltage 3 for tuning PLL		–0.3	+10	V
V_{DDA4}	analog supply voltage 4 for VCO		–0.3	+10	V
V_{DDA5}	analog supply voltage 5 for on-chip power supply		–0.3	+6.5	V
V_{DDA6}	analog supply voltage 6 for on-chip power supply		–0.3	+10	V
V_{DDD}	digital supply voltage		–0.3	+6.5	V
$\Delta V_{DD8.5\text{-}DD5}$	difference between any 8.5 V supply voltage and any 5 V supply voltage	note 1	–0.3	–	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{es}	electrostatic handling voltage	note 2	–200	+200	V
		note 3	–2000	+2000	V

Notes

1. To avoid damages and wrong operation it is necessary to keep all 8.5 V supply voltages at a higher level than any 5 V supply voltage. This is also necessary during power-on and power-down sequences. Precautions have to be provided in such a way that interferences can not pull down the 8.5 V supply below the 5 V supply.
2. Machine model (R = 0 Ω, C = 200 pF).
3. Human body model (R = 1.5 kΩ, C = 100 pF).

9 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	in free air	54	K/W

10 DC CHARACTERISTICS

$V_{MIX1OUT} = V_{AMMIX2OUT} = V_{DDA(n)} = 8.5$ V; $V_{DDA5} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage						
$V_{DDA(n)}$	analog supply voltages 1 to 4 and 6		8	8.5	9	V
$V_{MIX1OUT}$; $V_{AMMIX2OUT}$	mixer supply voltages		8	8.5	9	V
V_{DDA5}	analog supply voltage 5		4.75	5	5.25	V
V_{DDD}	digital supply voltage		4.75	5	5.25	V
Supply current in FM mode						
I_{DDD}	digital supply current		18	23	28	mA
I_{DDA1}	analog supply current 1 for IF amplifier 1 and 2		11	13	15	mA
I_{DDA2}	analog supply current 2 for FM mixer and AM mixer 1		4.2	5.2	6.2	mA
I_{DDA3}	analog supply current 3 for tuning PLL	data byte 5: bit TMS3 = 1	2.3	3	3.6	mA
I_{DDA4}	analog supply current 4 for VCO		5.2	6.5	7.8	mA
I_{DDA5}	analog supply current 5 for on-chip power supply		6.5	9.3	11.2	mA
I_{DDA6}	analog supply current 6 for on-chip power supply		16	20	24	mA
$I_{MIX1OUT1}$	bias current of FM mixer output 1		4.8	6	7.2	mA
$I_{MIX1OUT2}$	bias current of FM mixer output 2		4.8	6	7.2	mA
Supply current in AM mode						
I_{DDD}	digital supply current		18	23	28	mA
I_{DDA1}	analog supply current 1 for AM mixer 2		–	240	–	µA
I_{DDA2}	analog supply current 2 for FM mixer and AM mixer 1		1.6	2	2.4	mA
I_{DDA3}	analog supply current 3 for tuning PLL	data byte 5: bit TMS3 = 1	1.3	1.7	2.1	mA
I_{DDA4}	analog supply current 4 for VCO		5	6.5	8	mA
I_{DDA5}	analog supply current 5 for on-chip power supply		12.7	17.4	22.1	mA
I_{DDA6}	analog supply current 6 for on-chip power supply		15	19	23	mA
$I_{MIX1OUT1}$	bias current of AM mixer 1 output 1		4.8	6	7.2	mA
$I_{MIX1OUT2}$	bias current of AM mixer 1 output 2		4.8	6	7.2	mA
$I_{AMMIX2OUT1}$	bias current of AM mixer 2 output 1		3.6	4.5	5.4	mA
$I_{AMMIX2OUT2}$	bias current of AM mixer 2 output 2		3.6	4.5	5.4	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power supply reference current generator: pin IREF						
$V_{o(ref)}$	output reference voltage		4	4.25	4.5	V
R_o	output resistance		8	11	13	kΩ
$I_{o(max)}$	maximum output current		–100	–	+100	nA

11 AC CHARACTERISTICS

$V_{MIX1OUT} = V_{AMMIX2OUT} = V_{DDA(n)} = 8.5$ V; $V_{DDA5} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; see Figs 14 and 15; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled oscillator						
f_{osc}	oscillator frequency		151.2	–	248.2	MHz
C/N	carrier-to-noise ratio	f_{osc} = 200 MHz; Δf = 10 kHz; B = 1 Hz	–	101	–	dBc
RR	ripple rejection $\frac{\Delta f_{osc}}{f_{osc}}$	f_{ripple} = 100 Hz; $V_{DDA4(ripple)}$ = 100 mV (RMS)				
		f_{osc} = 250 MHz	90	97	–	dB
		f_{osc} = 200 MHz	92	99	–	dB
Crystal oscillator: pins XTAL1, XTALGND and XTAL2						
f_{osc}	oscillator frequency		–	20.5	–	MHz
R_i	real part of input impedance	$V_{XTAL1} - V_{XTAL2}$ = 1 mV	–500	–	–	Ω
C_i	input capacitance		8	10	12	pF
$V_{o(osc)(rms)}$	oscillator output voltage (RMS value)		240	350	500	mV
C/N	carrier-to-noise ratio	f_{osc} = 20.5 MHz (10.25 MHz); Δf = 10 kHz	–	112	–	$\frac{dBc}{\sqrt{Hz}}$
Oscillator divider N1						
N1	oscillator divider ratio	FM mode				
		standard, East Europe and local	–	2	–	
		weather band (WX)	–	1	–	
Oscillator divider N2						
N2	oscillator divider ratio	AM mode				
		LW and MW	–	10	–	
		SW	–	5	–	
Synthesizer						
PROGRAMMABLE DIVIDER						
N_{prog}	programmable divider ratio		512	–	32767	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔN_{step}	programmable divider step size		–	1	–	
REFERENCE FREQUENCY DIVIDER						
N_{ref}	crystal oscillator divider ratio	f_{osc} = 20.5 MHz				
		f_{ref} = 100 kHz	–	205	–	
		f_{ref} = 50 kHz	–	410	–	
		f_{ref} = 25 kHz	–	820	–	
		f_{ref} = 20 kHz	–	1025	–	
		f_{ref} = 10 kHz	–	2050	–	
CHARGE PUMP: PIN CPOUT						
$I_{sink(cp1)l}$	low charge pump 1 sink current	0.4 V < V_{CPOUT} < 7.6 V; data byte 4: bit 0 = 0, bit 1 = 1, bit 2 = 1 for FM weather band; $f_{VCO} > f_{ref} \times$ divider ratio	–	300	–	µA
$I_{source(cp1)l}$	low charge pump 1 source current	0.4 V < V_{CPOUT} < 7.6 V; data byte 4: bit 0 = 0, bit 1 = 1, bit 2 = 1 for FM weather band; $f_{VCO} < f_{ref} \times$ divider ratio	–	–300	–	µA
$I_{sink(cp1)h}$	high charge pump 1 sink current	0.4 V < V_{CPOUT} < 7.6 V; data byte 4: bit 0 = 1, bit 1 = 1, bit 2 = 1 for AM IF2 output; N2 = 10 (LW and MW); $f_{VCO} > f_{ref} \times$ divider ratio	–	1	–	mA
$I_{source(cp1)h}$	high charge pump 1 source current	0.4 V < V_{CPOUT} < 7.6 V; data byte 4: bit 0 = 1, bit 1 = 1, bit 2 = 1 for AM IF2 output; N2 = 10 (LW and MW); $f_{VCO} < f_{ref} \times$ divider ratio	–	–1	–	mA
$I_{sink(cp2)}$	charge pump 2 sink current	0.3 V < V_{CPOUT} < 7.1 V; data byte 4: bit 0 = 0, bit 1 = 0, bit 2 = 0; FM standard mode; $f_{VCO} > f_{ref} \times$ divider ratio	–	130	–	µA
$I_{source(cp2)}$	charge pump 2 source current	0.3 V < V_{CPOUT} < 7.1 V; data byte 4: bit 0 = 0, bit 1 = 0, bit 2 = 0; FM standard mode; $f_{VCO} < f_{ref} \times$ divider ratio	–	–130	–	µA
CHARGE PUMP: PIN V_{tune}						
$I_{sink(cp3)}$	charge pump 3 sink current	0.4 V < V_{tune} < 7.6 V; data byte 4: bit 0 = 0, bit 1 = 0, bit 2 = 0; FM standard mode; $f_{VCO} > f_{ref} \times$ divider ratio	–	3	–	mA
$I_{source(cp3)}$	charge pump 3 source current	0.4 V < V_{tune} < 7.6 V; data byte 4: bit 0 = 0, bit 1 = 0, bit 2 = 0; FM standard mode; $f_{VCO} < f_{ref} \times$ divider ratio	–	–3	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Antenna Digital Auto Alignment (DAA)						
DAA INPUT: PIN DAAIN						
$I_{bias(cp)}$	charge pump buffer input bias current	V_{DAAIN} = 0.4 to 8 V	–10	–	+10	nA
$V_{i(cp)}$	charge pump buffer input voltage		0	–	8.5	V
DAA OUTPUT: PIN DAAOUT						
$V_{o(min)}$	minimum DAA output voltage	data byte 3 = 10000000; FM mode; V_{DAAIN} = 0.5 V; V_{DAATD} = 0.45 V	–	–	0.5	V
$V_{o(max)}$	maximum DAA output voltage	data byte 3 = 11111111; FM mode; V_{DAAIN} = 4 V; V_{DAATD} = 0.45 V	8	–	8.5	V
V_o	DAA output voltage	I_{DAAOUT} < 100 µA; AM mode	–	–	0.3	V
		data byte 3 = 10000000; FM mode; V_{DAAIN} = 4 V; V_{DAATD} = 0.45 V; note 1	–	1.7	–	V
		data byte 3 = 11111111; FM mode; V_{DAAIN} = 3 V; V_{DAATD} = 0.45 V; note 1	6.2	6.5	6.8	V
$V_{o(n)}$	DAA output noise voltage	data byte 3 = 11000000; FM mode; V_{DAAIN} = 4 V; V_{DAATD} = 0.45 V; B = 400 Hz to 30 kHz	–	30	100	µV
$\Delta V_{o(T)}$	DAA output voltage variation with temperature	T_{amb} = –40 to +85 °C; data byte 3 = 10101011	–8	–	+8	mV
$\Delta V_{o(step)}$	DAA step accuracy $V_{DAAOUT(n+1)} - V_{DAAOUT(n)}$	n = 0 to 127; FM mode; V_{DAAOUT} < 8 V; V_{DAAIN} = 2 V; V_{DAATD} = 0.45 V	$0.5V_{LSB}$	V_{LSB}	$1.5V_{LSB}$	mV
$\Delta V_{o(sink)}$	DAA output variation caused by sink current	V_{DAAIN} = 4 V; I_L = 50 µA	$-V_{LSB}$	–	$+V_{LSB}$	
$\Delta V_{o(source)}$	DAA output variation caused by source current	V_{DAAIN} = 4 V; I_L = –50 µA	$-V_{LSB}$	–	$+V_{LSB}$	
t_{st}	DAA output settling time	V_{DAAOUT} = 0.2 to 8.25 V; C_L = 270 pF	–	20	30	µs
RR	ripple rejection $\frac{V_{DAAOUT}}{V_{DDA3}}$	data byte 3 = 10101011; FM mode; V_{DAAIN} = 4 V; V_{DAATD} = 0.45 V; f_{ripple} = 100 Hz; $V_{DDA3(ripple)}$ = 100 mV	–	50	–	dB
C_L	DAA output load capacitance	V_{DAAOUT} < 8 V; FM mode	–	–	270	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DAA TEMPERATURE COMPENSATION: PIN DAATD						
I_{source}	compensation diode source current	V_{DAATD} = 0.2 to 1.2 V	–50	–40	–30	µA
TC_{source}	temperature coefficient of compensation diode source current	V_{DAATD} = 0.2 to 1.2 V; T_{amb} = –40 to +85 °C	–300	–	+300	$\frac{10^{-6}}{K}$
IF counter (FM IF1 or AM IF2 counter)						
N_{IF}	IF counter length for AM and FM		–	8	–	bit
$T_{count(IF)}$	IF counter period	data byte 4: bit 7 = 1	–	2	–	ms
		data byte 4: bit 7 = 0	–	20	–	ms
$R_{precount}$	FM IF counter prescaler ratio	data byte 4: bit 3 = 1	–	10	–	
		data byte 4: bit 3 = 0	–	100	–	
$V_{FMLIMIN(sens)(rms)}$	FM sensitivity voltage (RMS value)	FM mode	–	30	100	µV
N	counter result (decimal)	period = 2 ms; f_{IF1} = 10.7 MHz; $V_{FMLIMIN}$ = 100 µV (RMS)				
		prescaler ratio = 10	–	92	–	
		prescaler ratio = 100	–	214	–	
		period = 20 ms; f_{IF1} = 10.7 MHz; $V_{FMLIMIN}$ = 100 µV (RMS)				
		prescaler ratio = 10	–	152	–	
		prescaler ratio = 100	–	92	–	
$V_{AMIF2IN(sens)(rms)}$	AM sensitivity voltage (RMS value)	AM mode; m = 0	–	50	100	µV
N	counter result (decimal)	period = 2 ms; f_{IF2} = 450 kHz; $V_{AMIF2IN}$ = 200 µV (RMS)	–	133	–	
		period = 20 ms; f_{IF2} = 450 kHz; $V_{AMIF2IN}$ = 200 µV (RMS)	–	40	–	
Reference frequency for car signal processor IC; note 2						
REFERENCE FREQUENCY DIVIDER						
N_{ref}	crystal oscillator divider ratio		–	272	–	
f_{ref}	reference frequency at pin FREF	f_{osc} = 20.5 MHz	–	75.368	–	kHz
VOLTAGE GENERATOR: PIN FREF						
$V_{o(p-p)}$	AC output voltage (peak-to-peak value)	R_L = ∞	80	130	200	mV
V_O	DC output voltage		3.2	3.4	3.7	V
R_o	output resistance		–	–	50	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{L(min)}$	minimum load resistance for first I^2C-bus address		1	–	–	MΩ
AM signal channel						
RF AGC STAGE INPUTS						
Pins AMMIX1IN1 and AMMIX1IN2						
$V_{i(RF)}$	RF input voltage for AGC start level	data byte 5: bit 5 = 0, bit 6 = 0	–	375	–	mV
		data byte 5: bit 5 = 1, bit 6 = 0	–	500	–	mV
		data byte 5: bit 5 = 0, bit 6 = 1	–	625	–	mV
		data byte 5: bit 5 = 1, bit 6 = 1	–	750	–	mV
Pin AMIF2IN						
$V_{i(IF2)}$	IF2 input voltage	AGC start level	280	380	500	mV
PIN diode drive: pin IAMAGC						
$I_{sink(max)}$	maximum AGC sink current	V_o = 2.8 V	11	15	19	mA
I_{sink}	AGC sink current	FM mode	1	–	–	mA
R_o	output resistance	I_o = 1 μA	1	–	–	MΩ
C_o	AM AGC current generator output capacitance		–	5	7	pF
AM MIXER 1 (IF1 = 10.7 MHz)						
Mixer inputs: pins AMMIX1IN1 and AMMIX1IN2						
R_i	input resistance		15	25	35	kΩ
C_i	input capacitance		2.5	4	5.5	pF
V_I	DC input voltage		2.3	2.7	3.1	V
$V_{i(max)}$	maximum input voltage	1 dB compression point of AM mixer 1 output (peak-to-peak value)	500	–	–	mV
$V_{i(n)(eq)}$	equivalent input noise voltage	band limited noise; R_{gen} = 750 Ω; R_L = 2.8 kΩ	–	5.8	8	$\frac{nV}{\sqrt{Hz}}$
Mixer outputs: pins MIX1OUT1 and MIX1OUT2						
R_o	output resistance		100	–	–	kΩ
C_o	output capacitance		–	5	7	pF
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)		12	15	–	V
$g_{m(conv)}$	conversion transconductance $\frac{I_{MIX1OUT}}{V_{AMMIX1IN}}$		2.0	2.55	3.2	$\frac{mA}{V}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$g_{m(conv)(T)}$	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$		–	-9×10^{-4}	–	K^{-1}
IP3	3rd-order intermodulation	R_L = 2.8 kΩ; Δf = 300 kHz	135	138	–	dBμV
IP2	2nd-order intermodulation	R_L = 2.8 kΩ	–	170	–	dBμV
F	noise figure of AM mixer 1		–	4.5	7.1	dB
I_{bias}	mixer bias current	AM mode	4.8	6	7.2	mA
AM MIXER 2 (IF2 = 450 kHz)						
Mixer inputs: pins IFAMP1IN and IFAMP1DEC						
R_i	input resistance		270	330	390	Ω
C_i	input capacitance		–	5	7	pF
V_I	DC input voltage		2.4	2.8	3.2	V
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of AM mixer 2 output (peak-to-peak value)	1.1	1.4	–	V
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 330 Ω; R_L = 4 kΩ	–	15	22	$\frac{nV}{\sqrt{Hz}}$
Mixer outputs: pins AMMIX2OUT1 and AMMIX2OUT2						
R_o	output resistance		100	–	–	kΩ
C_o	output capacitance		–	5	7	pF
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)	V_{DDA1} = 8.5 V	12	15	–	V
$g_{m(conv)}$	conversion transconductance $\frac{I_{AMMIX2OUT}}{V_{IFAMP1IN}}$		1.3	1.6	1.9	$\frac{mA}{V}$
$g_{m(conv)(T)}$	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$		–	-9×10^{-4}	–	K^{-1}
IP3	3rd-order intermodulation	R_L = 4 kΩ; Δf = 300 kHz	134	137	–	dBμV
IP2	2nd-order intermodulation	R_L = 4 kΩ	–	170	–	dBμV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
F	noise figure of AM mixer 2		–	16	19.5	dB
I_{bias}	mixer bias current	AM mode	3.6	4.5	5.4	mA
I_L	mixer leakage current	FM mode	–	–	50	μA
IF2 AGC STAGE: PINS AMIF2IN AND AMIF2DEC						
$V_{AGC(start)}$	AGC start voltage	input carrier voltage	–	14	30	μV
$V_{AGC(stop)}$	AGC stop voltage	maximum input peak voltage	1	–	–	V
$V_{AGC(ctrl)}$	AGC control voltage	$V_{AMIF2IN}$ = 1 mV	4.1	4.3	4.7	V
ΔAGC	AGC range	between start and stop of AGC	–	89	–	dB
R_i	input resistance		1.8	2	2.2	kΩ
C_i	input capacitance		–	–	5	pF
V_i	input voltage	audio attenuation α = −10 dB				
		data byte 5: bit 4 = 1; mute on	10	22	37	μV
		data byte 5: bit 4 = 0; mute off	–	6	12	μV
$V_{sens(rms)}$	sensitivity voltage (RMS value)	m = 0.3; f_{mod} = 400 Hz; B_{AF} = 2.5 kHz; R_{source} = 2 kΩ				
		(S+N)/N = 26 dB	–	45	65	μV
		(S+N)/N = 46 dB	–	600	900	μV
AM DETECTOR OUTPUT: PIN AMAFIF2; see Fig.3						
$V_{o(min)(rms)}$	minimum AM IF2 output level (RMS value)	data byte 4: bit 0 = 1, bit 1 = 1; m = 0; $V_{AMIF2IN}$ = 14 μV	1.5	3	4.5	mV
$V_{o(max)(rms)}$	maximum AM IF2 output level (RMS value)	data byte 4: bit 0 = 1, bit 1 = 1; m = 0; $V_{AMIF2IN}$ = 5 mV	130	180	230	mV
$V_{o(rms)}$	AM AF output voltage level (RMS value)	data byte 4: bit 0 = 1, bit 1 = 0; m = 0.3; f_{mod} = 400 Hz; $V_{AMIF2IN}$ = 100 μV to 500 mV (RMS)	235	285	340	mV
R_o	output resistance	data byte 4: bit 0 = 1, bit 1 = 1	–	–	500	Ω
C_o	output capacitance	data byte 4: bit 0 = 1, bit 1 = 0	–	5	7	pF
Z_L	load impedance	data byte 4: bit 0 = 1, bit 1 = 0	100	–	–	kΩ
		data byte 4: bit 0 = 1, bit 1 = 1	10	–	–	kΩ
RR	ripple rejection	f_{ripple} = 100 Hz; $V_{DDA5(ripple)}$ = 100 mV (RMS)	30	40	–	dB
AM DETECTOR; see Fig.3						
(S+N)/N	maximum signal plus noise-to-noise ratio	m = 0.3; f_{mod} = 400 Hz; B_{AF} = 2.5 kHz; R_{source} = 2 kΩ	54	60	70	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	B_{AF} = 2.5 kHz; C_{AGC} = 22 µF; $V_{AMIF2IN}$ = 100 µV to 250 mV (RMS)				
		m = 0.8; f_{mod} = 400 Hz	–	0.5	1	%
		m = 0.9; f_{mod} = 400 Hz	–	1	2	%
		m = 0.8; f_{mod} = 100 Hz	–	1.25	2.5	%
		m = 0.9; f_{mod} = 100 Hz	–	1.75	3.5	%
t_{sw}	FM to AM switching time	$V_{AMIF2IN}$ = 100 µV; C_{AGC} = 22 µF	–	1000	1500	ms
t_{st}	AM demodulator AGC settling time	C_{AGC} = 22 µF				
		$V_{AMIF2IN}$ = 100 µV to 100 mV	–	800	1200	ms
		$V_{AMIF2IN}$ = 100 mV to 100 µV	–	1200	1800	ms
AM IF2 LEVEL DETECTOR: PIN V_{level}; see Fig.4						
V_{level}	level output DC voltage	$V_{AMIF2IN}$ = 10 µV to 1 V	0	–	5	V
		$V_{AMIF2IN}$ < 1 µV; standard setting of level DAA	0.1	0.35	0.8	V
		$V_{AMIF2IN}$ = 1.4 mV; standard setting of level DAA	–	2.2	–	V
ΔV_{level}	step size of starting point adjustment	standard setting of level slope	40	53	70	mV
$V_{level(slope)}$	slope of level voltage $\frac{\Delta V_{level}}{\Delta V_{AMIF2IN}}$	$V_{AMIF2IN}$ = 140 µV to 140 mV; standard setting of level slope	800	1000	1200	$\frac{mV}{20\ dB}$
ΔV_{step}	step size of slope adjustment	$V_{AMIF2IN}$ = 1.4 mV	55	75	95	$\frac{mV}{20\ dB}$
B_{level}	bandwidth of level output voltage		200	300	–	kHz
R_o	output resistance		–	–	500	Ω
RR	ripple rejection $\frac{V_{level}}{V_{DDA6}}$	f_{ripple} = 100 Hz; $V_{DDA6(ripple)}$ = 100 mV (RMS)	–	40	–	dB
AM NOISE BLANKER; see Fig.5						
Threshold: pin AMNBHOLD						
V_O	DC output voltage		4.4	4.75	5.25	V
t_{sup}	suppression time		6	7.5	10	µs
$f_{trigger}$	trigger sensitivity	V_{pulse} = 200 mV; V_{level} < 1.8 V	–	1000	–	Hz
		V_{pulse} = 200 mV; V_{level} > 2.2 V	–	–	100	Hz
		V_{pulse} = 20 mV; V_{level} < 1.8 V	–	–	100	Hz
Noise detector output: pin TRDSMUTE						
$I_{sink(AGC)}$	AM noise blanker AGC sink current	$V_{TRDSMUTE}$ = 3 V	30	45	60	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{AGC}	AM noise blanker AGC voltage	AM mixer 1 input V_i = 0 V	2.1	2.45	2.85	V
FM signal channel						
RF AGC (FM DISTANCE MODE)						
FM mixer inputs: pins FMMIXIN1 and FMMIXIN2						
$V_{i(RF)(rms)}$	RF input voltage for start of wideband AGC (RMS value)	data byte 5: bit 5 = 1, bit 6 = 1	–	4	–	mV
		data byte 5: bit 5 = 0, bit 6 = 1	–	8	–	mV
		data byte 5: bit 5 = 1, bit 6 = 0	–	12	–	mV
		data byte 5: bit 5 = 0, bit 6 = 0	–	16	–	mV
AGC control: pin T2FMAGC						
R_{source}	source resistance		4	5	6	kΩ
$V_{O(ref)}$	DC output reference voltage	data byte 5: bit 5 = 0, bit 6 = 0; $V_{FMMIXIN1-FMMIXIN2}$ = 0 V	3.8	4.1	4.4	V
PIN diode drive output: pin IFMAGC						
$I_{sink(AGC)(max)}$	maximum AGC sink current	V_{IFMAGC} = 2.5 V; $V_{T2FMAGC} = V_{O(ref)} - 0.5$ V; data byte 5: bit 5 = 0, bit 6 = 0, bit 7 = 0; data byte 4: bit 1 = 0	8	10.5	14	mA
$I_{source(AGC)(max)}$	maximum AGC source current	V_{IFMAGC} = 2.5 V; $V_{T2FMAGC} = V_{O(ref)} + 0.5$ V; data byte 5: bit 5 = 0, bit 6 = 0, bit 7 = 0; data byte 4: bit 1 = 0	–14	–10.5	–8	mA
$I_{source(AGC)}$	AGC source current	AM mode	–19	–14	–10	mA
		V_{IFMAGC} = 2.5 V; data byte 4: bit 0 = 0, bit 1 = 1, bit 2 = 0 (FM local)	–4.4	–3.7	–2.7	mA
Level voltage: pin V_{level}						
V_{th}	threshold voltage for narrow-band AGC	data byte 5: bit 5 = 0, bit 6 = 0, bit 7 = 1	600	750	900	mV
FM RF MIXER						
FM mixer inputs: pins FMMIXIN1 and FMMIXIN2						
$V_{i(RF)(max)}$	maximum RF input voltage	1 dB compression point of FM mixer output voltage (peak-to-peak value)	70	140	–	mV
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 200 Ω; R_L = 2.8 kΩ	–	2.6	3.1	$\frac{nV}{\sqrt{Hz}}$
R_i	input resistance		1.4	2.8	4.2	kΩ
C_i	input capacitance		–	5	7	pF
FM mixer outputs: pins MIX1OUT1 and MIX1OUT2						
R_o	output resistance		100	–	–	kΩ
C_o	output capacitance		2	3.5	5	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{bias}	mixer bias current	FM mode	4.8	6	7.2	mA
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)		3	–	–	V
FM mixer reference voltage: pin $V_{ref(FMMIX)}$						
V_{ref}	reference voltage	FM mode	6.5	7.1	7.9	V
		AM mode	2.7	3.1	3.4	V
FM mixer						
$g_{m(conv)}$	conversion transconductance $\frac{I_{MIX1OUT}}{V_{FMMIXIN}}$		8.5	13	18	$\frac{mA}{V}$
$g_{m(conv)(T)}$	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$		–	-1×10^{-3}	–	K^{-1}
F	noise figure		–	3	4.6	dB
$R_{gen(opt)}$	optimum generator resistance		180	240	300	Ω
IP3	3rd-order intermodulation		116	119	–	dBµV
IRR	image rejection ratio $\frac{V_{MIX1OUTwanted}}{V_{MIX1OUTimage}}$	$f_{RFwanted}$ = 87.5 MHz; $f_{RFimage}$ = 108.9 MHz	25	30	–	dB
		data byte 4 = X010X110; $f_{RFwanted}$ = 162.475 MHz; $f_{RFimage}$ = 183.875 MHz; weather band mode	22	30	–	dB
IF AMPLIFIER 1						
G	gain $\frac{V_{IFAMP1OUT}}{V_{IFAMP1IN}}$	R_L = 330 Ω; $V_{IFAMP1IN}$ = 1 mV	8.5	10.5	12.5	dB
F	noise figure		–	10	13	dB
IP3	3rd-order intermodulation		117	120	–	dBµV
Inputs: pins IFAMP1IN and IFAMP1DEC						
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of IF amplifier 1 output voltage (peak value)	250	–	–	mV
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 330 Ω; R_L = 330 Ω	–	8	10	$\frac{nV}{\sqrt{Hz}}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_i	input resistance		270	330	390	Ω
C_i	input capacitance		–	5	7	pF
Output: pin IFAMP1OUT						
$V_{o(max)(p)}$	maximum output voltage (peak value)		1.2	1.5	–	V
R_o	output resistance		270	330	390	Ω
C_o	output capacitance		–	5	7	pF
IF AMPLIFIER 2						
G	gain $\frac{V_{IFAMP2OUT}}{V_{IFAMP2IN}}$	R_L = 330 Ω; $V_{IFAMP2IN}$ = 1 mV	6.5	8.5	10.5	dB
F	noise figure		–	13	15	dB
IP3	3rd-order intermodulation		127	130	–	dBμV
Inputs: pins IFAMP2IN and IFAMP2DEC						
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of IF amplifier 2 output voltage (peak value)	500	–	–	mV
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 330 Ω; R_L = 330 Ω	–	10	13	$\frac{nV}{\sqrt{Hz}}$
R_i	input resistance		270	330	390	Ω
C_i	input capacitance		–	5	7	pF
Output: pin IFAMP2OUT						
$V_{o(max)(p)}$	maximum output voltage (peak value)		1.2	1.5	–	V
R_o	output resistance		270	330	390	Ω
C_o	output capacitance		–	5	7	pF
FM demodulator and level detector; see Figs 6 and 7						
FM DEMODULATOR						
FM limiter inputs: pins FMLIMIN and FMLIMDEC						
R_i	input resistance		10	12	14	kΩ
C_i	input capacitance		–	5	7	pF
$V_{start(lim)(rms)}$	start of limiting of RDS MPX output voltage (RMS value)	α_{AF} = –3 dB; R_{gen} = 165 Ω	–	10	15	μV
$V_{o(sens)(rms)}$	sensitivity for RDS MPX output voltage (RMS value)	Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs				
		R_{gen} = 165 Ω; (S+N)/N = 26 dB	–	10	15	μV
		(S+N)/N = 46 dB	–	50	75	μV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{start(lim)(rms)}$	start of limiting of FM MPX output voltage (RMS value)	α_{AF} = –3 dB; R_{gen} = 165 Ω	–	10	15	µV
$V_{o(sens)(rms)}$	sensitivity for FM MPX output voltage (RMS value)	Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs				
		R_{gen} = 165 Ω; (S+N)/N = 26 dB	–	10	15	µV
		(S+N)/N = 46 dB	–	50	75	µV
RDS MPX output: pin RDSMPX						
$V_{o(rms)}$	RDS MPX output voltage (RMS value)	$V_{FMLIMIN}$ = 20 µV to 1 V				
		Δf = 5 kHz; f_{mod} = 57 kHz	40	50	60	mV
		Δf = 22.5 kHz; f_{mod} = 1 kHz	180	230	280	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; $V_{FMLIMIN}$ = 10 mV	70	73	–	dB
THD	total harmonic distortion	Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; $V_{FMLIMIN}$ = 200 µV to 800 mV	–	0.4	0.75	%
α_{AM}	AM suppression $\frac{V_{o(rms)}}{V_{o(AM)(rms)}}$	FM: Δf = 22.5 kHz; f_{mod} = 1 kHz; AM: m = 0.3; f_{mod} = 1 kHz; de-emphasis = 75 µs				
		$V_{FMLIMIN}$ = 30 to 70 µV	20	30	–	dB
		$V_{FMLIMIN}$ = 70 to 500 µV	30	40	–	dB
		$V_{FMLIMIN}$ = 500 µV to 300 mV	50	60	–	dB
		$V_{FMLIMIN}$ = 300 mV to 1 V	30	40	–	dB
$I_{o(max)}$	maximum output current		–	–	100	µA
R_o	output resistance		–	–	500	Ω
R_L	load resistance		20	–	–	kΩ
C_L	load capacitance		–	–	50	pF
B	bandwidth	C_L = 0; R_L > 20 kΩ	200	300	–	kHz
PSRR	power supply ripple rejection	f_{ripple} = 100 Hz to 20 kHz	–	40	–	dB
FM MPX output: pin FMMPX						
$V_{o(rms)}$	FM MPX output voltage (RMS value)	Δf = 22.5 kHz; f_{mod} = 1 kHz; $V_{FMLIMIN}$ = 20 µV to 1 V	180	230	280	mV
		data byte 4 = X010X110; Δf = 1.5 kHz; f_{mod} = 1 kHz; $V_{FMLIMIN}$ = 20 µV to 1 V; weather band mode	150	230	310	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; $V_{FMLIMIN}$ = 10 mV	66	70	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD	total harmonic distortion	Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; $V_{FMLIMIN}$ = 200 µV to 800 mV	–	0.4	0.75	%
α_{AM}	AM suppression $\frac{V_{o(rms)}}{V_{o(AM)(rms)}}$	FM: Δf = 22.5 kHz; f_{mod} = 1 kHz; AM: m = 0.3; f_{mod} = 1 kHz; de-emphasis = 75 µs				
		$V_{FMLIMIN}$ = 30 to 70 µV	20	30	–	dB
		$V_{FMLIMIN}$ = 70 to 500 µV	30	40	–	dB
		$V_{FMLIMIN}$ = 500 µV to 300 mV	50	60	–	dB
		$V_{FMLIMIN}$ = 300 mV to 1 V	30	40	–	dB
$I_{o(max)}$	maximum output current		–	–	100	µA
$R_{o(max)}$	maximum output resistance		–	–	500	Ω
$R_{L(min)}$	minimum load resistance		20	–	–	kΩ
$C_{L(max)}$	maximum load capacitance		–	–	50	pF
B	bandwidth	C_L = 0; R_L > 20 kΩ	200	–	–	kHz
PSRR	power supply ripple rejection	f_{ripple} = 100 Hz to 20 kHz	–	40	–	dB
t_{sw}	AM to FM switching time	$V_{FMLIMIN}$ = 100 µV	–	100	150	ms
FM MPX SOFT MUTE						
Soft mute						
α_{mute}	mute attenuation	$V_{FMLIMIN}$ = 10 mV; V_{TMUTE} = 300 mV				
		data byte 7 = XX000100	–	7	–	dB
		data byte 7 = XX001100	–	8	–	dB
		data byte 7 = XX010100	–	9.5	–	dB
		data byte 7 = XX011100	–	11	–	dB
		data byte 7 = XX100100	–	14	–	dB
		data byte 7 = XX101100	–	18	–	dB
		data byte 7 = XX110100	–	25	–	dB
		data byte 7 = XX111100	–	39	–	dB
$\alpha_{mute(off)}$	mute off	$V_{FMLIMIN}$ = 10 mV; V_{TMUTE} = 300 mV; data byte 7 = XXXXX111	–1	0	+1	dB
$V_{offset(DC)}$	DC offset created by soft mute on pin FMMPX $\Delta V = V_{muted} - V_{notmuted}$		–150	–	+150	mV

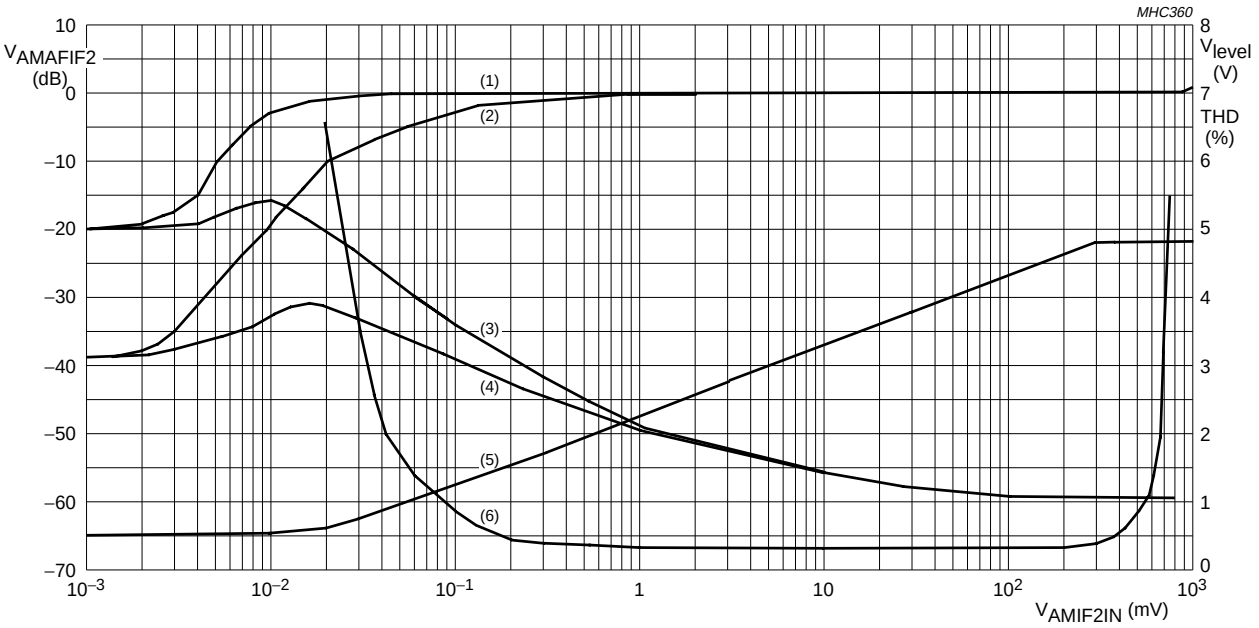
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input: pin TMUTE						
V_{TMUTE}	mute voltage	$V_{FMLIMIN}$ = 0 to 1 V	0	–	5	V
V_{offset}	voltage offset with V_{level}	$V_{FMLIMIN}$ = 0 to 1 V	–200	–	+200	mV
I_{dch}	discharge current	$V_{level} < V_{TMUTE}$	2.5	3.5	4.5	µA
I_{ch}	charge current	$V_{level} > V_{TMUTE}$	–4.5	–3.5	–2.5	µA
$V_{TMUTE(start)}$	mute start voltage	α_{mute} = 3 dB; $V_{FMLIMIN}$ = 10 mV				
		data byte 7 = XX111000	300	450	600	mV
		data byte 7 = XX111001	400	550	700	mV
		data byte 7 = XX111010	450	630	810	mV
		data byte 7 = XX111011	520	720	920	mV
		data byte 7 = XX111100	580	800	1020	mV
		data byte 7 = XX111101	640	890	1140	mV
		data byte 7 = XX111110	680	980	1280	mV
Output: pin V_{level}						
R_o	output resistance of level output		–	–	500	Ω
RR	ripple rejection of level output	f_{ripple} = 100 Hz; $V_{DDA1(ripple)}$ = 100 mV (RMS)	–	40	–	dB
RDS update; see Figs 10 and 11						
RDS mute						
α_{mute}	muting depth	data byte 3: bit 7 = 1 (mute)	60	80	–	dB
$V_{offset(DC)}$	DC offset during RDS update mute on pin FMMPX $\Delta V = V_{muted} - V_{notmuted}$		–30	–	+30	mV
Capacitor: pin TRDSMUTE						
$V_{TRDSMUTE}$	voltage on pin TRDSMUTE	no mute	–	5.7	–	V
		mute	–	1.1	–	V
I_{dch}	discharge current	V_o = 3 V; data byte 3: bit 7 = 1	24	32	38	µA
I_{ch}	charge current	V_o = 3 V; data byte 3: bit 7 = 0	–38	–32	–24	µA
I_{LI}	input leakage current	mute	–10	–	+10	nA
Output: pin AFHOLD						
$I_{sink(max)}$	maximum sink current	after first bus transmission with data byte 1: bit 7 = 1 (start of RDS update); V_o = 0.5 V	1.0	1.2	1.4	mA
Output: pin AFSAMPLE						
$I_{sink(max)}$	maximum sink current	no RDS update in progress; V_o = 0.5 V	1.0	1.2	1.4	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Demodulator AFC						
OUTPUT: PIN RDSMPX						
G_{AFC}	AFC gain on V_{RDSMPX} $\frac{\Delta V_{o(AFC)(disabled)}}{\Delta V_{o(AFC)(enabled)}}$	detuning Δf = 100 kHz; $V_{FMLIMIN}$ = 1 mV	28	32	–	dB
$V_{offset(DC)}$	residual DC offset	L_{demod} = typical value				
		$V_{FMLIMIN}$ = 10 to 80 μV	–	0.1	1	V
		$V_{FMLIMIN}$ = 80 μV to 800 mV	–	10	30	mV
		L_{demod} = ±6%				
		$V_{FMLIMIN}$ = 10 to 80 μV	–	0.240	1	V
		$V_{FMLIMIN}$ = 80 μV to 800 mV	–	25	500	mV
CAPACITOR: PIN C_{AFC}						
I_{dch}	AFC time constant discharge current	V_i = 1.4 to 4.1 V	90	120	150	μA
I_{ch}	AFC time constant charge current	V_i = 1.4 to 4.1 V	–150	–120	–90	μA
FM IF level detector: pin V_{level}						
V_{level}	level output DC voltage	$V_{FMLIMIN}$ = 10 μV to 1 V	0	–	5	V
		$V_{FMLIMIN}$ < 1 μV; standard setting of level DAA	0.1	0.35	0.8	V
		$V_{FMLIMIN}$ = 1 mV; standard setting of level DAA	1.4	2	2.4	V
ΔV_{level}	step size of level starting point adjustment	standard setting of level slope; $V_{FMLIMIN}$ = 1 to 300 mV	40	53	70	mV
$V_{level(slope)}$	slope of level voltage $\frac{\Delta V_{level}}{\Delta V_{FMLIMIN}}$	standard setting of level slope	800	1000	1200	$\frac{mV}{20\ dB}$
ΔV_{step}	level slope adjust step size	$V_{FMLIMIN}$ = 1 mV	55	75	95	$\frac{mV}{20\ dB}$
$\Delta V_{level(T)}$	level voltage variation with temperature $\frac{\Delta V_{level}}{V_{level} \times \Delta T}$	$V_{FMLIMIN}$ = 1 mV	-10^{-3}	–	$+10^{-3}$	K^{-1}
B_{level}	bandwidth of level output voltage	$V_{FMLIMIN}$ = 10 mV; standard setting of DAA	200	300	–	kHz
I_{source}	output source current		–	–	–300	μA
I_{sink}	output sink current		50	–	–	μA
R_o	output resistance		–	–	500	Ω
RR	ripple rejection	f_{ripple} = 100 Hz; $V_{DDA1(ripple)}$ = 100 mV (RMS)	–	40	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Weather band mode						
WEATHER BAND FLAG: PIN T1AMAGC						
$I_{L(max)}$	maximum load current		–5	–	+5	µA
$V_{o(FM)(max)}$	maximum output voltage for FM mode		0	–	0.5	V
$V_{o(WB)}$	output voltage for weather band mode		5.1	6	6.9	V
WEATHER BAND SWITCH OUTPUT: PIN WBSW						
$I_{L(max)}$	maximum load current		–1000	–	–	µA
$R_{int(shunt)}$	internal shunt resistance to ground		–	–	50	kΩ
$V_{o(FM)(max)}$	maximum output voltage for FM mode		0	–	0.35	V
$V_{o(WB)}$	output voltage for weather band mode		4	–	5	V

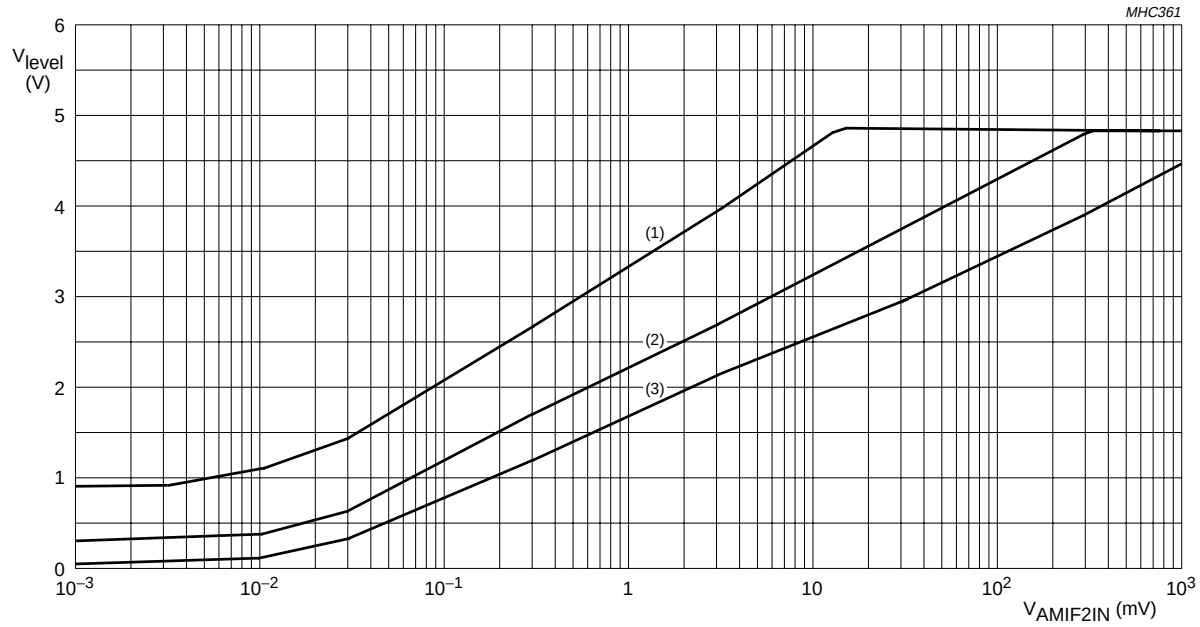
Notes

1. DAA conversion gain formula: $V_{DAAOUT} = \left[2 \times \left(0.75 \times \frac{n}{128} + 0.25\right) \times (V_{DAAIN} + V_{DAATD})\right] - V_{DAATD}$; where n = 0 to 127.
2. Pin FREF: R_{ext} = 68 kΩ connected to ground activates the 2nd I^2C-bus address.
3. The AM AGC transconductance buffer delivers a sink current which is proportional to the voltage at pin T1AMAGC.



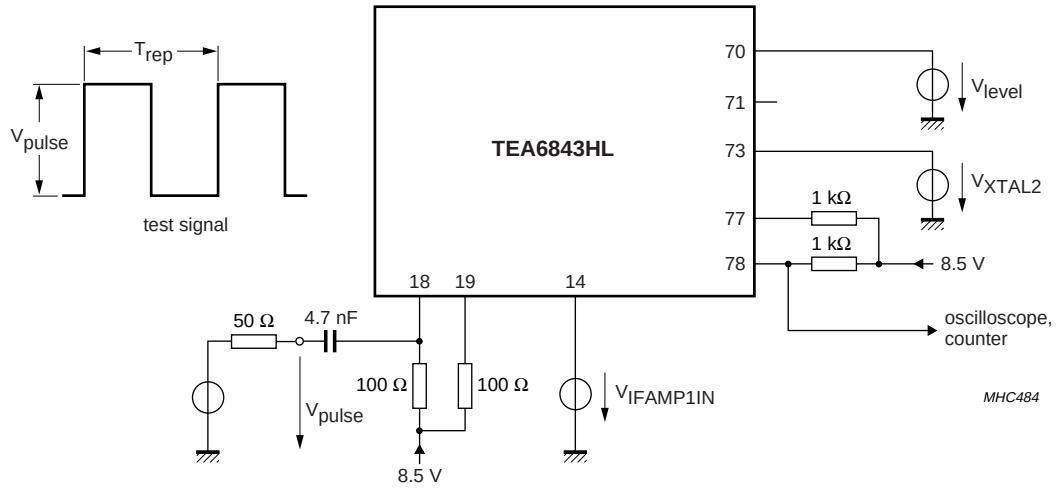
(1) Output voltage at AM audio output: m = 0.3; f_{mod} = 1 kHz; soft mute off.
(2) Output voltage at AM audio output: m = 0.3; f_{mod} = 1 kHz; soft mute on.
(3) Noise voltage at AM audio output: unweighted B = 2.5 kHz; soft mute off.
(4) Noise voltage at AM audio output: unweighted B = 2.5 kHz; soft mute on.
(5) Level detector output voltage for standard setting of level DAA.
(6) THD of AM audio output voltage: m = 0.8; f_{mod} = 1 kHz.

Fig.3 AM detector and level output.



(1) Level DAA setting byte 6 = FFH.
(2) Level DAA setting byte 6 = 84H (standard setting).
(3) Level DAA setting byte 6 = 00H.

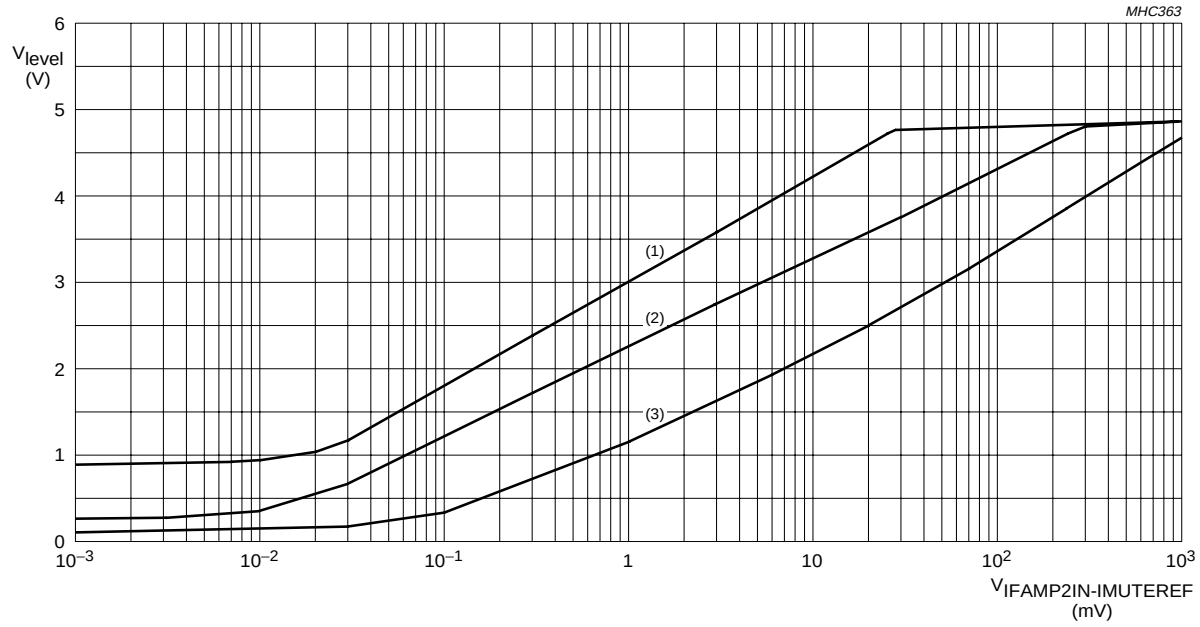
Fig.4 AM level voltage.



Test signal: T_{rep} = 2 ms, t_r < 50 ns, t_f < 50 ns and duty factor 50%.

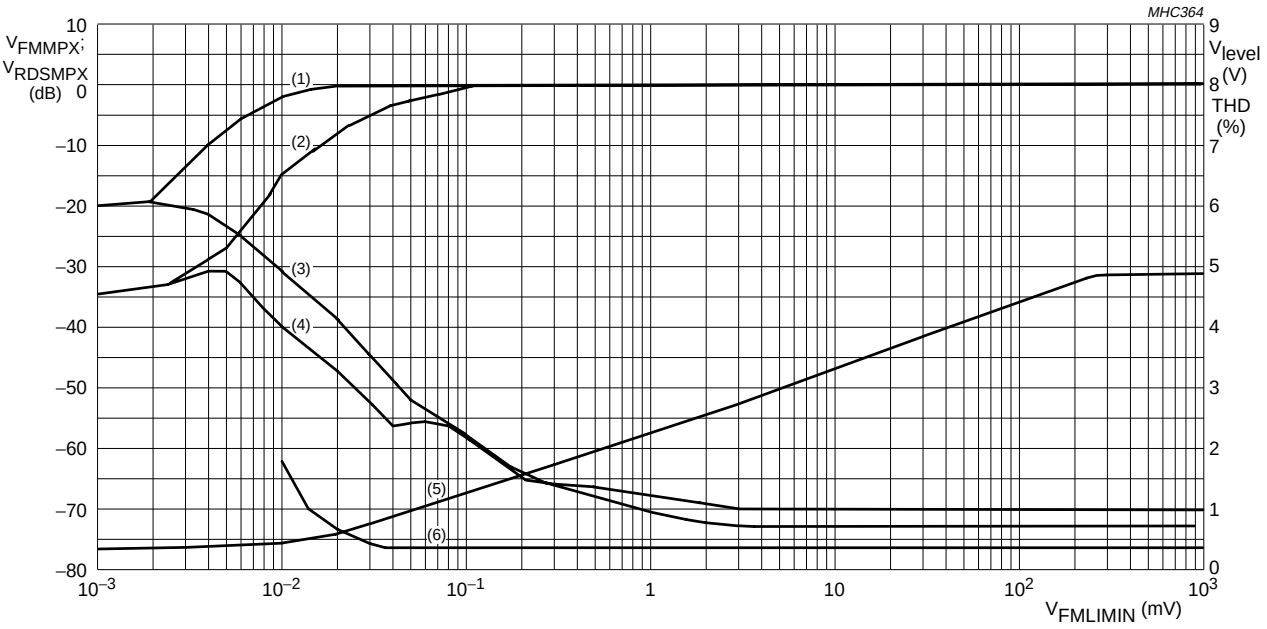
$V_{IFAMP1IN}$ = 4 V.
V_{XTAL2} = 3 V.

Fig.5 Test circuit for AM noise blanker.



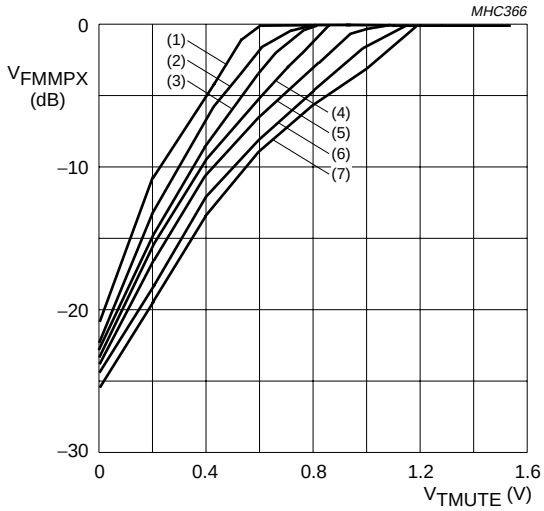
(1) Level DAA setting byte 6 = FFH.
(2) Level DAA setting byte 6 = 84H (standard setting).
(3) Level DAA setting byte 6 = 00H.

Fig.6 FM level voltage.



(1) Output voltage for not muted RDSMPX: Δf = 22.5 kHz; f_{mod} = 1 kHz.
(2) Output voltage for muted FMMPX: Δf = 22.5 kHz; f_{mod} = 1 kHz.
(3) Noise voltage at not muted RDSMPX: unweighted B = 250 Hz to 15 kHz with de-emphasis 75 μs.
(4) Noise voltage at muted FMMPX: unweighted B = 250 Hz to 15 kHz with de-emphasis 75 μs.
(5) Level voltage for standard setting of level DAA; data byte 6 = 84H.
(6) THD of FMMPX and RDSMPX: Δf = 22.5 kHz; f_{mod} = 1 kHz.

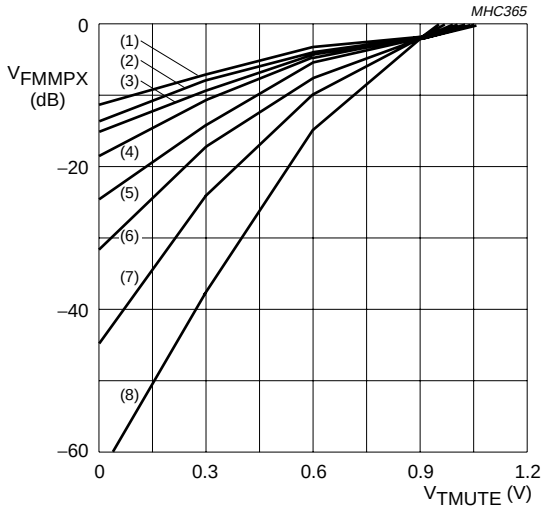
Fig.7 (S+N)/N, THD and level voltage for FM mode as a function of FM demodulator input voltage.



Mute start:
(1) MD[2:0] = 000.
(2) MD[2:0] = 001.
(3) MD[2:0] = 010.
(4) MD[2:0] = 011.
(5) MD[2:0] = 100.
(6) MD[2:0] = 101.
(7) MD[2:0] = 110.

Mute start adjustment range, mute slope = 100 and $V_{FMLIMIN}$ = 10 mV.

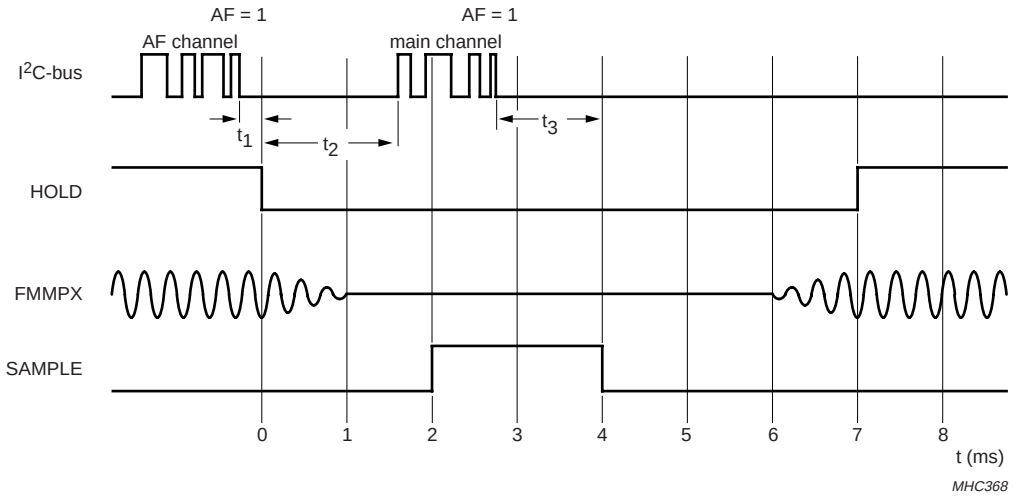
Fig.8 Adjustment of soft mute start.



Mute slope:
(1) MS[2:0] = 000.
(2) MS[2:0] = 001.
(3) MS[2:0] = 010.
(4) MS[2:0] = 011.
(5) MS[2:0] = 100.
(6) MS[2:0] = 101.
(7) MS[2:0] = 110.
(8) MS[2:0] = 111.

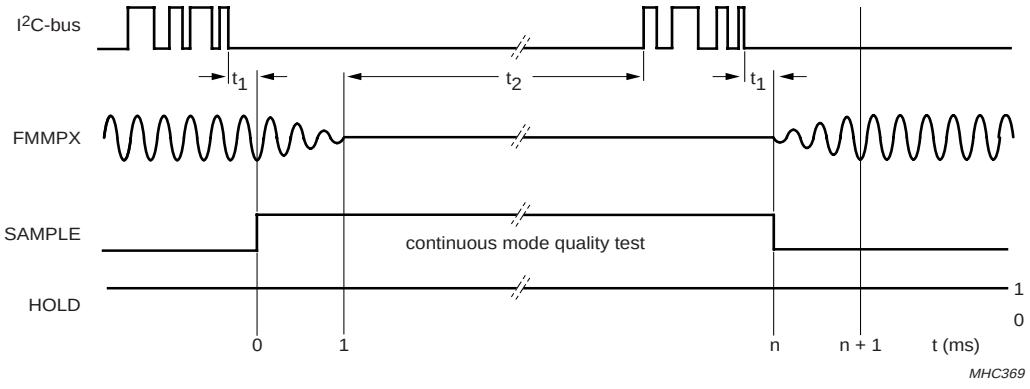
Mute slope adjustment range, mute start = 100 and $V_{FMLIMIN}$ = 10 mV.

Fig.9 Adjustment of soft mute slope.



Hold signal is used to hold the quality information for signal processing of the main channel during the alternative frequency jumps.
Quality measurement can be carried out during sample = 1.
t_1 is the internal clock related logic delay of 100 µs.
t_2 should be >1.1 ms to ensure correct loading of PLL for the main channel.
t_3 should be >0 to ensure inaudible update; $t_3 < 0$ extends the mute period.

Fig.10 Inaudible RDS update timing diagram.



t_1 is the internal clock related logic delay of 100 µs.
t_2 should be larger than the required PLL tuning time for the given band: FM = 1 ms and AM = 20 ms.

Fig.11 Preset mode timing diagram.

12 I²C-BUS PROTOCOL

12.1 I²C-bus specification

The standard I²C-bus specification is expanded by the following definitions.

IC addresses:

- 1st IC address C2H: 1100001 R/$\overline{W}$
- 2nd IC address C0H: 1100000 R/$\overline{W}$.

A second I²C-bus address can be selected by connecting pin FREF via a 68 kΩ resistor to GND.

Structure of the I²C-bus logic: slave transceiver with auto increment.

Subaddresses are not used.

Remark: The I²C-bus operates at a maximum clock rate of 100 kHz. It is not allowed to connect the IC to an I²C-bus operating at a higher clock rate. Maximum LOW level is 1.5 V and minimum HIGH level is 3 V.

12.1.1 DATA TRANSFER

Data sequence: address, byte 1, byte 2, byte 3, byte 4, byte 5, byte 6 and byte 7. The data transfer has to be in this order. The LSB = 0 indicates a WRITE operation to the TEA6843HL.

Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.

The data becomes valid at the output of the internal latches with the acknowledge of each byte. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, this byte is lost and the previous information is available.

In byte 5, 4 bits are reserved for test mode purposes. The state of the test bits, if not in test mode, is don't care.

12.1.2 I²C-BUS PULL-UP RESISTORS

When the IC is used together with the TEA688x or TEF689x and both SCL and SDA lines are connected via the I²C-bus to the TEA688x or TEF689x, the pull-up resistors of the tuner IC should be connected to the digital supply voltage of the TEA688x or TEF689x. Otherwise an I²C-bus pull-down can occur switching off the tuner IC supply when the I²C-bus buffer interface of the TEA688x or TEF689x is enabled for data transfer to the tuner IC.

12.1.3 FREQUENCY SETTING

For new frequency setting, in both AM and FM mode, the programmable divider is enabled by setting bit MUTE = 1. To select an FM frequency, two I²C-bus transmissions are necessary:

- First: bit MUTE = 1
- Second: bit MUTE = 0.

12.1.4 DEFAULT SETTINGS

No default settings at power-on reset. One I²C-bus transmission is required to program the IC.

12.2 I²C-bus protocol

12.2.1 DATA TRANSFER MODE AND IC ADDRESS

Table 1 Write mode

S[1]	address (write)	A[2]	data byte(s)	A[2]	P[3]

Notes

1. S = START condition.
2. A = acknowledge.
3. P = STOP condition.

Table 2 Read mode

S[1]	address (read)	A[2]	data byte 1

Notes

1. S = START condition.
2. A = acknowledge.

Table 3 IC address byte

IC ADDRESS							MODE
1	1	0	0	0	0	0/1[1]	R/$\overline{W}$[2]

Notes

1. Defined by address pin FREF:
   a) 1 = 1st IC address
   b) 0 = 2nd IC address.
2. Read or write mode:
   a) 0 = write operation to TEA6843HL
   b) 1 = read operation from TEA6843HL.

12.2.2 WRITE MODE: DATA BYTE 1

Table 4 Format of data byte 1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AF	PLL14	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 5 Description of data byte 1 bits

BIT	SYMBOL	DESCRIPTION
7	AF	**Alternative frequency.** If AF = 0, then normal operation. If AF = 1, then AF (RDS) update mode.
6 to 0	PLL[14:8]	**Setting of programmable counter of synthesizer PLL.** Upper byte of PLL divider word.

12.2.3 WRITE MODE: DATA BYTE 2

Table 6 Format of data byte 2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 7 Description of data byte 2 bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PLL[7:0]	**Setting of programmable counter of synthesizer PLL.** Lower byte of PLL divider word.

12.2.4 WRITE MODE: DATA BYTE 3

Table 8 Format of data byte 3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MUTE	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0

Table 9 Description of data byte 3 bits

BIT	SYMBOL	DESCRIPTION
7	MUTE	**FM audio mute.** If MUTE = 0, then FM audio not muted. If MUTE = 1, then FM audio muted; writing to programmable divider and antenna DAA enabled.
6 to 0	DAA[6:0]	**Setting of antenna digital auto alignment.**

12.2.5 WRITE MODE: DATA BYTE 4

Table 10 Format of data byte 4

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IFMT	RFS2	RFS1	RFS0	IFPR	BND1	BND0	AMFM

Table 11 Description of data byte 4 bits

BIT	SYMBOL	DESCRIPTION
7	IFMT	**IF measuring time.** If IFMT = 0, then IF measuring time is 20 ms. If IFMT = 1, then IF measuring time is 2 ms.
6 to 4	RFS[2:0]	**Reference frequency for synthesizer.** These 3 bits determine the reference frequency, see Table 12.
3	IFPR	**IF counter prescaler ratio.** If IFPR = 0, then IF prescaler ratio is 100. If IFPR = 1, then IF prescaler ratio is 10.
2 and 1	BND[1:0]	**Band switch.** These 2 bits select in FM mode band and local or distant, see Table 13; in AM mode band select and output of AM IF2 for AM stereo, see Table 14.
0	AMFM	**AM or FM switch.** If AMFM = 0, then FM mode. If AMFM = 1, then AM mode.

Table 12 Reference frequency setting

RFS2	RFS1	RFS0	f_{ref} (kHz)
0	0	0	100
1	0	0	50
0	1	0	25
1	1	0	20
0	0	1	10
1	0	1	10
0	1	1	10
1	1	1	10

Table 13 FM mode

BND1	BND0	SELECTION
0	0	FM standard: dead zone high current charge pump active, FM AGC defined by RF level and threshold level setting by I^2C-bus
0	1	FM local: dead zone high current charge pump active, FM AGC source current set to maximum
1	0	FM East Europe: dead zone high current charge pump switched off, current of low current charge pump set to 1 mA
1	1	FM weather band: N1 divider set to 1 and I and Q phase shift network switched on, WX flag signal activated

Table 14 AM mode; note 1

BND1	BND0	SELECTION
0	0	AM mono; N2 divider set to 5 (SW)
0	1	AM stereo; N2 divider set to 5 (SW)
1	0	AM mono; N2 divider set to 10 (LW, MW)
1	1	AM stereo; N2 divider set to 10 (LW, MW)

Note

1. In AM mode dead zone high current charge pump switched off, current of low current charge pump set to 1 mA.

12.2.6 WRITE MODE: DATA BYTE 5

Table 15 Format of data byte 5

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
KAGC	WBA1	WBA0	AMSM	TMS3	TMS2	TMS1	TMS0

Table 16 Description of data byte 5 bits

BIT	SYMBOL	DESCRIPTION
7	KAGC	**Keyed FM AGC.** If KAGC = 0, then keyed FM AGC is off. If KAGC = 1, then keyed FM AGC is on.
6 and 5	WBA[1:0]	**Wideband AGC.** These 2 bits set the start value of wideband AGC. For AM, see Table 17 and for FM, see Table 18.
4	AMSM	**AM soft mute.** If AMSM = 0, then AM soft mute is off. If AMSM = 1, then AM soft mute is on (default).
3	TMS3	**In test mode charge pump 3-state.** If TMS3 = 0, then 3-state off. If TMS3 = 1, then 3-state on.
2	TMS2	**In test mode external clock for level and antenna DAA.** If TMS2 = 0, then external clock disabled. If TMS2 = 1, then external clock enabled.
1 and 0	TMS[1:0]	**In test mode setting of pin FREF.** These 2 bits define the function of pin FREF, see Table 19.

Table 17 Setting of wideband AGC for AM

WBA1	WBA0	AM MIXER 1 INPUT VOLTAGE (PEAK VALUE) (mV)
0	0	375
0	1	500
1	0	625
1	1	750

Table 18 Setting of wideband AGC for FM

WBA1	WBA0	FM RF MIXER INPUT VOLTAGE (RMS VALUE) (mV)
1	1	4
1	0	8
0	1	12
0	0	16

Table 19 Setting function of pin FREF in test mode

TMS1	TMS0	OUTPUT AT PIN FREF
0	0	reference frequency of TEA688x or TEF689x
0	1	tuner oscillator frequency divided by division ratio of programmable divider
1	0	PLL synthesizer reference frequency
1	1	not used (no output)

12.2.7 WRITE MODE: DATA BYTE 6

Table 20 Format of data byte 6

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0

Table 21 Description of data byte 6 bits

BIT	SYMBOL	DESCRIPTION
7 to 3	LST[4:0]	**Setting of level DAA starting point.** These 5 bits determine the offset of the level detector output voltage.
2 to 0	LSL[2:0]	**Setting of level DAA slope.** These 3 bits determine the steepness of the level detector output voltage.

Table 22 Standard setting of data byte 6 bits

SETTING OF LEVEL DAA STARTING POINT					SETTING OF LEVEL DAA SLOPE		
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0
1	0	0	0	0	1	0	0

12.2.8 WRITE MODE: DATA BYTE 7

Table 23 Format of data byte 7

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	MS2	MS1	MS0	MD2	MD1	MD0

Table 24 Description of data byte 7 bits

BIT	SYMBOL	DESCRIPTION
7 and 6	–	These bits are not used and must be set to logic 0.
5 to 3	MS[2:0]	**Setting of soft mute slope;** see Fig.9.
2 to 0	MD[2:0]	**Setting of soft mute start;** see Fig.8.

12.2.9 READ MODE: DATA BYTE 1

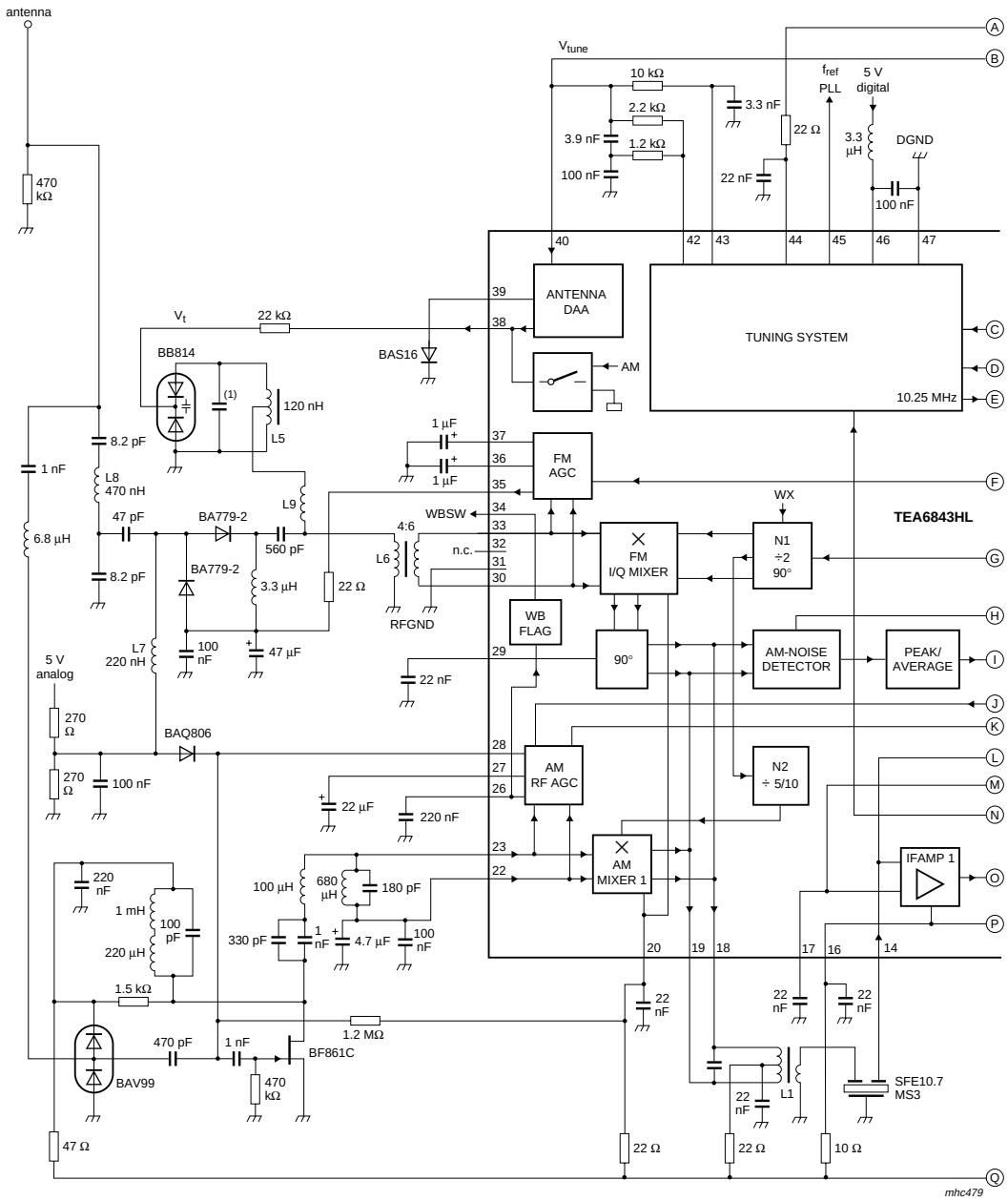
Table 25 Format of 1st data byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IFC7	IFC6	IFC5	IFC4	IFC3	IFC2	IFC1	IFC0

Table 26 Description of data byte 1 bits

BIT	SYMBOL	DESCRIPTION
7 to 0	IFC[7:0]	**IF counter result.** These bits contain the last eight bits of the IF counter result.

13 TEST AND APPLICATION INFORMATION



For list of components see Table 27.

(1) 1 to 5 pF trimmer without DAA.

Fig.12 Application diagram (continued in Fig.13).

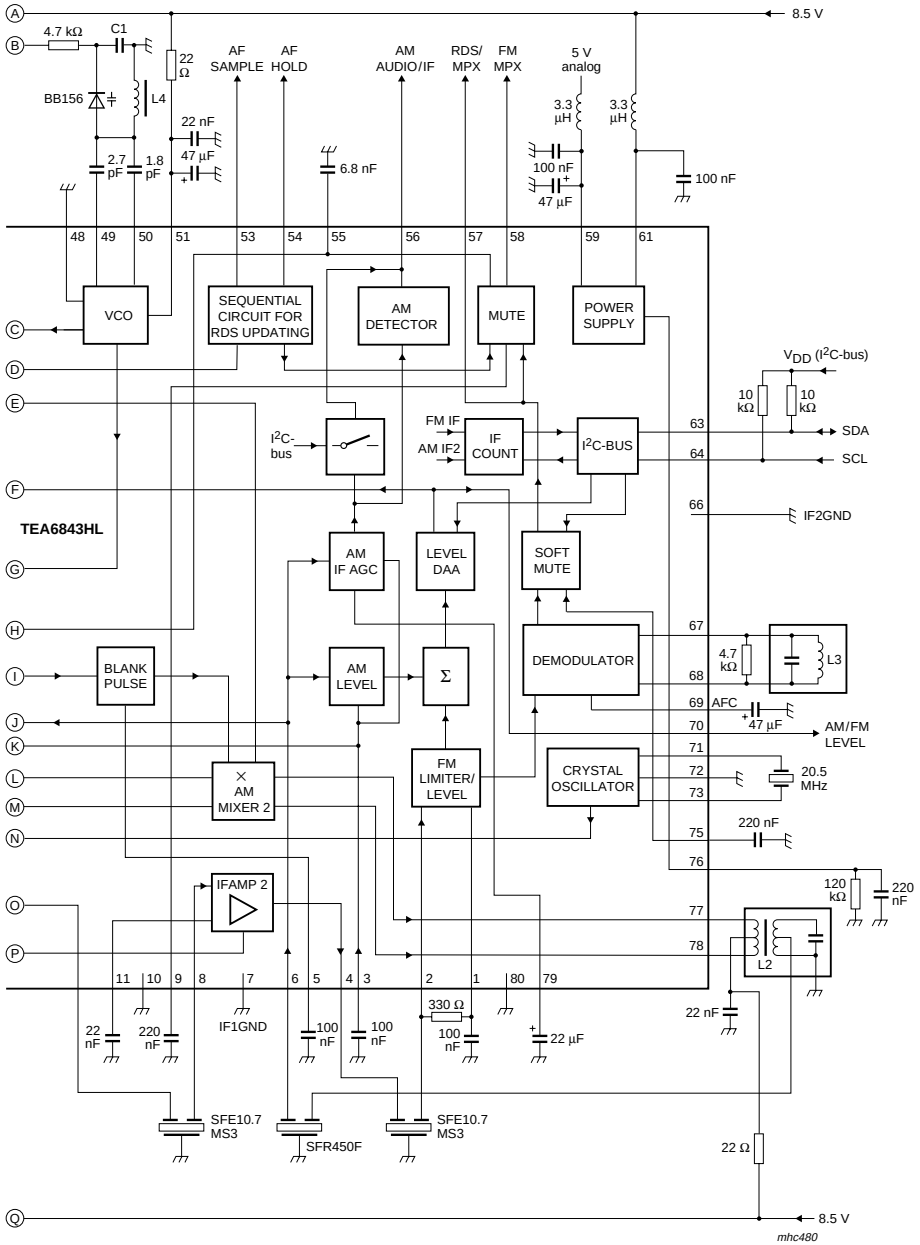
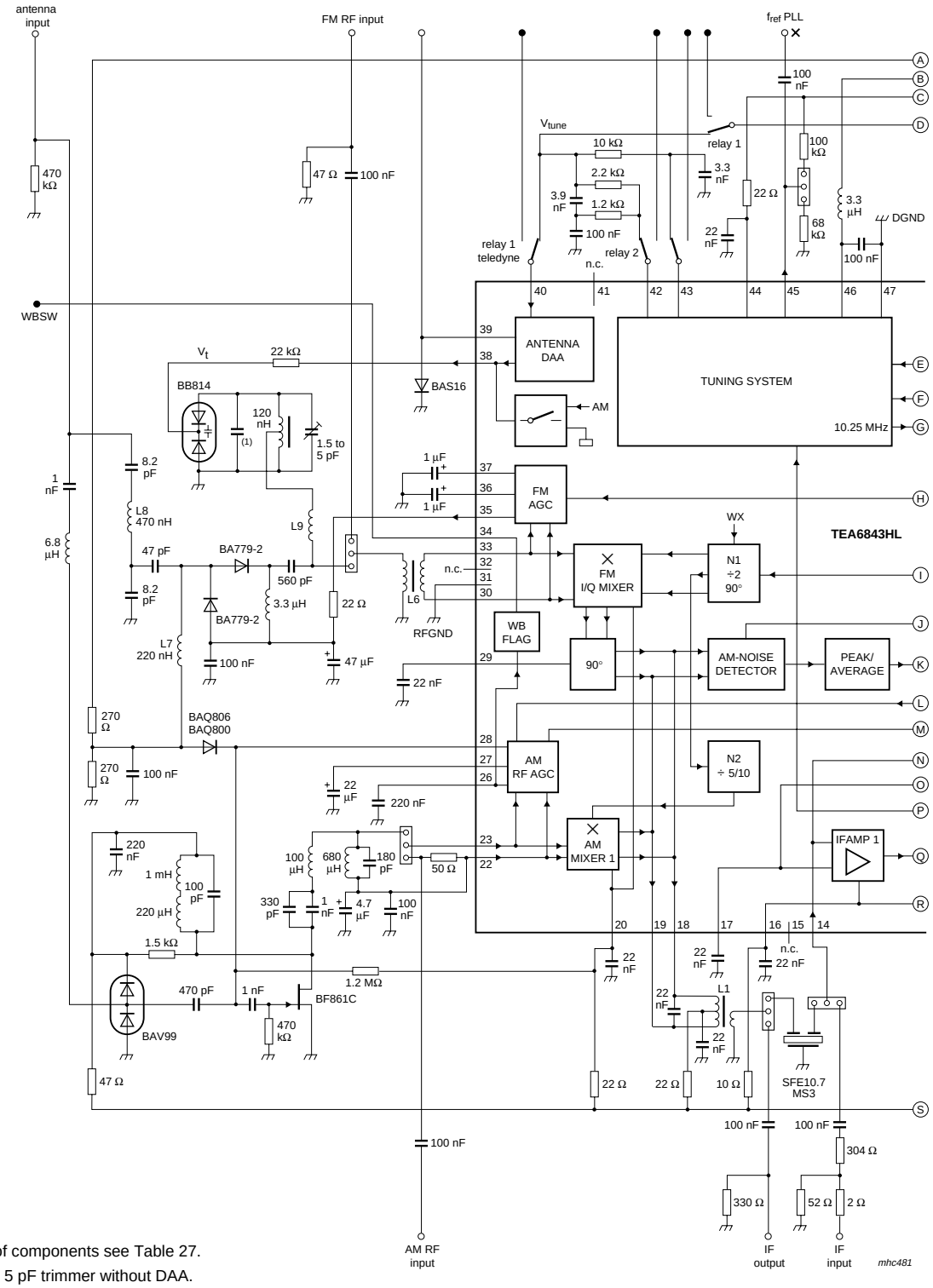


Fig.13 Application diagram (continued from Fig.12).



For list of components see Table 27.

(1) 1 to 5 pF trimmer without DAA.

Fig.14 Test circuit (continued in Fig.15).

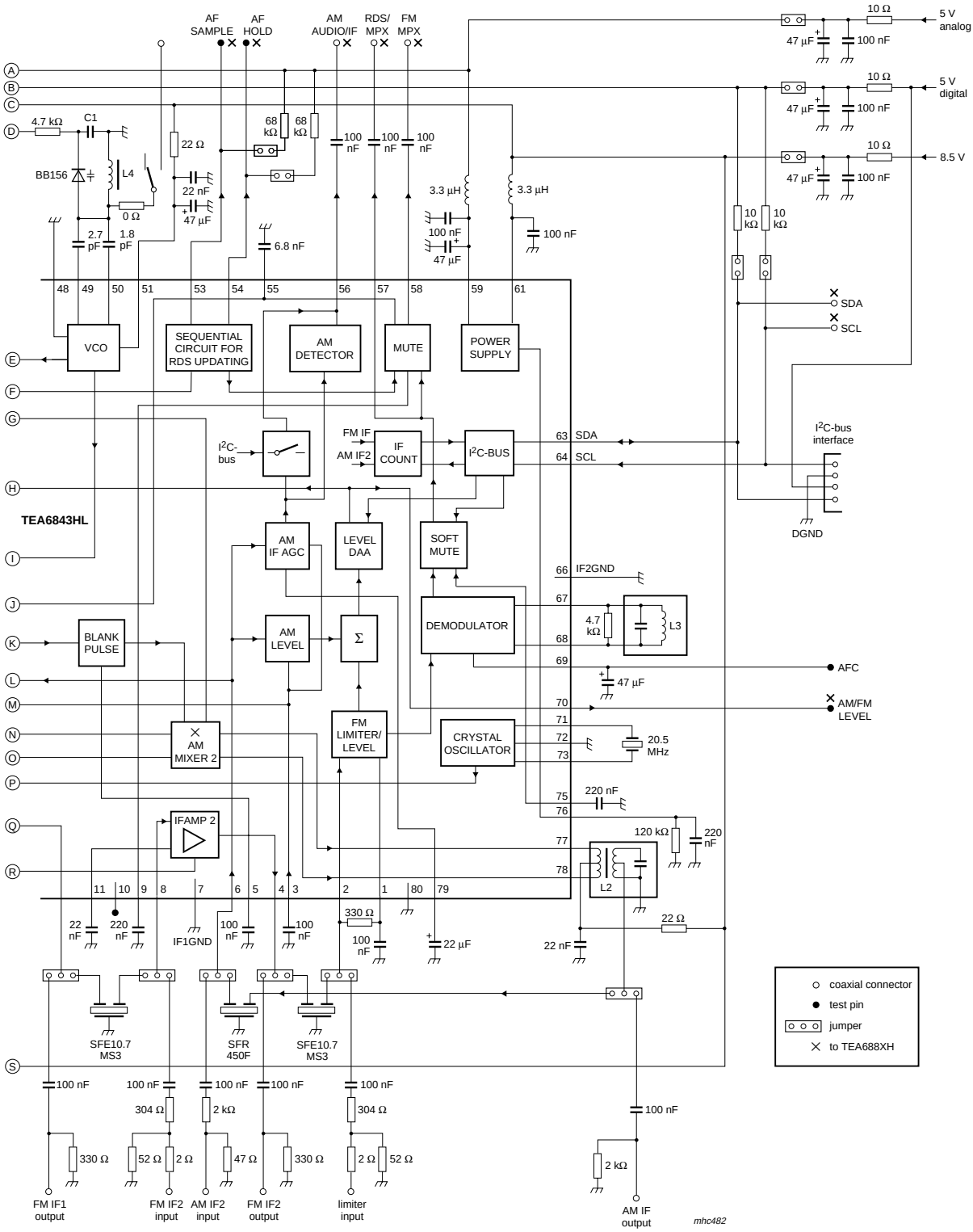


Fig.15 Test circuit (continued from Fig.14).

Table 27 List of components

SYMBOL	PARAMETER	TYPE	MANUFACTURER
C1	capacitor for VCO tuning	270 pF; type NP0	–
L1	10.7 MHz IF coil	P7 PSG P826RC 5134N=S	TOKO
L2	450 kHz IF coil	P7PSGAE-5078D=S	TOKO
L3	10.7 MHz demodulator coil	392BC-1977Z	TOKO
L4	oscillator coil	E543SNAS-02010	TOKO
L5	FM image rejection	611SNS-1066Y	TOKO
L6	FM input transformer	369INS-3076X	TOKO
L7	–	LQN	MURATA
L8	–	LQN	MURATA
L9	–	Air coil	–
–	crystal 20.5 MHz	TQX6238	Tele Quarz

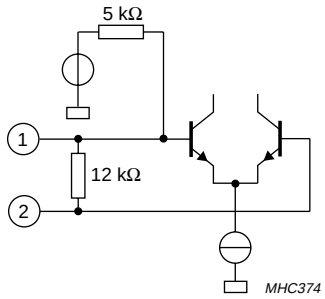
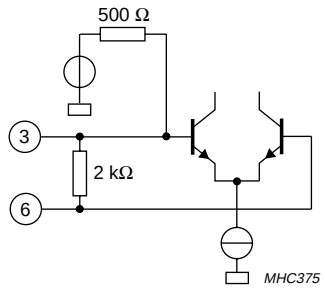
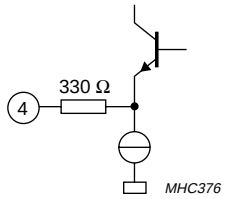
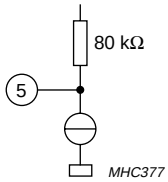
Table 28 DC operating points

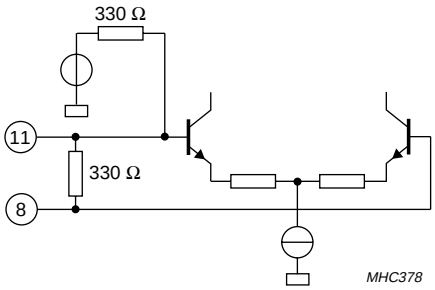
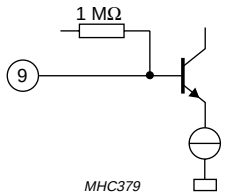
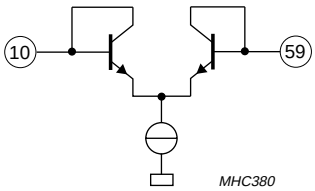
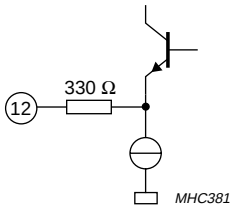
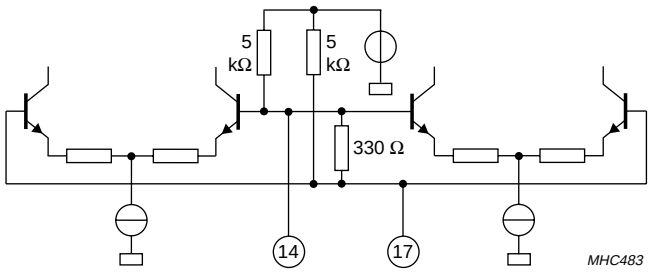
SYMBOL	PIN	UNLOADED DC VOLTAGE (V)					
		AM			FM		
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
FMLIMDEC	1	2.5	3	3.5	2.5	2.8	3.1
FMLIMIN	2	2.5	3	3.5	2.5	2.8	3.1
AMIF2DEC	3	2.4	2.7	3.2	floating		
IFAMP2OUT	4	7.2	7.9	–	3.4	3.9	4.4
AMNBHOLD	5	4.4	4.75	5.25	8	8.4	–
AMIF2IN	6	2.4	2.7	3.2	floating		
IF1GND	7	external 0			external 0		
IFAMP2IN	8	3	3.4	3.8	2.7	3.1	3.5
C_{offset}	9	floating			3	3.5	4
IMUTEREF	10	external biased (ground)			external biased (ground)		
IFAMP2DEC	11	3	3.4	3.8	2.7	3.1	3.5
IFAMP1OUT	12	7.2	7.9	–	3.6	4	4.4
IFAMP1IN	14	2.4	2.8	3.2	2.3	2.7	3.1
V_{DDA1}	16	external 8.5			external 8.5		
IFAMP1DEC	17	2.4	2.8	3.2	2.3	2.7	3.1
MIX1OUT1	18	external 8.5			external 8.5		
MIX1OUT2	19	external 8.5			external 8.5		
V_{DDA2}	20	external 8.5			external 8.5		
AMMIX1IN2	22	2.4	2.85	3.2	floating		
AMMIX1IN1	23	external biased			floating		
T1AMAGC	26	0	2.8	4.6	0 (no WX)	0.3 (no WX)	0.5 (no WX)
T2AMAGC	27	2.5	2.8	3.1	floating		
IAMAGC	28	external biased			external biased		
$V_{ref(FMMIX)}$	29	2.7	3.1	3.4	6.5	7.1	7.9
FMMIXIN1	30	1	1.3	1.6	2.3	2.8	3.3
RFGND	31	external 0			external 0		
FMMIXIN2	33	1	1.3	1.6	2.3	2.8	3.3
WBSW	34	floating			4 (WB)	4.5 (WB)	5 (WB)
					– (FM)	<0.5 (FM)	– (FM)
IFMAGC	35	external biased			1.5 (external biasing)	–	4 (external biasing)
T2FMAGC	36	7.5	8	8.3	3.6	4.2	4.6
T1FMAGC	37	floating			1	–	7
DAAOUT	38	–	0.2	0.3	0.2	–	8.25
DAATD	39	floating			0.2	–	1.5
DAAIN	40	0	–	8.5	0	–	8.5

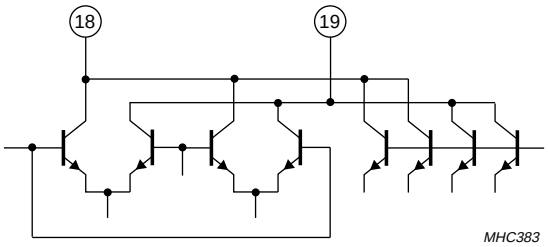
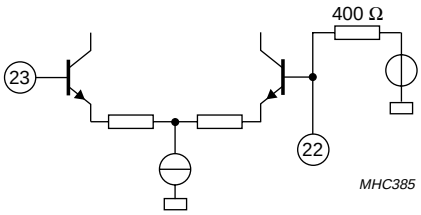
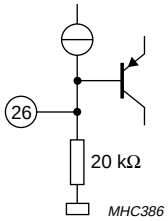
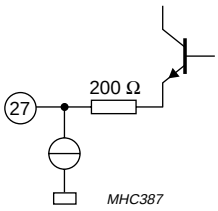
SYMBOL	PIN	UNLOADED DC VOLTAGE (V)					
		AM			FM		
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
V_{tune}	42	0	–	8.5	0	–	8.5
CPOUT	43	0	–	8.5	0	–	8.5
V_{DDA3}	44	external 8.5			external 8.5		
FREF	45	3.2	3.4	3.7	3.2	3.4	3.7
V_{DDD}	46	external 5			external 5		
DGND	47	external 0			external 0		
VCOGND	48	external 0			external 0		
OSCFDB	49	2.2	2.8	3.4	2.2	2.8	3.4
OSCTNK	50	5	6	7	5	6	7
V_{DDA4}	51	external 8.5			external 8.5		
AFSAMPLE	53	0	0.2	0.5	0	0.2	0.5
AFHOLD	54	open-collector			open-collector		
TRDSMUTE	55	1.9	2.2	2.5	0.7 (muted)	1.2 (muted)	1.7 (muted)
					5.2 (not muted)	5.7 (not muted)	6.2 (not muted)
AMAFIF2	56	4	4.3	4.6	floating		
RDSMPX	57	floating			2.6	3.1	3.3
FMMPX	58	floating			3	3.5	4
V_{DDA5}	59	external 5			external 5		
V_{DDA6}	61	external 8.5			external 8.5		
SDA	63	4.8	5	5.2	4.8	5	5.2
SCL	64	4.8	5	5.2	4.8	5	5.2
IF2GND	66	external 0			external 0		
QDET1	67	floating			3.6	4.1	4.6
QDET2	68	floating			3.6	4.1	4.6
C_{AFC}	69	floating			1.2	3.4	4.1
V_{level}	70	0	–	7	0	–	7
XTAL1	71	1.7	2.1	2.5	1.7	2.1	2.5
XTALGND	72	external 0			external 0		
XTAL2	73	1.7	2.1	2.5	1.7	2.1	2.5
TMUTE	75	0	–	5	0	–	5
IREF	76	4	4.25	4.5	4	4.25	4.5
AMMIX2OUT1	77	external 8.5			external 8.5		
AMMIX2OUT2	78	external 8.5			external 8.5		
C_{AGC}	79	4.1	4.4	4.7	4	4.5	5

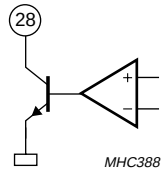
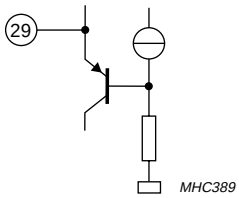
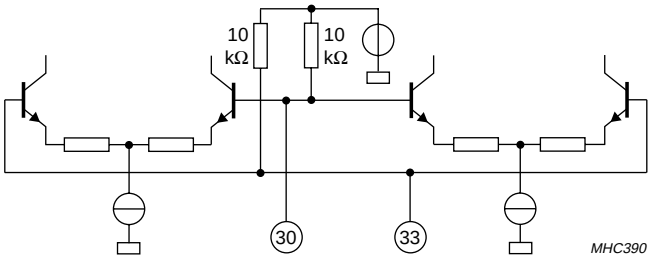
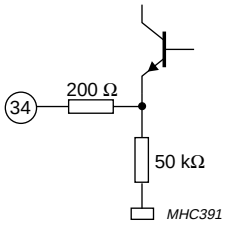
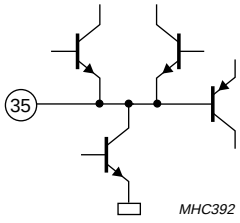
14 INTERNAL CIRCUITRY

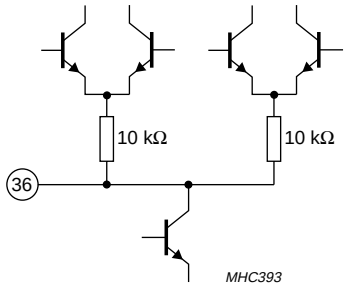
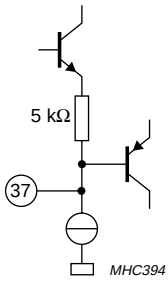
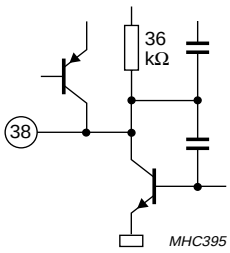
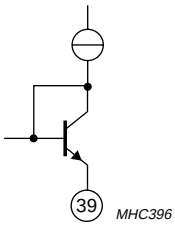
Table 29 Equivalent pin circuits

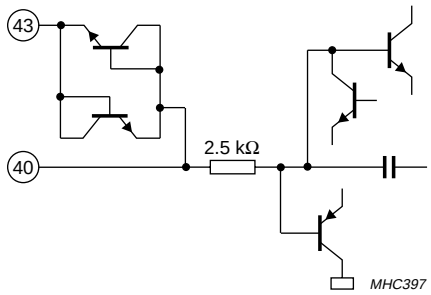
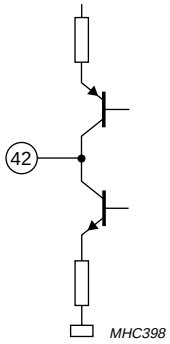
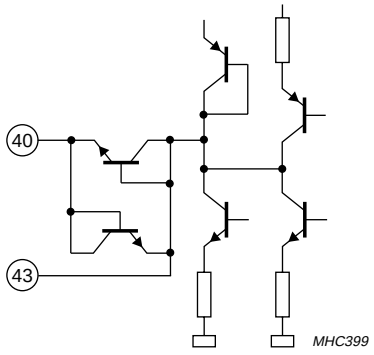
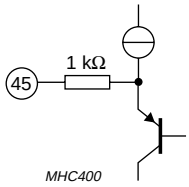
PIN	SYMBOL	EQUIVALENT CIRCUIT
1	FMLIMDEC	
2	FMLIMIN	
3	AMIF2DEC	
6	AMIF2IN	
4	IFAMP2OUT	
5	AMNBHOLD	
7	IF1GND	

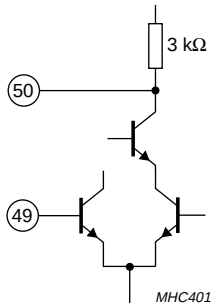
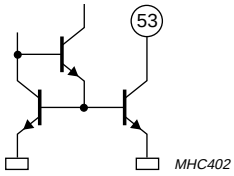
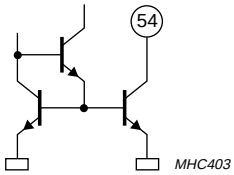
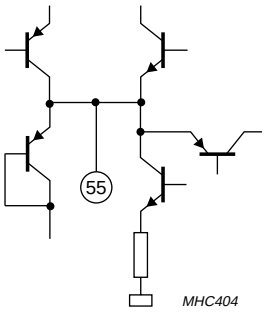
PIN	SYMBOL	EQUIVALENT CIRCUIT
8	IFAMP2IN	
11	IFAMP2DEC	
9	C_{offset}	
10	IMUTEREF	
12	IFAMP1OUT	
13	n.c.	
14	IFAMP1IN	
17	IFAMP1DEC	
15	n.c.	

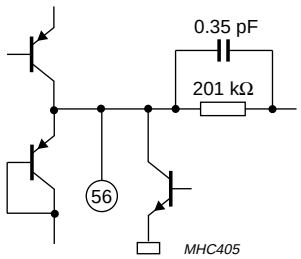
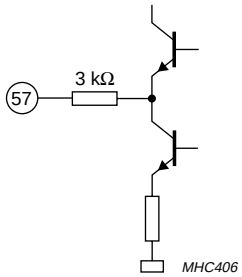
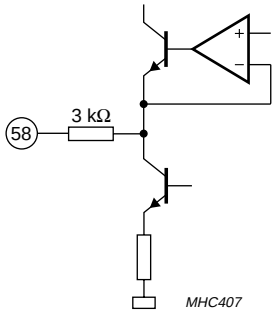
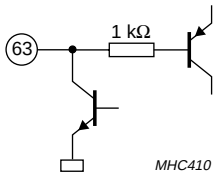
PIN	SYMBOL	EQUIVALENT CIRCUIT
16	V_{DDA1}	
18	MIX1OUT1	
19	MIX1OUT2	
20	V_{DDA2}	
21	n.c.	
22	AMMIX1IN2	
23	AMMIX1IN1	
24	n.c.	
25	n.c.	
26	T1AMAGC	
27	T2AMAGC	

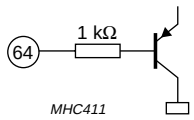
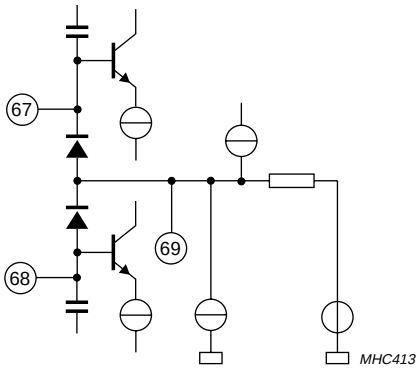
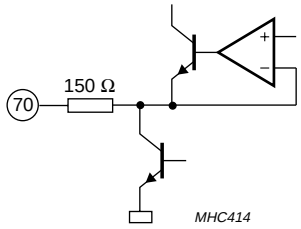
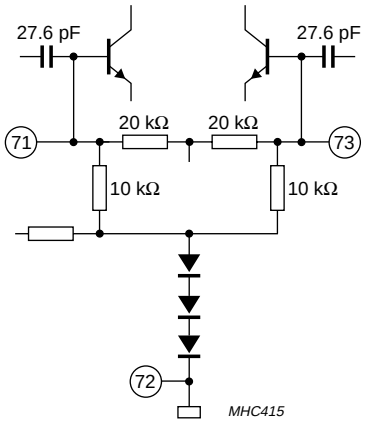
PIN	SYMBOL	EQUIVALENT CIRCUIT
28	IAMAGC	
29	$V_{ref(FMMIX)}$	
30	FMMIXIN1	
33	FMMIXIN2	
31	RFGND	
32	n.c.	
34	WBSW	
35	IFMAGC	

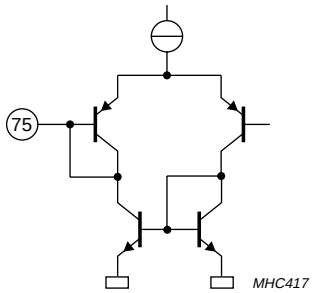
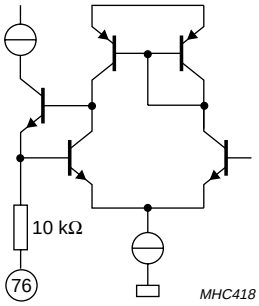
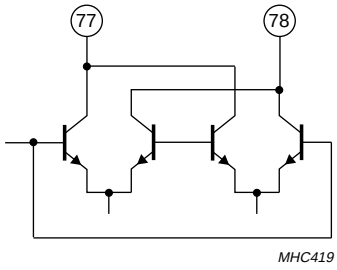
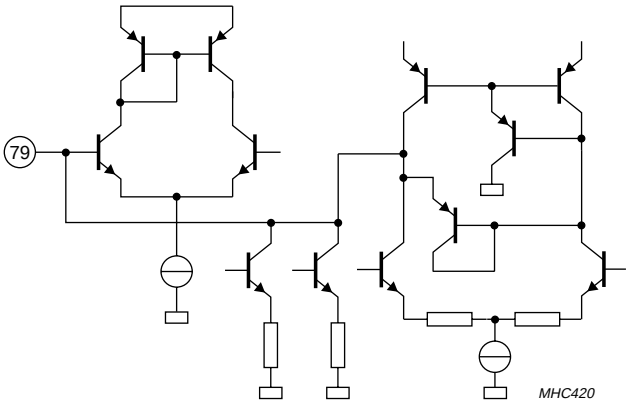
PIN	SYMBOL	EQUIVALENT CIRCUIT
36	T2FMAGC	
37	T1FMAGC	
38	DAAOUT	
39	DAATD	

PIN	SYMBOL	EQUIVALENT CIRCUIT
40	DAAIN	
41	n.c.	
42	V_{tune}	
43	CPOUT	
44	V_{DDA3}	
45	FREF	
46	V_{DDD}	
47	DGND	

PIN	SYMBOL	EQUIVALENT CIRCUIT
48	VCOGND	
49	OSCFDB	
50	OSCTNK	
51	V_{DDA4}	
52	n.c.	
53	AFSAMPLE	
54	AFHOLD	
55	TRDSMUTE	

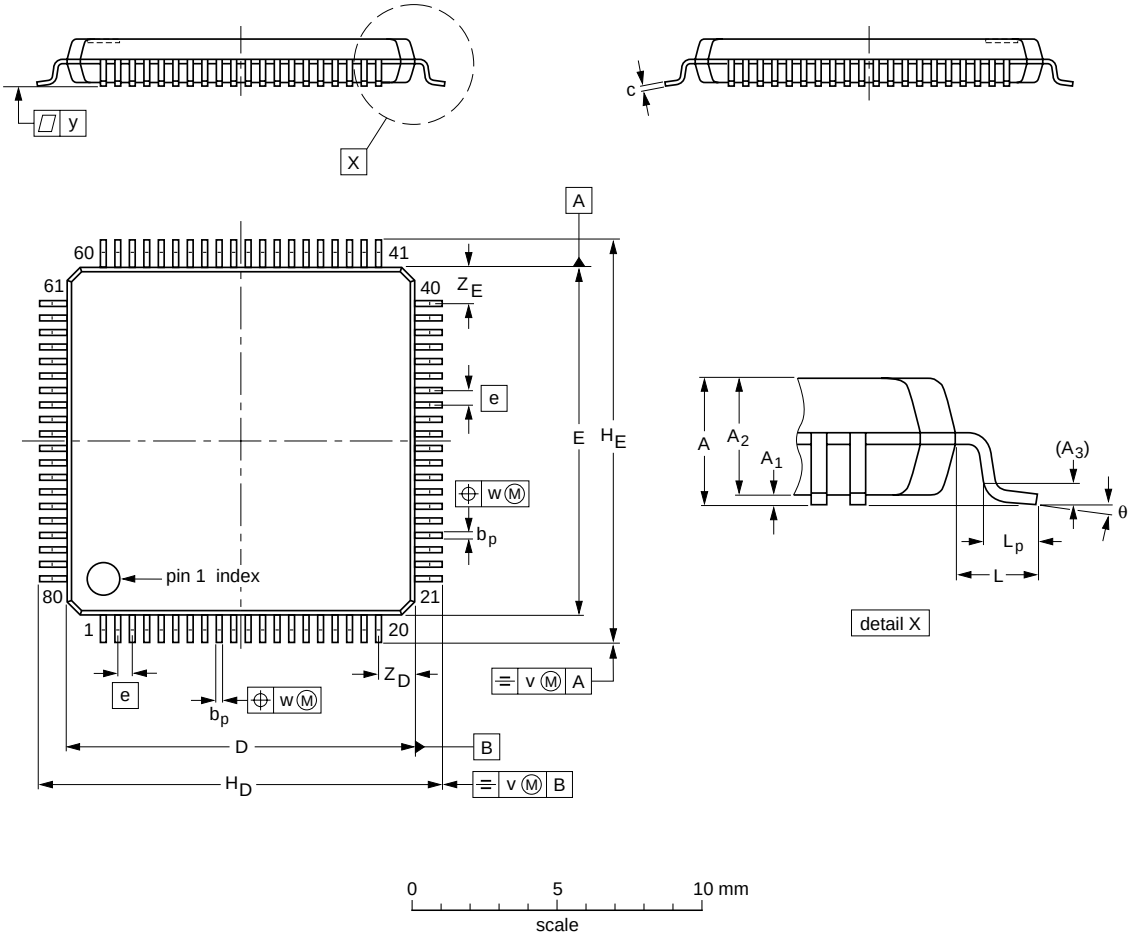
PIN	SYMBOL	EQUIVALENT CIRCUIT
56	AMAFIF2	
57	RDSMPX	
58	FMMPX	
59	V_{DDA5}	
60	n.c.	
61	V_{DDA6}	
62	n.c.	
63	SDA	

PIN	SYMBOL	EQUIVALENT CIRCUIT
64	SCL	
65	n.c.	
66	IF2GND	
67	QDET1	
68	QDET2	
69	C_{AFC}	
70	V_{level}	
71	XTAL1	
72	XTALGND	
73	XTAL2	
74	n.c.	

PIN	SYMBOL	EQUIVALENT CIRCUIT
75	TMUTE	
76	IREF	
77	AMMIX2OUT1	
78	AMMIX2OUT2	
79	C_{AGC}	
80	n.c.	

15 PACKAGE OUTLINE

LQFP80: plastic low profile quad flat package; 80 leads; body 12 x 12 x 1.4 mm **SOT315-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.16 0.04	1.5 1.3	0.25	0.27 0.13	0.18 0.12	12.1 11.9	12.1 11.9	0.5	14.15 13.85	14.15 13.85	1	0.75 0.30	0.2	0.15	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT315-1	136E15	MS-026				~~00-01-19~~ 03-02-25

16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar or manual soldering is suitable for PMFP packages.

17 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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