

# 74HC245

## Octal 3-State Noninverting Bus Transceiver

### High-Performance Silicon-Gate CMOS

The 74HC245 is identical in pinout to the LS245. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

The HC245 is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

#### Features

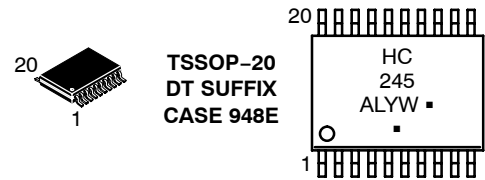
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 308 FETs or 77 Equivalent Gates
- This is a Pb-Free Device



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#### MARKING DIAGRAMS



HC245 = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# 74HC245

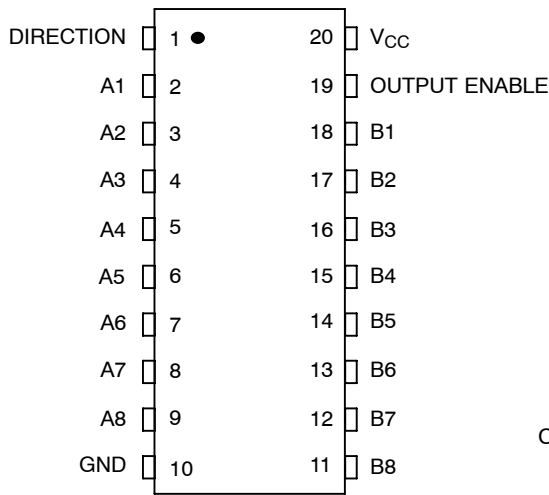


Figure 1. Pin Assignment

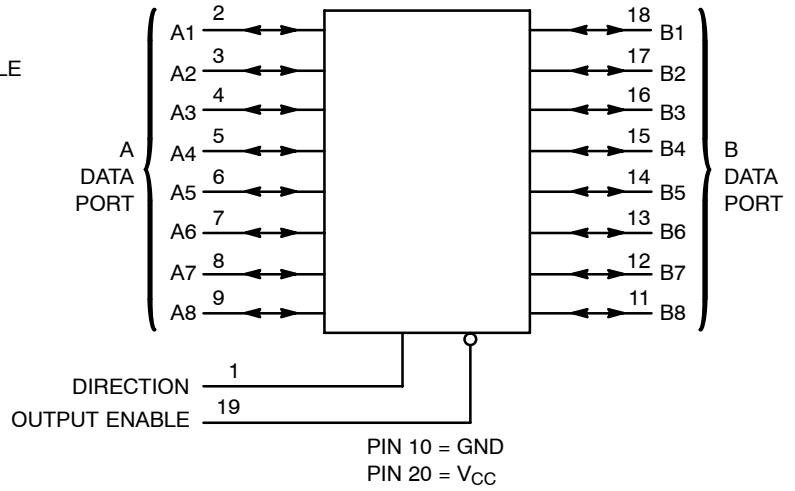


Figure 2. Logic Diagram

## FUNCTION TABLE

Control Inputs		Operation
Output Enable	Direction	
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High-Impedance State)

X = don't care

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
74HC245DTR2G	TSSOP-20*	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

# 74HC245

## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>OUT</sub>	DC Output Voltage (Note 2)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	DC Input Diode Current	±20	mA
I <sub>OK</sub>	DC Output Diode Current	±35	mA
I <sub>OUT</sub>	DC Output Sink Current	±35	mA
I <sub>CC</sub>	DC Supply Current per Supply Pin	±75	mA
I <sub>GND</sub>	DC Ground Current per Ground Pin	±75	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance TSSOP	128	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 85°C TSSOP	450	mW
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating Oxygen Index: 30% to 35%	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4)	> 2000 > 200	V
I <sub>LATCHUP</sub>	Latchup Performance Above V <sub>CC</sub> and Below GND at 85°C (Note 5)	±300	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 20 ounce copper trace with no air flow.
2. I<sub>O</sub> absolute maximum rating must be observed.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to EIA/JESD78.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 3)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

# 74HC245

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				-55 to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V <sub>in</sub> = V <sub>IH</sub>  I <sub>out</sub>   ≤ 2.4 mA  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V <sub>in</sub> = V <sub>IL</sub>  I <sub>out</sub>   ≤ 2.4 mA  I <sub>out</sub>   ≤ 6.0 mA  I <sub>out</sub>   ≤ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	6.0	±0.1	±1.0	±1.0	μA
I <sub>OZ</sub>	Maximum Three-State Leakage Current	Output in High-Impedance State V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub> V <sub>out</sub> = V <sub>CC</sub> or GND	6.0	±0.5	±5.0	±10	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	6.0	4.0	40	40	μA

6. Information on typical parametric values and high frequency or heavy load considerations can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			-55 to 25°C	≤ 85°C	≤ 125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, A to B, B to A (Figures 1 and 3)	2.0	75	95	110	ns
		3.0	55	70	80	
		4.5	15	19	22	
		6.0	13	16	19	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4)	2.0	110	140	165	ns
		3.0	90	110	130	
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Propagation Delay, Output Enable to A or B (Figures 2 and 4)	2.0	110	140	165	ns
		3.0	90	110	130	
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	60	75	90	ns
		3.0	23	27	32	
		4.5	12	15	18	
		6.0	10	13	15	
C <sub>in</sub>	Maximum Input Capacitance (Pin 1 or Pin 19)	-	10	10	10	pF
C <sub>out</sub>	Maximum Three-State I/O Capacitance (I/O in High-Impedance State)	-	15	15	15	pF

7. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C <sub>PD</sub>	Power Dissipation Capacitance (Per Transceiver Channel) (Note 8)	Typical @ 25°C, V <sub>CC</sub> = 5.0 V		pF
		40		

8. Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

# 74HC245

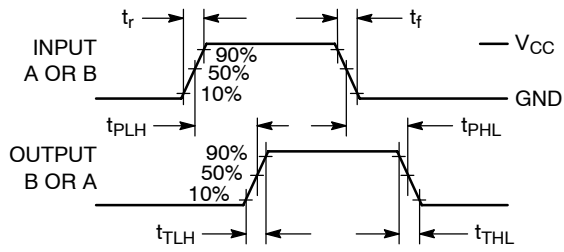


Figure 3. Switching Waveform

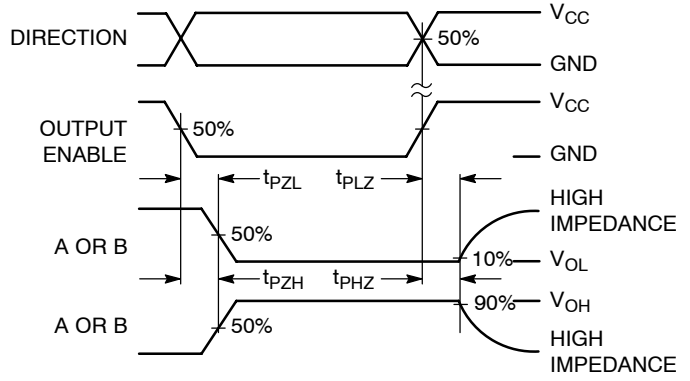
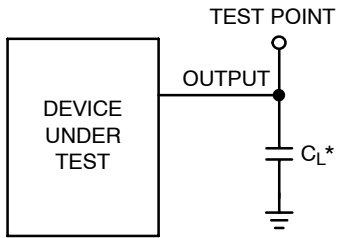
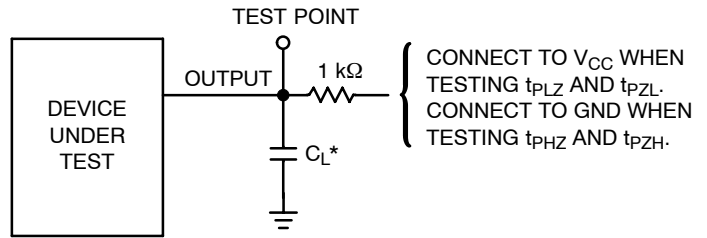


Figure 4. Switching Waveform



\*Includes all probe and jig capacitance

Figure 5. Test Circuit



\*Includes all probe and jig capacitance

Figure 6. Test Circuit

# 74HC245

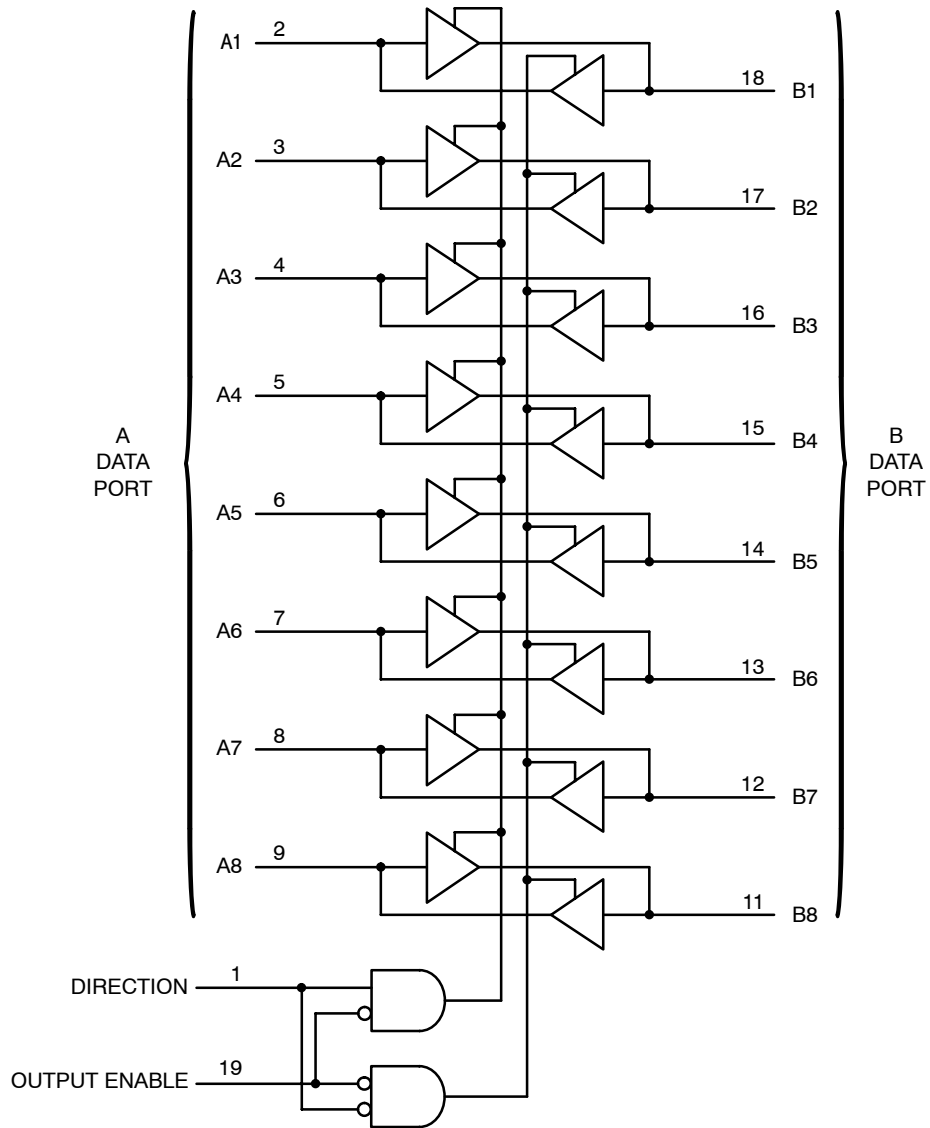
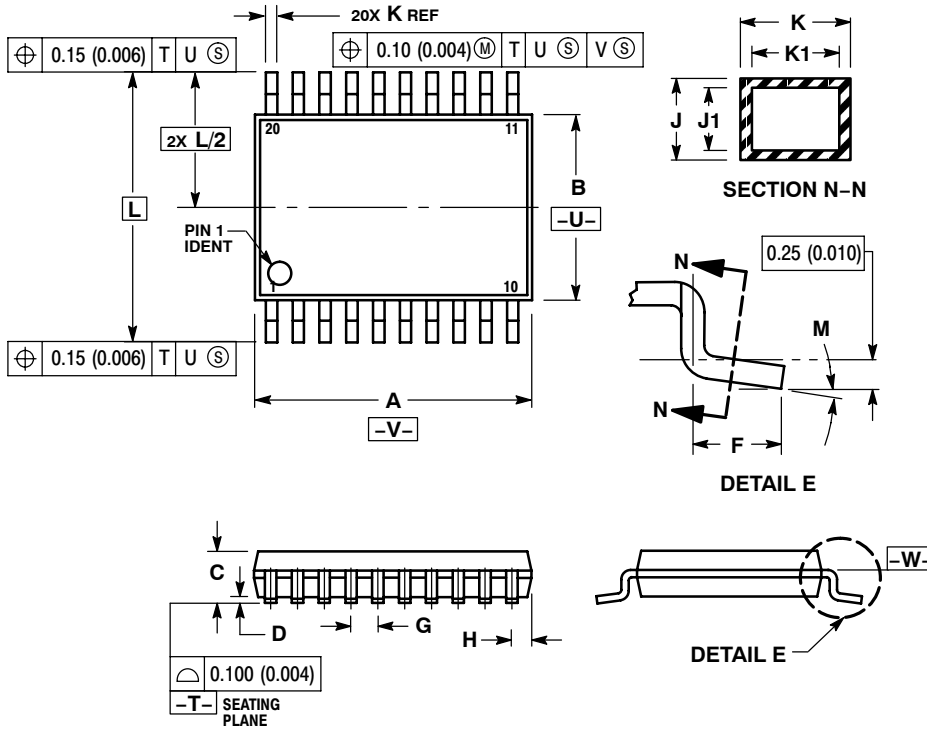


Figure 7. Expanded Logic Diagram

# 74HC245

## PACKAGE DIMENSIONS

TSSOP-20  
CASE 948E-02  
ISSUE C

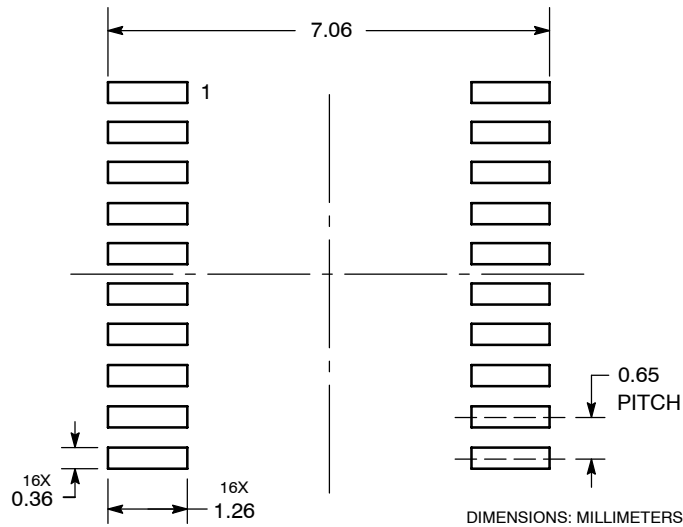


**NOTES:**


1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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