

# 74HCT04

## Hex Inverter

### With LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The 74HCT04 may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs. The HCT04A is identical in pinout to the LS04.

#### Features

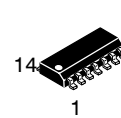
- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance With the JEDEC Standard No. 7A Requirements
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 48 FETs or 12 Equivalent Gates
- These are Pb-Free Devices



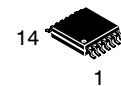
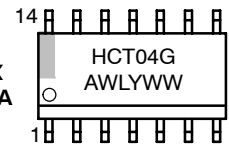
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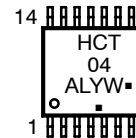
#### MARKING DIAGRAMS



SOIC-14  
D SUFFIX  
CASE 751A



TSSOP-14  
DT SUFFIX  
CASE 948G



HCT04 = Device Code  
A = Assembly Location  
L, WL = Wafer Lot  
Y = Year  
W, WW = Work Week  
G or ■ = Pb-Free Package

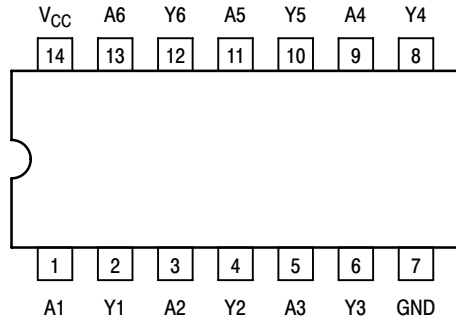
(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# 74HCT04

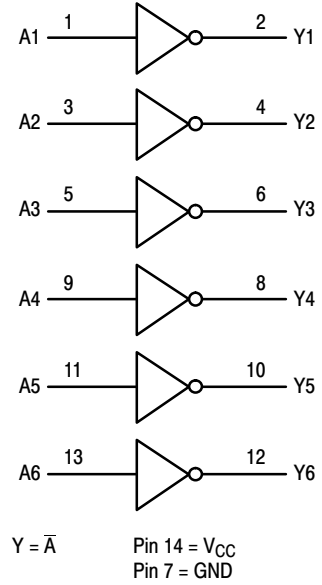
## Pinout: 14-Lead Packages (Top View)



## FUNCTION TABLE

| Inputs | Outputs |
|--------|---------|
| A      | Y       |
| L      | H       |
| H      | L       |

## LOGIC DIAGRAM



## ORDERING INFORMATION

| Device       | Package           | Shipping <sup>†</sup> |
|--------------|-------------------|-----------------------|
| 74HCT04DR2G  | SOIC-14 (Pb-Free) | 2500 / Tape & Reel    |
| 74HCT04DTR2G | TSSOP-14*         |                       |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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## MAXIMUM RATINGS

| Symbol    | Parameter  | Value                   | Unit |
|-----------|--|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)                                    | - 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)                                     | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)                                    | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin  | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin   | $\pm 25$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins                                 | $\pm 50$                | mA   |
| $P_D$     | Power Dissipation in Still Air<br>SOIC Package†<br>TSSOP Package†        | 500<br>450              | mW   |
| $T_{stg}$ | Storage Temperature Range  | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>SOIC or TSSOP Package | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†Derating — SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min  | Max      | Unit |
|-------------------|--|------|----------|------|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 4.5  | 5.5      | V    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0    | $V_{CC}$ | V    |
| $T_A$             | Operating Temperature Range, All Package Types       | - 55 | + 125    | °C   |
| $t_r, t_f$        | Input Rise/Fall Time (Figure 1)                      | 0    | 500      | ns   |

## DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Condition   | $V_{CC}$<br>(V) | Guaranteed Limit         |                         |                          | Unit    |
|-----------------|--|---|-----------------|--------------------------|-------------------------|--------------------------|---------|
|                 |  |   |                 | -55 to 25°C              | $\leq 85^\circ\text{C}$ | $\leq 125^\circ\text{C}$ |         |
| $V_{IH}$        | Minimum High-Level Input Voltage               | $V_{out} = 0.1V$<br>$ I_{out}  \leq 20\mu A$  | 4.5             | 2.0                      | 2.0                     | 2.0                      | V       |
|                 |  |   | 5.5             | 2.0                      | 2.0                     | 2.0                      |         |
| $V_{IL}$        | Maximum Low-Level Input Voltage                | $V_{out} = V_{CC} - 0.1V$<br>$ I_{out}  \leq 20\mu A$   | 4.5             | 0.8                      | 0.8                     | 0.8                      | V       |
|                 |  |   | 5.5             | 0.8                      | 0.8                     | 0.8                      |         |
| $V_{OH}$        | Minimum High-Level Output Voltage              | $V_{in} = V_{IL}$<br>$ I_{out}  \leq 20\mu A$   | 4.5             | 4.4                      | 4.4                     | 4.4                      | V       |
|                 |  |   | 5.5             | 5.4                      | 5.4                     | 5.4                      |         |
| $V_{OL}$        | Maximum Low-Level Output Voltage               | $V_{in} = V_{IH}$<br>$ I_{out}  \leq 20\mu A$   | 4.5             | 0.1                      | 0.1                     | 0.1                      | V       |
|                 |  |   | 5.5             | 0.1                      | 0.1                     | 0.1                      |         |
| $I_{in}$        | Maximum Input Leakage Current                  | $V_{in} = V_{CC}$ or GND  | 4.5             | 0.26                     | 0.33                    | 0.40                     | $\mu A$ |
|                 |  |   | 5.5             | $\pm 0.1$                | $\pm 1.0$               | $\pm 1.0$                |         |
| $I_{CC}$        | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC}$ or GND<br>$I_{out} = 0\mu A$  | 4.5             | 2.0                      | 20                      | 40                       | $\mu A$ |
|                 |  |   | 5.5             | 2.0                      | 20                      | 40                       |         |
| $\Delta I_{CC}$ | Additional Quiescent Supply Current            | $V_{in} = 2.4V$ , Any One Input<br>$V_{in} = V_{CC}$ or GND, Other Inputs<br>$I_{out} = 0\mu A$ | 5.5             | $\geq -55^\circ\text{C}$ | 25 to 125°C             |                          | mA      |
|                 |  |   |                 | 2.9                      | 2.4                     |                          |         |

- Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

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## AC CHARACTERISTICS ( $V_{CC} = 5.0V \pm 10\%$ , $C_L = 50pF$ , Input $t_r = t_f = 6ns$ )

| Symbol                   | Parameter   | Guaranteed Limit |          |          | Unit |
|--------------------------|---|------------------|----------|----------|------|
|                          |   | -55 to 25°C      | ≤85°C    | ≤125°C   |      |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Maximum Propagation Delay, Input A to Output Y<br>(Figures 1 and 2) | 15<br>17         | 19<br>21 | 22<br>26 | ns   |
| $t_{TLH}$ ,<br>$t_{THL}$ | Maximum Output Transition Time, Any Output<br>(Figures 1 and 2)     | 15               | 19       | 22       | ns   |
| $C_{in}$                 | Maximum Input Capacitance   | 10               | 10       | 10       | pF   |

3. For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| $C_{PD}$ | Power Dissipation Capacitance (Per Inverter)* | Typical @ 25°C, $V_{CC} = 5.0 V$ |  | pF |
|----------|---|----------------------------------|--|----|
|          |   | 22                               |  |    |
|          |   |                                  |  |    |

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ . For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

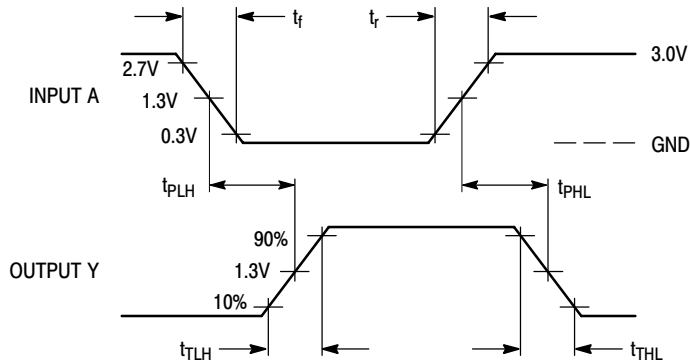
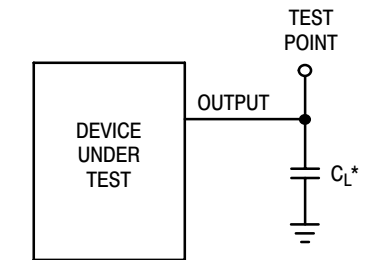


Figure 1. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 2. Test Circuit

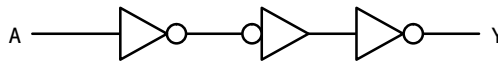
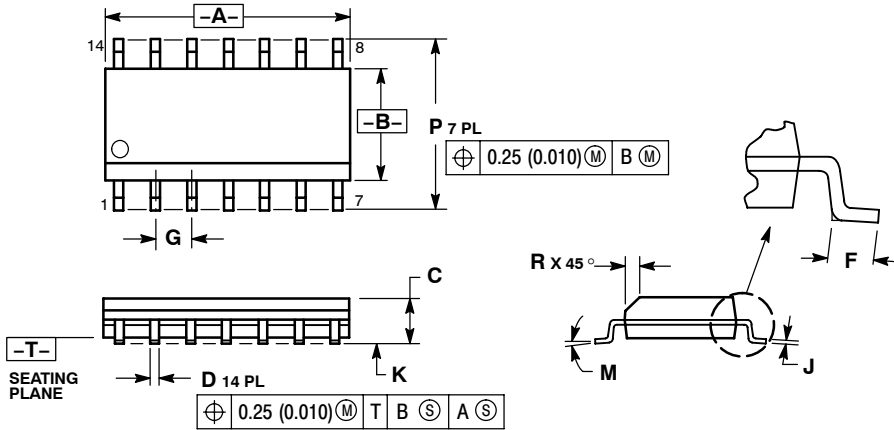


Figure 3. Expanded Logic Diagram  
(1/6 of the Device Shown)

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## PACKAGE DIMENSIONS

SOIC-14  
CASE 751A-03  
ISSUE H

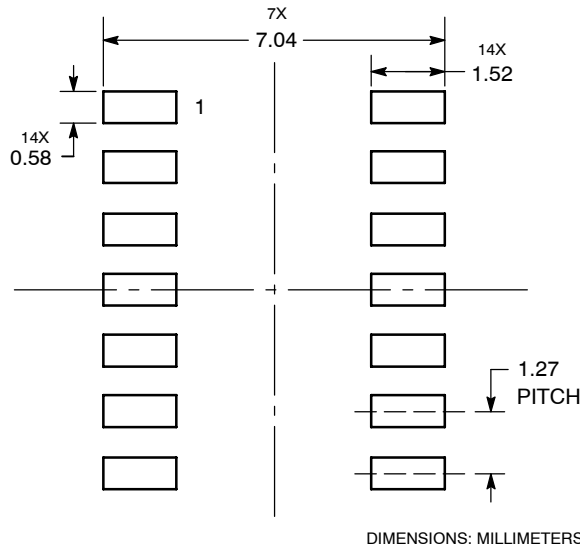


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 8.55        | 8.75 | 0.337     | 0.344 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.054     | 0.068 |
| D   | 0.35        | 0.49 | 0.014     | 0.019 |
| F   | 0.40        | 1.25 | 0.016     | 0.049 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| J   | 0.19        | 0.25 | 0.008     | 0.009 |
| K   | 0.10        | 0.25 | 0.004     | 0.009 |
| M   | 0°          | 7°   | 0°        | 7°    |
| P   | 5.80        | 6.20 | 0.228     | 0.244 |
| R   | 0.25        | 0.50 | 0.010     | 0.019 |

### SOLDERING FOOTPRINT\*



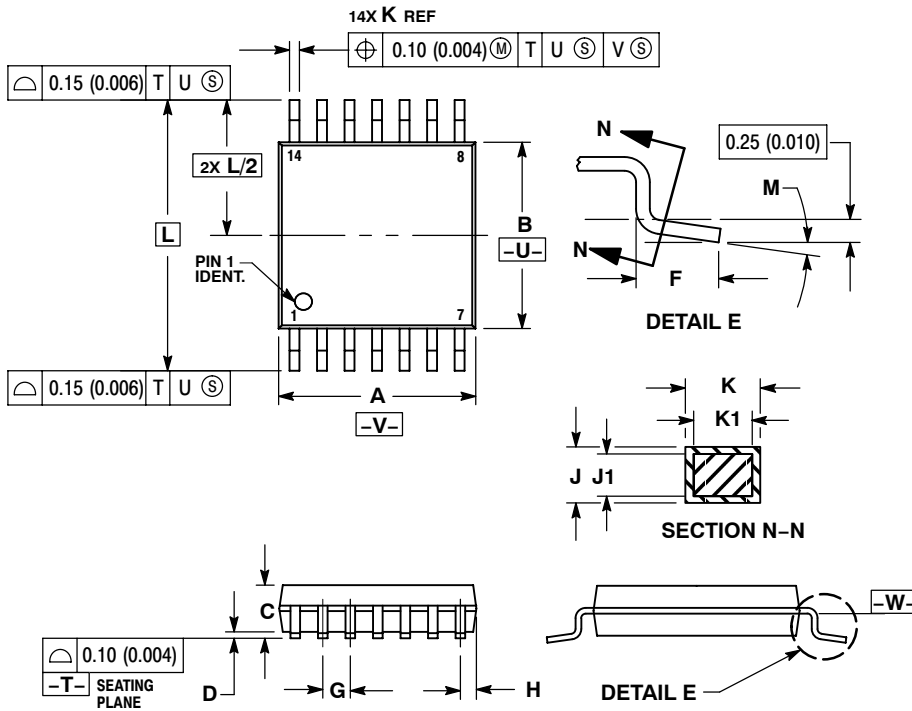
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## PACKAGE DIMENSIONS

TSSOP-14  
CASE 948G-01  
ISSUE B

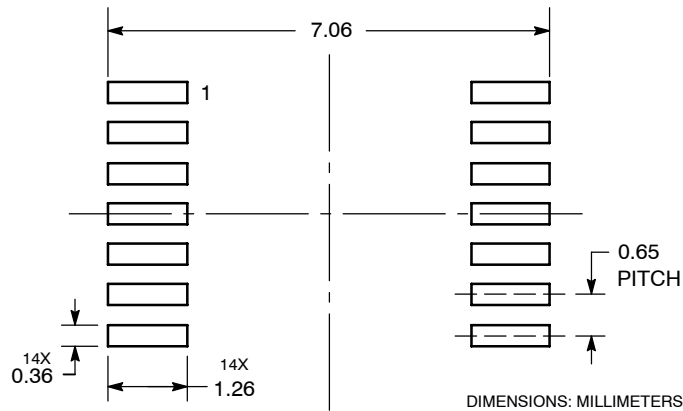


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | ---         | 1.20 | ---       | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0° 8°       |      | 0° 8°     |       |

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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