NB3N3011DTEVB

NB3N3011DTEVB Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Board Description

The NB3N3011 Evaluation Board provides a flexible and convenient platform to quickly evaluate, characterize and verify the performance and operation of the NB3N3011 Clock Generator. This user's manual provides detailed information on board contents, layout and its use. It should be used in conjunction with a device datasheet: NB3N3011. (www.onsemi.com)

A single TSSOP−8 (wide) device can be mounted on the board.

Board Features

- Accommodates the Electrical Characterization of the NB3N3011
- Supports Use of a 25 MHz and 26.5625 MHz Through−hole or Surface Mount Crystal
- Incorporates on Board Power Supply Filter
- Convenient and Compact Board Layout
- 3.3 V Single or Split−power Supply Operation
- LVPECL Differential Output Signals are Accessed via SMA Connectors

Board Layout

The evaluation board is constructed with FR4 material and is designed to minimize noise, and crosstalk and achieve high bandwidth. SMA connectors are provided for output signal access.

Layer Stack

L1 Signal and SMAGND
L2 SMA Ground
L3 V_{CC} (Positive Power Supply) and V_{EE} (Device Negative Power Supply)
L4 Signal

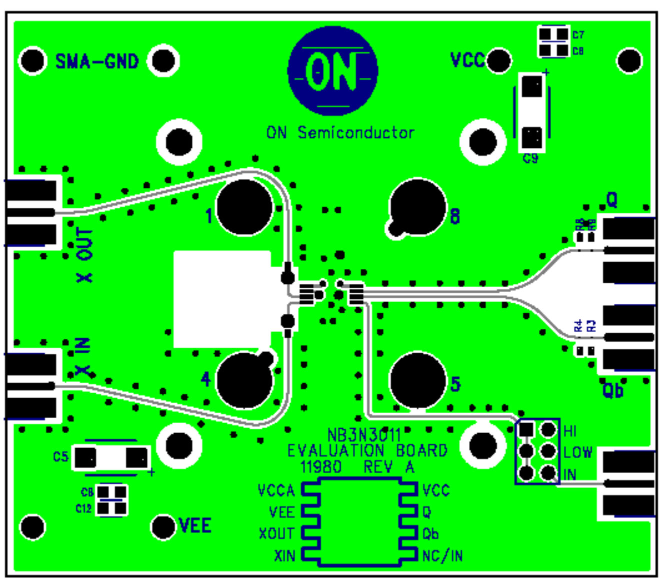


Figure 1. Evaluation Board

LAB SETUP PROCEDURE

Power Supply Connections and Output Termination

The NB3N3011 has a positive supply pin, V_{CC}, and a negative supply pin, V_{EE}. SMAGND (V_{TT}) is the termination supply for the LVPECL outputs, only.

Power supply banana plug connectors for V_{CC}, V_{EE} and SMAGND are provided in the corners of the board. The LVPECL Q and $\overline{Q}$ outputs have standard, open emitter outputs and must be externally DC loaded and terminated. Thevenin equivalent load and termination resistors pads are provided at the Q/$\overline{Q}$ output's SMA connectors, but are not installed. A "split" or dual power supply technique can be used to take advantage of terminating the LVPECL outputs into 50 Ω of an oscilloscope or a frequency counter. Since $V_{TT} = V_{CC} - 2.0$ V, offsetting V_{CC} to +2.0 V yields V_{TT} = 0 V or Ground. The V_{TT} terminal connects to the isolated SMAGND connector ground plane, and is not to be confused with the device ground pin or V_{EE}.

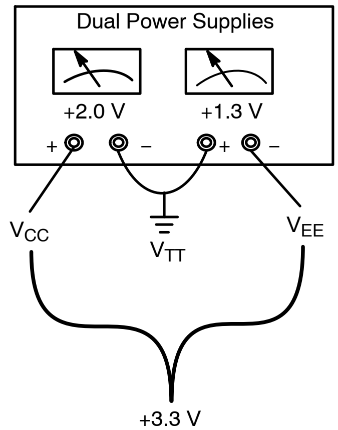


Figure 2. "Split" or Dual Power Supply Connections

Table 1. "SPLIT" POWER SUPPLY CONFIGURATION

Device Pin	Power Supply	"Spilt" Power Supply
V_{CC}	RED	V_{CC} = +2.0 V
SMAGND	BLACK	$V_{TT} = V_{CC} - 2.0$ V = 0 V
V_{EE}	BLACK	V_{EE} = −1.3 V

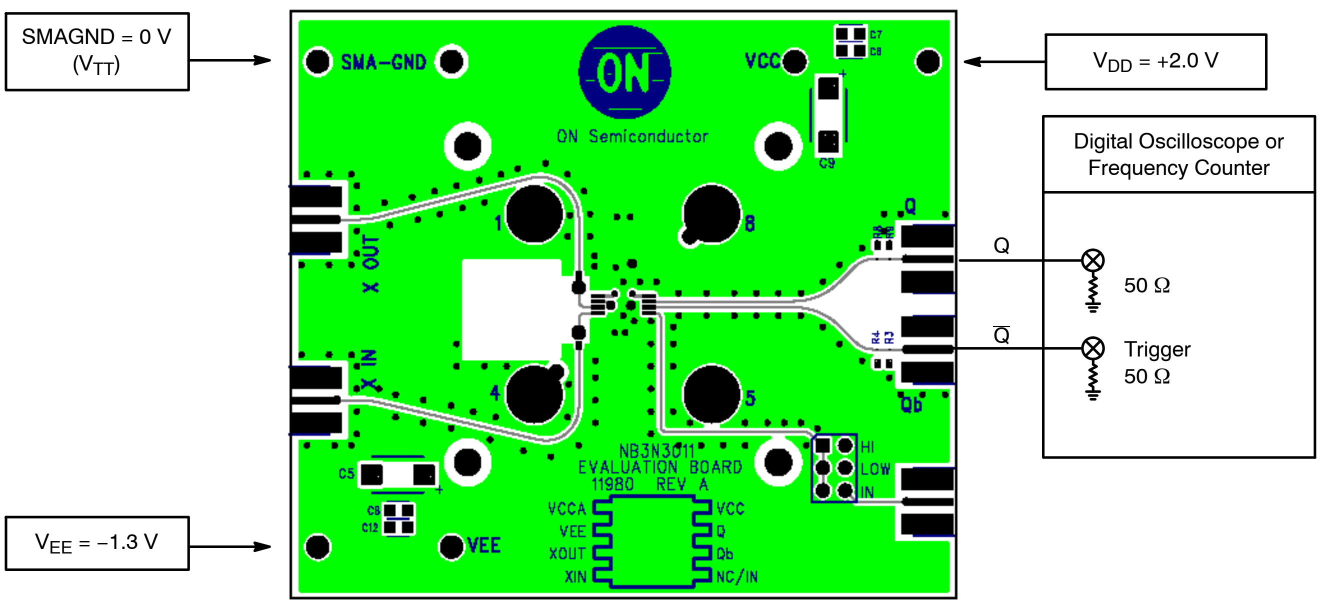


Figure 3. "Split" Power Supply Connections

LAB SETUP AND MEASUREMENT PROCEDURE

Equipment Used

- Tektronix TDS8000 Oscilloscope or Frequency Counter
- Agilent #6624A DC Power Supply
- Digital Voltmeter
- Matched high−speed cables with SMA connectors

In order to get started and demonstrate the NB3N3011, perform the following test set−up sequence:

To monitor the Q and $\overline{Q}$ outputs on an oscilloscope or frequency counter (with internal 50 Ω termination impedance), the power supply needs to be DC offset:

1. Connect a “split” power supply to the evaluation board. (see Figure 2)
   Connect V_{CC} banana jack to +2.0 V
   Connect SMAGND banana jack to ground = 0 V
   Connect V_{EE} banana jack to −1.3 V for 3.3 V operation
2. Ensure the oscilloscope is triggered properly and has 50 Ω internal termination to ground. The board does not provide 50 Ω source termination resistors. Two oscilloscope trigger methods are1) from Q (using a “T” connector) or 2) directly from $\overline{Q}$.
3. Connect the LVPECL Q and $\overline{Q}$ outputs to the oscilloscope with good quality matched cables. The outputs are terminated with 50 Ω to V_{TT} = SMAGND (V_{CC} – 2.0 V) = 0 V = Ground internal to the oscilloscope.

NB3N3011 Evaluation Board Pin Descriptions and Features by Pin

The NB3N3011 Evaluation Board was designed to accommodate the test and evaluation of the NB3N3011 LVPECL Clock Generator. Detailed board features by device pin are described below:

Crystal (XTAL_IN and XTAL_OUT)

A through−hole or surface mount parallel resonant crystal can be used.

Disregard the metal traces and connectors from X_{IN} and X_{OUT}. They are open and NOT connected to the crystal package pins and have no impedance affect on the crystal.

Q and $\overline{Q}$

The Q and $\overline{Q}$ LVPECL outputs have equal length 50 Ω board traces with SMA connectors. Matched cables can connect to an oscilloscope or frequency counter.

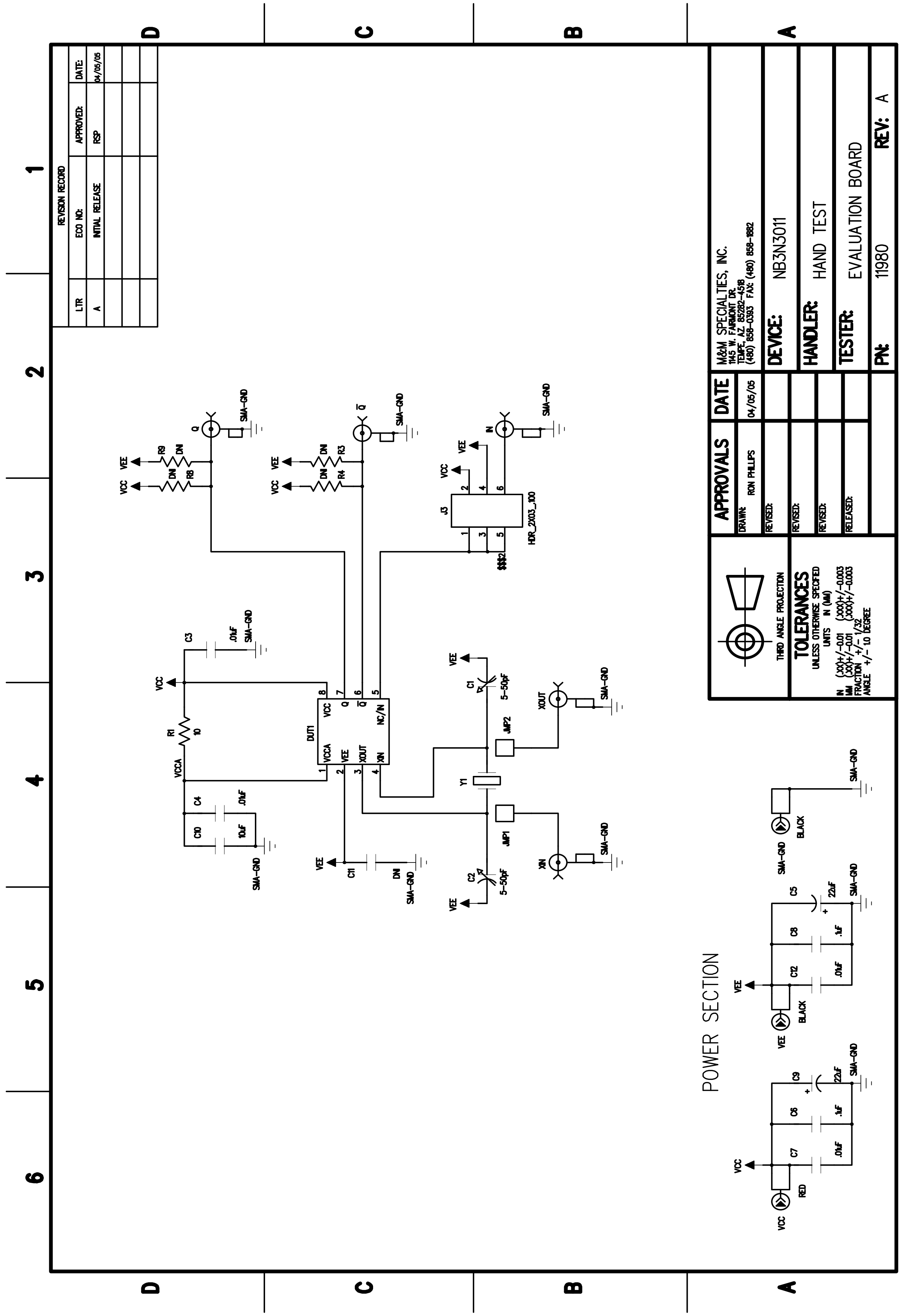
V_{CC} and V_{CCA}

The V_{CC} pin is connected directly to the V_{CC} power plane. By−pass capacitors are installed.

The V_{CCA} pin has the power supply filter components installed per the datasheet.

Table 2. NB3N3011 BILL OF MATERIALS

Component	Description	Qty	Designator
Connector	Johnson Comp Inc SMA #142−0711−821	2	Q, $\overline{Q}$
Capacitor, P/S Bypass	22 μF	2	C5, C9
Capacitor, P/S Bypass; VCCA Filter	0.01 μF	4	C7, C12
Capacitor, P/S Bypass	0.1 μF	2	C8, C8
Capacitor, VCCA Filter	10 μF	1	C10
Capacitor, Cyrstal Load	33 μF	1	C14
Capacitor, Cyrstal Load	22 μF	1	C13
Crystal	25 MHz, Ecliptek #ECX6106−25.00M − Surface Mount #ECX6150−25.000M − Through−hole 26.5625 MHz, Ecliptek #ECX6110−26.5625M − Surface Mount #ECX6151−26.5625M − Through−hole	1	Y1
Jumper Header		0	
Jumper		0	
Resistor, VCCA Filter	10 Ω	1	R1
Banana Jack	Deltron #EF681 150−039 Red	1	VCC
Banana Jack	Deltron #EF681 150−040 Black	2	VEE, SMAGND
Stand−offs		4	
NB3N3011	TSSOP−8 (Wide) device mounted on board	1	
TSSOP−8 (Wide) Socket	M&M Specialties #50−000−00659 (Optional) (480)−858−0393	Optional	



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DEVICE: NB3N3011
HANDLER: HAND TEST
TESTER: EVALUATION BOARD
PN: 11980
REV: A
APPROVALS
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DRAWN: RON PHILLIPS
04/05/05
REVISED:
RELEASED:
THIRD ANGLE PROJECTION
TOLERANCES
UNLESS OTHERWISE SPECIFIED
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ECO NO:
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DATE:
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