1 GHz Current Feedback Op Amp

NCS2511 is a 1 GHz current feedback monolithic operational amplifier featuring high slew rate and low differential gain and phase error. The current feedback architecture allows for a superior bandwidth and low power consumption.

Features

- -3.0 dB Small Signal BW ($A_V = +2.0$, $V_O = 0.5 V_{p-p}$) 1 GHz Typ
- Slew Rate 2500 V/µs
- Supply Current 7.5 mA
- Input Referred Voltage Noise 5.0 nV/\sqrt{Hz}
- THD -67 dB (f = 5.0 MHz, $V_0 = 2.0 V_{p-p}$)
- Output Current 120 mA
- Pin Compatible with AD8001, TSH350, OPA681
- This is a Pb–Free Device

Applications

- High Resolution Video
- Line Driver
- High-Speed Instrumentation
- Wide Dynamic Range IF Amp
- Set Top Box
- NTSC/PAL/HDTV



Áv = +2.0



ON Semiconductor®

http://onsemi.com



SOT23-5 (TSOP-5) PINOUT



ORDERING INFORMATION

Device	Package	Shipping [†]
NCS2511SNT1G	SOT23-5 (TSOP-5) (Pb-Free)	3000/Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTION





Figure 2. Simplified Device Schematic

ATTRIBUTES

Characteristics	Value
ESD	
Human Body Model	2.0 kV (Note 1)
Machine Model	200 V
Charged Device Model	1.0 kV
Moisture Sensitivity (Note 2)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in

1. 0.8 kV between the input pairs +IN and -IN pins only. All other pins are 2.0 kV.

2. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VS	11	Vdc
Input Voltage Range	VI	≤VS	Vdc
Input Differential Voltage Range	V _{ID}	≤VS	Vdc
Output Current	Ι _Ο	120	mA
Maximum Junction Temperature (Note 3)	TJ	150	°C
Operating Ambient Temperature	T _A	-40 to +85	°C
Storage Temperature Range	T _{stg}	–60 to +150	°C
Power Dissipation	PD	(See Graph)	mW
Thermal Resistance, Junction-to-Air	$R_{ hetaJA}$	121	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 150°C. If the maximum is exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the "overheated" condition for an extended period can result in device damage. To ensure proper operation, it is important to observe the derating curves.



Figure 3. Power Dissipation vs. Temperature

AC ELECTRICAL CHARACTERISTICS (V _{CC} = +5.0 V, V _{EE} = -5.0 V, T _A = -40°C to +85°C, R _L = 150 Ω to GND, R _F = 270	Ω,
$A_V = +2.0$, Enable is left open, unless otherwise specified).	

Symbol	Characteristic	Conditions	Min	Тур	Max	Unit
FREQUENC	Y DOMAIN PERFORMANCE					
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 2.0 V_{p-p}		1000 800		MHz
GF _{0.1dB}	0.1 dB Gain Flatness Bandwidth	A _V = +2.0		50		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω , f = 3.58 MHz		0.01		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω , f = 3.58 MHz		0.01		0
TIME DOM	AIN RESPONSE					
SR	Slew Rate	$A_{V} = +2.0, V_{step} = 2.0 V$		2500		V/µs

SR	Slew Rate	$A_V = +2.0, V_{step} = 2.0 V$	2500	v/µs
t _s	Settling Time 0.1%	A _V = +2.0, V _{step} = 2.0 V	13	ns
t _r t _f	Rise and Fall Time	(10%–90%) A _V = +2.0, V _{step} = 2.0 V	1.5	ns

HARMONIC/NOISE PERFORMANCE

THD	Total Harmonic Distortion	$f = 5.0 \text{ MHz}, V_0 = 2.0 V_{p-p}$	-67	dB
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_0 = 2.0 V_{p-p}	-72	dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_0 = 2.0 V_{p-p}	-70	dBc
IP3	Third-Order Intercept	$f = 10 \text{ MHz}, \text{ V}_{O} = 1.0 \text{ V}_{p-p}$	35	dBm
SFDR	Spurious-Free Dynamic Range	f = 5.0 MHz, V_0 = 2.0 V_{p-p}	70	dBc
e _N	Input Referred Voltage Noise	f = 1.0 MHz	5.0	nV/\sqrt{Hz}
i _N	Input Referred Current Noise	f = 1.0 MHz, Inverting f = 1.0 MHz, Non–Inverting	20 30	pA/\sqrt{Hz}

DC ELECTRICAL CHARACTERISTICS (V _{CC} = +5.0 V, V _{FF} = +	-5.0 V, T _A = -40° C to $+85^{\circ}$ C, R _I = 150 Ω to GND, R _F = 270 Ω,
$A_V = +2.0$, Enable is left open, unless otherwise specified).	

Symbol	Characteristic	Conditions	Min	Тур	Max	Unit
DC PERFOR	RMANCE					
V _{IO}	Input Offset Voltage (Note 4)		-10	0	+10	mV
$\Delta V_{IO} / \Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/°C
I _{IB}	Input Bias Current	+Input (Non–Inverting), $V_O = 0 V$ -Input (Inverting), $V_O = 0 V$ (Note 4)		$\begin{array}{c} \pm 3.0 \\ \pm 6.0 \end{array}$	± 35 ± 35	μΑ
$\Delta I_{IB} / \Delta T$	Input Bias Current Tempera- ture Coefficient	+Input (Non–Inverting), $V_O = 0 V$ –Input (Inverting), $V_O = 0 V$		+40 -10		nA/°C
INPUT CHA	RACTERISTICS					
V _{CM}	Input Common Mode Voltage Range (Note 4)		± 3.0	±4.0		V
CMRR	Common Mode Rejection Ratio (Note 4)	(See Graph)	40	50		dB
R _{IN}	Input Resistance	+Input (Non-Inverting) –Input (Inverting)		150 70		kΩ Ω
C _{IN}	Differential Input Capacitance			1.0		pF
OUTPUT CH	IARACTERISTICS					
R _{OUT}	Output Resistance	Closed Loop Open Loop		0.1 30		Ω
V _O	Output Voltage Range		±3.0	±4.0		V
Ι _Ο	Output Current		±90	±120		mA
POWER SU	PPLY					
V _S	Operating Voltage Supply			10		V
۱ _S	Power Supply Current	V _O = 0 V		7.5		mA
PSRR	Power Supply Rejection Ratio (Note 4)	(See Graph)	40	55		dB

4. Guaranteed by design and/or characterization.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V, V_{EE} = -2.5 V, T_A = -40°C to +85°C, R_L = 150 Ω to GND, R_F = 270 Ω , A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Тур	Max	Unit
FREQUENC	CY DOMAIN PERFORMANCE					
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	$\begin{array}{l} A_V = +2.0, V_O = 0.5 V_{p-p} \\ A_V = +2.0, V_O = 1.0 V_{p-p} \end{array}$		800 500		MHz
GF _{0.1dB}	0.1 dB Gain Flatness Bandwidth	A _V = +2.0		40		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω , f = 3.58 MHz		0.01		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω , f = 3.58 MHz		0.01		٥
TIME DOM	AIN RESPONSE					
SR	Slew Rate	A _V = +2.0, V _{step} = 1.0 V		1500		V/μs
t _s	Settling Time 0.1%	A _V = +2.0, V _{step} = 1.0 V		10		ns
t _r t _f	Rise and Fall Time	(10%–90%) A _V = +2.0, V _{step} = 1.0 V		1.2		ns
HARMONIC	/NOISE PERFORMANCE					
THD	Total Harmonic Distortion	$f = 5.0 \text{ MHz}, V_0 = 1.0 V_{p-p}$		-57		dB
HD2	2nd Harmonic Distortion	$f = 5.0 \text{ MHz}, V_0 = 1.0 V_{p-p}$		-62		dBc
HD3	3rd Harmonic Distortion	$f = 5.0 \text{ MHz}, V_{O} = 1.0 V_{p-p}$		-60	1	dBc

$$\label{eq:f} \begin{split} f &= 5.0 \text{ MHz}, \text{ } \text{V}_{\text{O}} = 1.0 \text{ } \text{V}_{\text{p-p}} \\ \\ f &= 10 \text{ } \text{MHz}, \text{ } \text{V}_{\text{O}} = 0.5 \text{ } \text{V}_{\text{p-p}} \end{split}$$

f = 5.0 MHz, V_{O} = 1.0 V_{p-p}

f = 1.0 MHz

f = 1.0 MHz, Inverting

f = 1.0 MHz, Non-Inverting

dBm

dBc

 nV/\sqrt{Hz}

 pA/\sqrt{Hz}

28

60

5.0

20

30

IP3

SFDR

e_N

i_N

Third-Order Intercept

Range

Spurious-Free Dynamic

Input Referred Voltage Noise

Input Referred Current Noise

DC ELECTRICAL CHARACTERISTICS (V _{CC} = +2.5 V, V _{FF} = -2.5 V, T _A = -40°C to +85°C, R _I = 150 Ω to GND, R _F = 270 Ω ,	
$A_V = +2.0$, Enable is left open, unless otherwise specified).	

Characteristic	Conditions	Min	Тур	Max	Unit
RMANCE					
Input Offset Voltage (Note 5)		-10	0	+10	mV
Input Offset Voltage Temperature Coefficient			6.0		μV/°C
Input Bias Current	+Input (Non–Inverting), $V_0 = 0 V$ -Input (Inverting), $V_0 = 0 V$ (Note 5)		$\begin{array}{c} \pm 3.0 \\ \pm 6.0 \end{array}$	± 35 ± 35	μΑ
Input Bias Current Tempera- ture Coefficient	+Input (Non–Inverting), $V_0 = 0 V$ –Input (Inverting), $V_0 = 0 V$		+40 -10		nA/°C
RACTERISTICS					
Input Common Mode Voltage Range (Note 5)		±1.1	±1.5		V
Common Mode Rejection Ratio (Note 5)	(See Graph)	40	50		dB
Input Resistance	+Input (Non–Inverting) –Input (Inverting)		150 70		kΩ Ω
Differential Input Capacitance			1.0		pF
HARACTERISTICS					
Output Resistance	Closed Loop Open Loop		0.1 30		Ω
Output Voltage Range		±1.1	±1.5		V
Output Current		±90	±120		mA
IPPLY					
Operating Voltage Supply			5.0		V
Power Supply Current	V _O = 0 V		6.5		mA
Power Supply Rejection Ratio (Note 5)	(See Graph)	40	55		dB
	Characteristic RMANCE Input Offset Voltage (Note 5) Input Offset Voltage Temperature Coefficient Input Bias Current Input Bias Current Tempera- ture Coefficient RACTERISTICS Input Common Mode Voltage Range (Note 5) Common Mode Rejection Ratio (Note 5) Input Resistance Differential Input Capacitance HARACTERISTICS Output Resistance Output Voltage Range Output Voltage Range Output Current PPLY Operating Voltage Supply Power Supply Current Power Supply Rejection Ratio (Note 5)	Characteristic Conditions RMANCE Input Offset Voltage (Note 5) Input Offset Voltage Temperature Coefficient Input Bias Current +Input (Non–Inverting), V _O = 0 V Input Bias Current Temperature Coefficient +Input (Non–Inverting), V _O = 0 V Input Bias Current Temperature Coefficient +Input (Non–Inverting), V _O = 0 V Input Common Mode Voltage Range (Note 5) +Input (Inverting), V _O = 0 V Common Mode Rejection Ratio (Note 5) (See Graph) Input Resistance +Input (Non–Inverting) Differential Input Capacitance +Input (Non–Inverting) Output Resistance Closed Loop Open Loop Output Voltage Range Open Loop Output Voltage Range Open Loop Output Current V _O = 0 V PPLY Power Supply Current V _O = 0 V Power Supply Rejection Ratio (Note 5) (See Graph)	CharacteristicConditionsMinRMANCEInput Offset Voltage (Note 5)-10Input Offset Voltage Temperature Coefficient-10Input Bias Current+Input (Non-Inverting), $V_0 = 0 V$ -Input (Inverting), $V_0 = 0 V$ -Input (Inverting), $V_0 = 0 V$ Input Bias Current Temperature Coefficient+Input (Non-Inverting), $V_0 = 0 V$ -Input (Inverting), $V_0 = 0 V$ RACTERISTICS+Input (Non-Inverting), $V_0 = 0 V$ Input Common Mode Voltage Range (Note 5) ± 1.1 Common Mode Rejection Ratio (Note 5)(See Graph)Input Resistance+Input (Non-Inverting) -Input (Inverting)Differential Input Capacitance ± 1.1 Output ResistanceClosed Loop Open LoopOutput Voltage Range ± 1.1 Output Voltage Range ± 1.1 Output Current ± 90 PPLYOperating Voltage SupplyVo = 0 VPower Supply Rejection Ratio (Note 5)(See Graph)40	CharacteristicConditionsMinTypRMANCEInput Offset Voltage (Note 5) -10 0Input Offset Voltage Temperature Coefficient $+1$ nput (Non-Inverting), $V_0 = 0$ V ± 3.0 Input Bias Current $+1$ nput (Non-Inverting), $V_0 = 0$ V ± 6.0 Input Bias Current Tempera- ture Coefficient $+1$ nput (Non-Inverting), $V_0 = 0$ V ± 440 Input Bias Current Tempera- ture Coefficient $+1$ nput (Non-Inverting), $V_0 = 0$ V ± 440 Input Common Mode Voltage Rarge (Note 5) ± 1.1 ± 1.5 Input Common Mode Rejection Ratio (Note 5)(See Graph)4050Input Resistance $+1$ nput (Non-Inverting) -1 nput (Inverting)150Differential Input Capacitance -1 nput (Inverting)10HARACTERISTICS ± 1.1 ± 1.5 Output ResistanceClosed Loop Open Loop 30 Output Voltage Range ± 1.1 ± 1.5 Dutput Voltage Range ± 1.2 ± 90 PPLY $perting Voltage Supply$ 5.0 Power Supply Current $V_0 = 0$ V 6.5 Power Supply Rejection Ratio (Note 5) 40 55	CharacteristicConditionsMinTypMaxRMANCEInput Offset Voltage (Note 5) -10 0 $+10$ Input Offset Voltage (Note 5) -10 6.0 ± 3.0 ± 3.0 Input Offset Voltage Temperature Coefficient $+1nput (Non-Inverting), V_0 = 0 V$ ± 3.0 ± 3.5 Input Bias Current $+1nput (Inverting), V_0 = 0 V$ ± 4.0 ± 3.0 ± 3.5 Input Bias Current Tempera- ture Coefficient $+1nput (Inverting), V_0 = 0 V$ ± 4.0 ± 3.5 Input Common Mode Voltage Range (Note 5) ± 1.1 ± 1.5 ± 1.5 Common Mode Rejection Ratio (Note 5)(See Graph) 4.0 50 Input Resistance $+1nput (Inverting)$ 7.0 7.0 Differential Input Capacitance $-1nput (Inverting)$ 7.0 1.0 tARACTERISTICS ± 1.1 ± 1.5 5.0 5.0 Output Resistance $Olesed Loop$ Open Loop ± 9.0 ± 120 PELY $\mathbf{V}_0 = 0 V$ 6.5 $Power Supply Rejection Ratio(Note 5)5.0$

5. Guaranteed by design and/or characterization.



Figure 4. Typical Test Setup (A_V = +2.0, R_F = 270 Ω , R_L = 150 Ω)



Figure 11. THD, HD2, HD3 vs. Frequency

Figure 12. THD, HD2, HD3 vs. Output Voltage

Figure 15. PSRR vs. Frequency

General Design Considerations

The current feedback amplifier is optimized for use in high performance video and data acquisition systems. For current feedback architecture, its closed–loop bandwidth depends on the value of the feedback resistor. The closed–loop bandwidth is not a strong function of gain, as is for a voltage feedback amplifier, as shown in Figure 23.

Figure 23. Frequency Response vs. R_F

The -3.0 dB bandwidth is, to some extent, dependent on the power supply voltages. By using lower power supplies, the bandwidth is reduced, because the internal capacitance increases. Smaller values of feedback resistor can be used at lower supply voltages, to compensate for this affect.

Feedback and Gain Resistor Selection for Optimum Frequency Response

A current feedback operational amplifier's key advantage is the ability to maintain optimum frequency response independent of gain by using appropriate values for the feedback resistor. To obtain a very flat gain response, the feedback resistor tolerance should be considered as well. Resistor tolerance of 1% should be used for optimum flatness. Normally, lowering RF resistor from its recommended value will peak the frequency response and extend the bandwidth while increasing the value of RF resistor will cause the frequency response to roll off faster. Reducing the value of RF resistor too far below its recommended value will cause overshoot, ringing, and eventually oscillation.

Since each application is slightly different, it is worth some experimentation to find the optimal RF for a given circuit. A value of the feedback resistor that produces ~ 0.1 dB of peaking is the best compromise between stability and maximal bandwidth. It is not recommended to use a current feedback amplifier with the output shorted directly to the inverting input.

Printed Circuit Board Layout Techniques

Proper high speed PCB design rules should be used for all wideband amplifiers as the PCB parasitics can affect the overall performance. Most important are stray capacitances at the output and inverting input nodes as it can effect peaking and bandwidth. A space (3/16" is plenty) should be left around the signal lines to minimize coupling. Also, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than 1/4" are recommended.

Video Performance

This device designed to provide good performance with NTSC, PAL, and HDTV video signals. Best performance is obtained with back terminated loads as performance is degraded as the load is increased. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage.

ESD Protection

All device pins have limited ESD protection using internal diodes to power supplies as specified in the attributes table (see Figure 24). These diodes provide moderate protection to input overdrive voltages above the supplies. The ESD diodes can support high input currents with current limiting series resistors. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Under closed–loop operation, the ESD diodes have no effect on circuit performance. However, under certain conditions the ESD diodes will be evident. If the device is driven into a slewing condition, the ESD diodes will clamp large differential voltages until the feedback loop restores closed–loop operation. Also, if the device is powered down and a large input signal is applied, the ESD diodes will conduct.

NOTE: Human Body Model for +IN and –IN pins are rated at 0.8kV while all other pins are rated at 2.0kV.

Figure 24. Internal ESD Protection

PACKAGE DIMENSIONS

TSOP-5 **SN SUFFIX** CASE 483-02 **ISSUE E**

D

⊕ 0.05 (0.002)

G

В

С

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- 2. MAXIMUM LEAD THICKNESS INCLUDES 3.
- LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS
- OF BASE MATERIAL. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE 4. BURRS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α	2.90	3.10	0.1142	0.1220
В	1.30	1.70	0.0512	0.0669
С	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
н	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
ĸ	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
м	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and 💷 are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910 Japan Customer Focus Center Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative