NCS2540

Triple 750 MHz Voltage Feedback Op Amp with Enable Feature

NCS2540 is a triple 750 MHz voltage feedback monolithic operational amplifier featuring high slew rate and low differential gain and phase error. The voltage feedback architecture allows for a superior bandwidth and low power consumption. This device features an enable pin.

Features

- −3.0 dB Small Signal BW (A_V = +2.0, V_O = 0.5 V_{p-p}) 750 MHz Typ
- Slew Rate 1700 V/μs
- Supply Current 13 mA/amp
- Input Referred Voltage Noise 5.0 nV/$\sqrt{Hz}$
- THD −64 dBc (f = 5.0 MHz, V_O = 2.0 V_{p-p})
- Output Current 100 mA
- Enable Pin Available
- These are Pb−Free Devices

Applications

- Line Drivers
- Radar/Communication Receivers

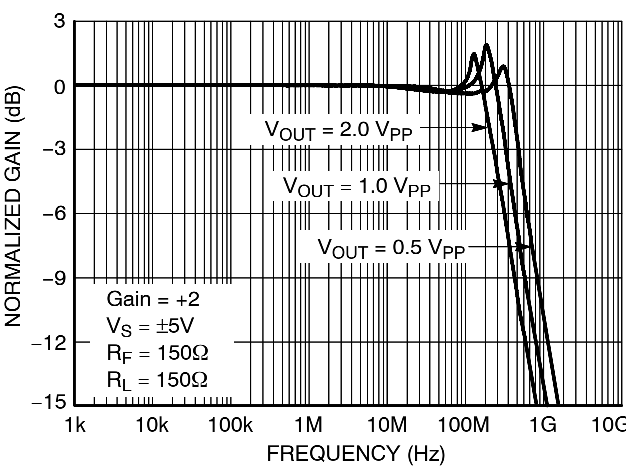

Figure 1. Frequency Response: Gain (dB) vs. Frequency Av = +2.0

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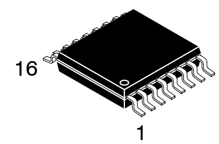
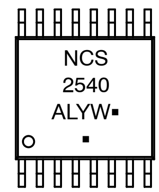
MARKING DIAGRAM



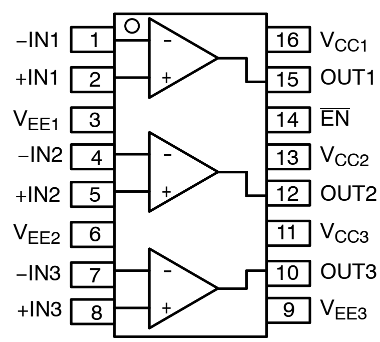
TSSOP−16
DT SUFFIX
CASE 948F



2540	= NCS2540
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

TSSOP−16 PINOUT



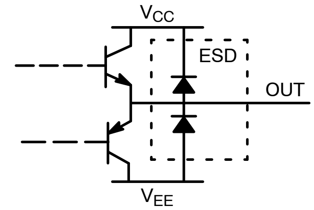
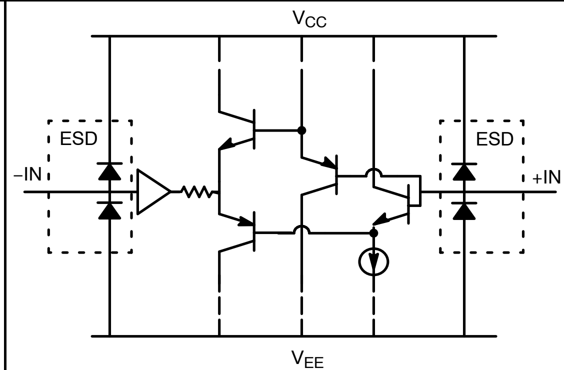
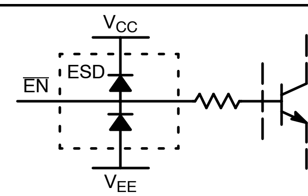
(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCS2540DTBG	TSSOP−16 (Pb−Free)	96 Units / Rail
NCS2540DTBR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Function	Equivalent Circuit
10, 12, 15	OUTx	Output	
3, 6, 9	V_{EE}	Negative Power Supply	
2, 5, 8	+INx	Non−inverted Input	
1, 4, 7	−INx	Inverted Input	See Above
11, 13, 16	V_{CC}	Positive Power Supply	
14	$\overline{EN}$	Enable	

ENABLE PIN TRUTH TABLE

	High	Low*
Enable	Disabled	Enabled

*Default open state

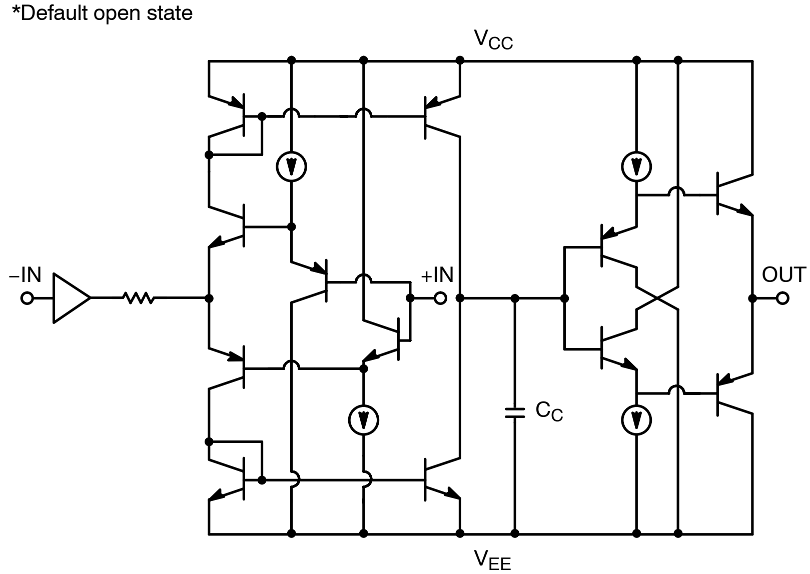


Figure 2. Simplified Device Schematic

ATTRIBUTES

Characteristics		Value
ESD Human Body Model Machine Model Charged Device Model		 2.0 kV 200 V 1.0 kV
Moisture Sensitivity (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_S	11	Vdc
Input Voltage Range	V_I	$\leq V_S$	Vdc
Input Differential Voltage Range	V_{ID}	$\leq V_S$	Vdc
Output Current	I_O	100	mA
Maximum Junction Temperature (Note 2)	T_J	150	°C
Operating Ambient Temperature	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−60 to +150	°C
Power Dissipation	P_D	(See Graph)	mW
Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	179	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. Power dissipation must be considered to ensure maximum junction temperature (T_J) is not exceeded.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated is limited by the associated rise in junction temperature. For the plastic packages, the maximum safe junction temperature is 150°C. If the maximum is exceeded momentarily, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in the “overheated” condition for an extended period can result in device damage.

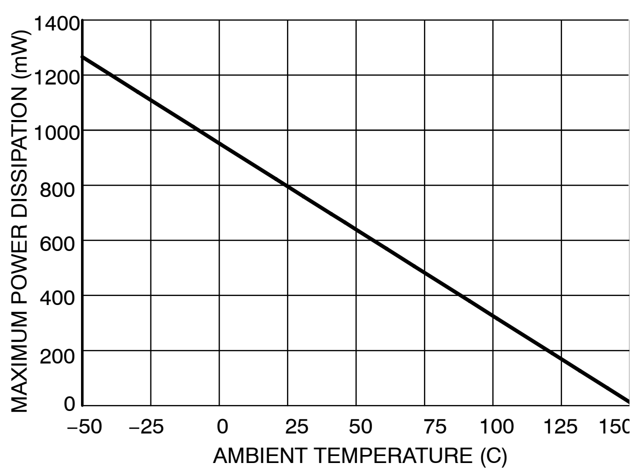


Figure 3. Power Dissipation vs. Temperature

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN PERFORMANCE						
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 2.0 V_{p-p}		 750 350		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		40		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.07		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.01		°
TIME DOMAIN RESPONSE						
SR	Slew Rate	A_V = +2.0, V_{step} = 2.0 V		1700		V/μs
t_s	Settling Time 0.1%	 A_V = +2.0, V_{step} = 2.0 V		 10		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 2.0 V		2.0		ns
t_{ON}	Turn−on Time			20		ns
t_{OFF}	Turn−off Time			40		ns
HARMONIC/NOISE PERFORMANCE						
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−64		dB
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−65		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 2.0 V_{p-p}		−75		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = 1.0 V_{p-p}		40		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 2.0 V_{p-p}		65		dBc
e_N	Input Referred Voltage Noise	f = 1.0 MHz		5.0		$nV/\sqrt{Hz}$
i_N	Input Referred Current Noise	f = 1.0 MHz		4.0		$pA/\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = –5.0 V, T_A = –40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{IO}	Input Offset Voltage (Note 3)		–10	0	+10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/°C
I_{IB}	Input Bias Current	V_O = 0 V		±3.2	±20	μA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Coefficient	V_O = 0 V		±40		nA/°C
V_{IH}	Input High Voltage (Enable) (Note 3)		3.0			V
V_{IL}	Input Low Voltage (Enable) (Note 3)				1.0	V
INPUT CHARACTERISTICS						
V_{CM}	Input Common Mode Voltage Range (Note 3)		±3.0	±3.2		V
CMRR	Common Mode Rejection Ratio (Note 3)	(See Graph)	40	50		dB
R_{IN}	Input Resistance			4.5		MΩ
C_{IN}	Differential Input Capacitance			1.0		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance			0.1		Ω
V_O	Output Voltage Range		±3.0	±4.0		V
I_O	Output Current		±50	±100		mA
POWER SUPPLY						
V_S	Operating Voltage Supply			10		V
$I_{S,ON}$	Power Supply Current – Enabled per amplifier (Note 3)		5.0	13	17	mA
$I_{S,OFF}$	Power Supply Current – Disabled per amplifier			0.1	0.3	mA
PSRR	Power Supply Rejection Ratio (Note 3)	(See Graph)	40	56		dB
	Crosstalk	Channel to Channel, f = 5 MHz		85		dB

3. Guaranteed by design and/or characterization.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
FREQUENCY DOMAIN PERFORMANCE						
BW	Bandwidth 3.0 dB Small Signal 3.0 dB Large Signal	 A_V = +2.0, V_O = 0.5 V_{p-p} A_V = +2.0, V_O = 1.0 V_{p-p}		 550 200		MHz
$GF_{0.1dB}$	0.1 dB Gain Flatness Bandwidth	A_V = +2.0		35		MHz
dG	Differential Gain	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.07		%
dP	Differential Phase	A_V = +2.0, R_L = 150 Ω, f = 3.58 MHz		0.02		°
TIME DOMAIN RESPONSE						
SR	Slew Rate	A_V = +2.0, V_{step} = 1.0 V		900		V/μs
t_s	Settling Time 0.1%	 A_V = +2.0, V_{step} = 1.0 V		 10		ns
t_r t_f	Rise and Fall Time	(10%−90%) A_V = +2.0, V_{step} = 1.0 V		1.7		ns
t_{ON}	Turn−on Time			20		ns
t_{OFF}	Turn−off Time			40		ns
HARMONIC/NOISE PERFORMANCE						
THD	Total Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−60		dB
HD2	2nd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−65		dBc
HD3	3rd Harmonic Distortion	f = 5.0 MHz, V_O = 1.0 V_{p-p}		−63		dBc
IP3	Third−Order Intercept	f = 10 MHz, V_O = 0.5 V_{p-p}		35		dBm
SFDR	Spurious−Free Dynamic Range	f = 5.0 MHz, V_O = 1.0 V_{p-p}		63		dBc
e_N	Input Referred Voltage Noise	f = 1.0 MHz		5.0		$nV/\sqrt{Hz}$
i_N	Input Referred Current Noise	f = 1.0 MHz		4.0		$pA/\sqrt{Hz}$

DC ELECTRICAL CHARACTERISTICS (V_{CC} = +2.5 V, V_{EE} = −2.5 V, T_A = −40°C to +85°C, R_L = 150 Ω to GND, R_F = 150 Ω, A_V = +2.0, Enable is left open, unless otherwise specified).

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{IO}	Input Offset Voltage (Note 4)		−10	0	+10	mV
$\Delta V_{IO}/\Delta T$	Input Offset Voltage Temperature Coefficient			6.0		μV/°C
I_{IB}	Input Bias Current	V_O = 0 V		±3.2	±20	μA
$\Delta I_{IB}/\Delta T$	Input Bias Current Temperature Coefficient	V_O = 0 V		±40		nA/°C
V_{IH}	Input High Voltage (Enable) (Note 4)		1.5			V
V_{IL}	Input Low Voltage (Enable) (Note 4)				0.5	V
INPUT CHARACTERISTICS						
V_{CM}	Input Common Mode Voltage Range (Note 4)		±1.1	±1.5		V
CMRR	Common Mode Rejection Ratio (Note 4)	(See Graph)	40	50		dB
R_{IN}	Input Resistance			4.5		MΩ
C_{IN}	Differential Input Capacitance			1.0		pF
OUTPUT CHARACTERISTICS						
R_{OUT}	Output Resistance			0.1		Ω
V_O	Output Voltage Range		±1.1	±1.5		V
I_O	Output Current		±50	±100		mA
POWER SUPPLY						
V_S	Operating Voltage Supply			5.0		V
$I_{S,ON}$	Power Supply Current – Enabled per amplifier		5.0	11	17	mA
$I_{S,OFF}$	Power Supply Current – Disabled per amplifier			0.1	0.3	mA
PSRR	Power Supply Rejection Ratio (Note 4)	(See Graph)	40	56		dB
	Crosstalk	Channel to Channel, f = 5 MHz		85		dB

4. Guaranteed by design and/or characterization.

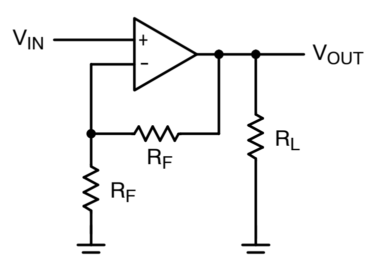


Figure 4. Typical Test Setup
(A_V = +2.0, R_F = 150 kΩ, R_L = 150 Ω)

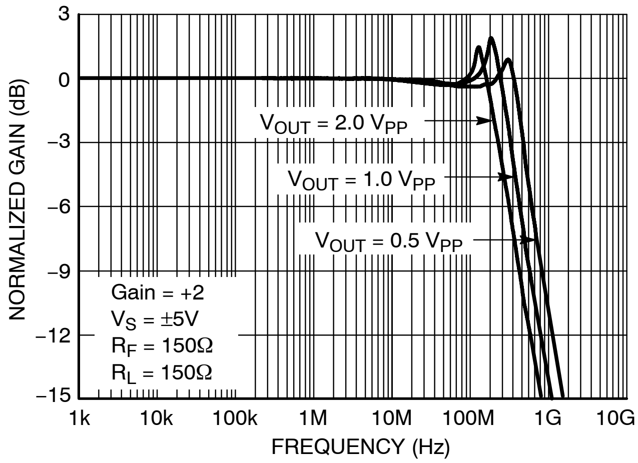


Figure 5. Frequency Response: Gain (dB) vs. Frequency Av = +2.0

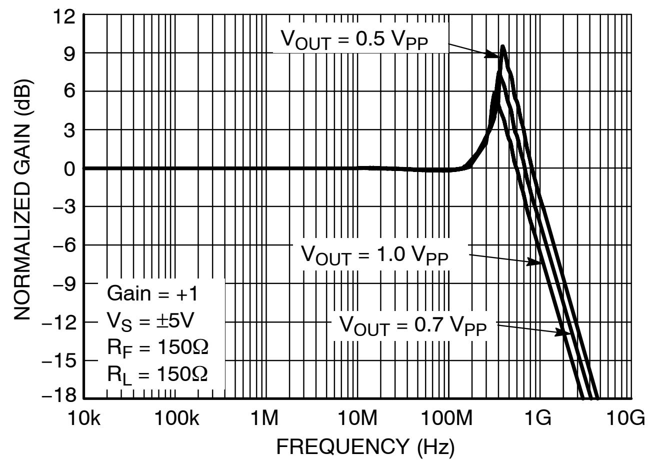


Figure 6. Frequency Response: Gain (dB) vs. Frequency Av = +1.0

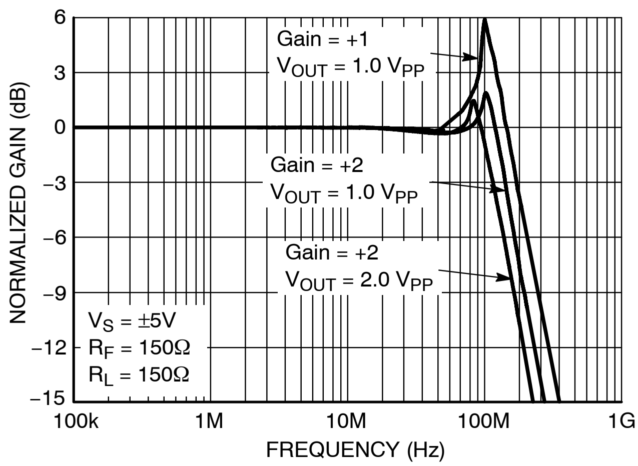


Figure 7. Large Signal Frequency Response Gain (dB) vs. Frequency

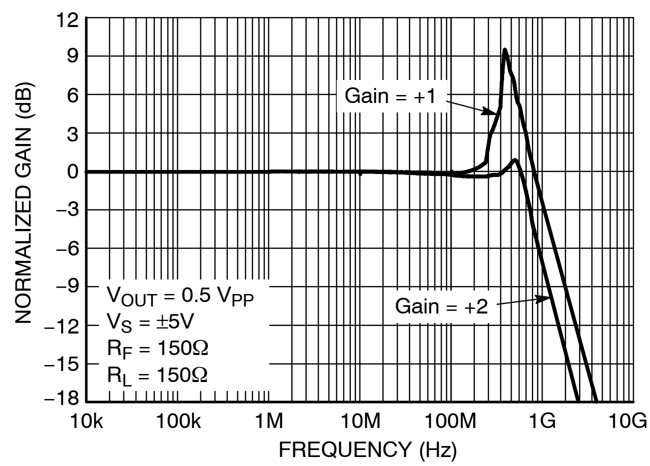


Figure 8. Small Signal Frequency Response Gain (dB) vs. Frequency

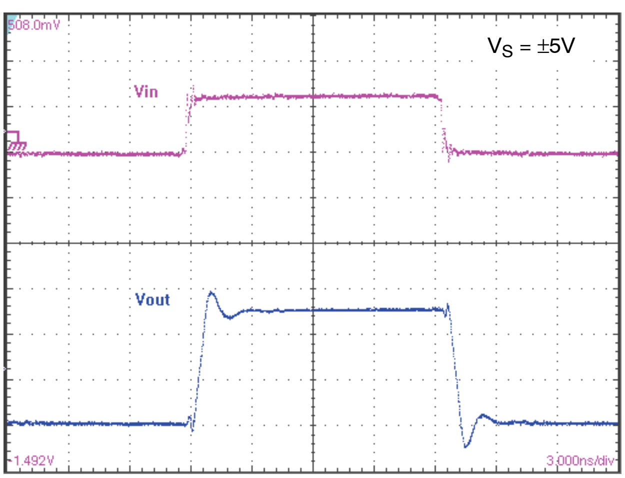


Figure 9. Small Signal Step Response Vertical: 20 mV/div Horizontal: 3 ns/div

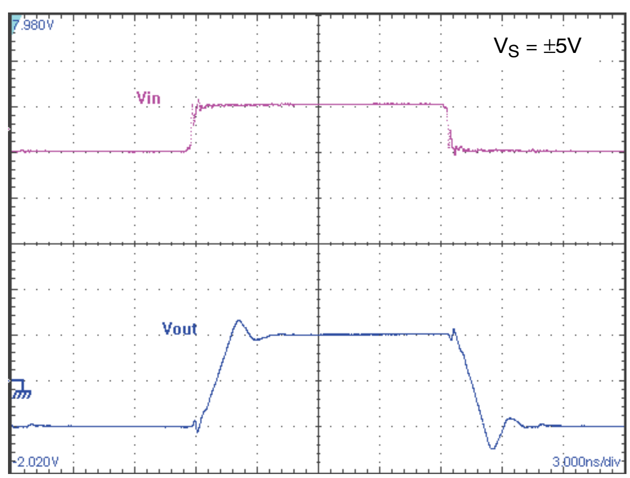


Figure 10. Large Signal Step Response Vertical: 1 V/div Horizontal: 3 ns/div

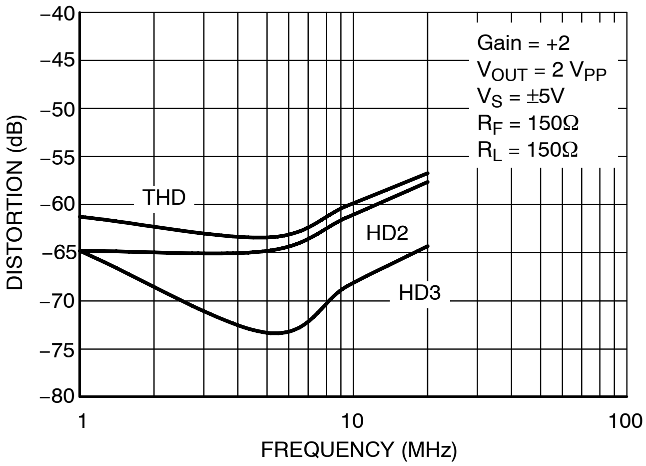


Figure 11. THD, HD2, HD3 vs. Frequency

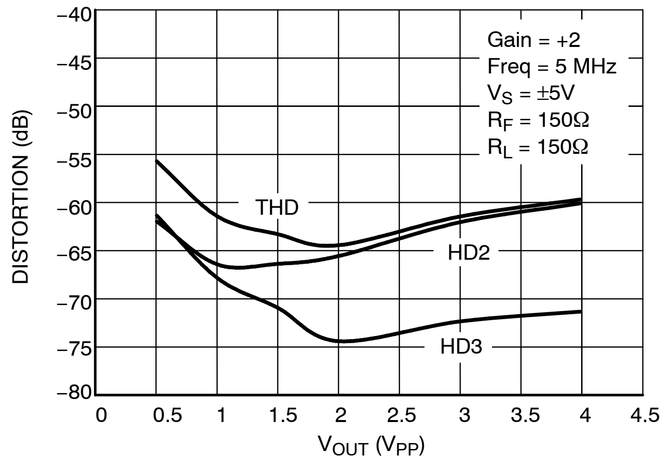


Figure 12. THD, HD2, HD3 vs. Output Voltage

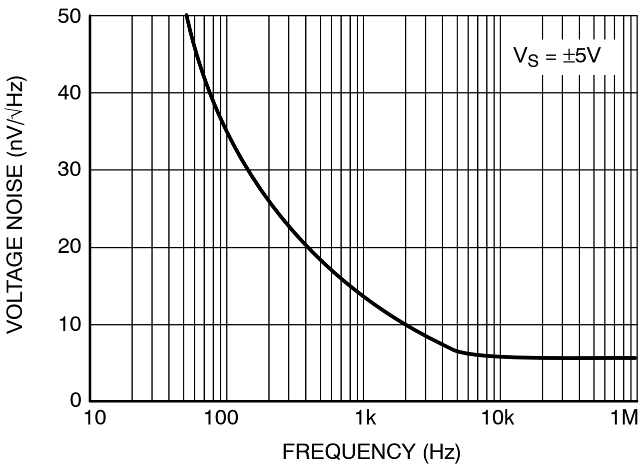


Figure 13. Input Referred Voltage Noise vs. Frequency

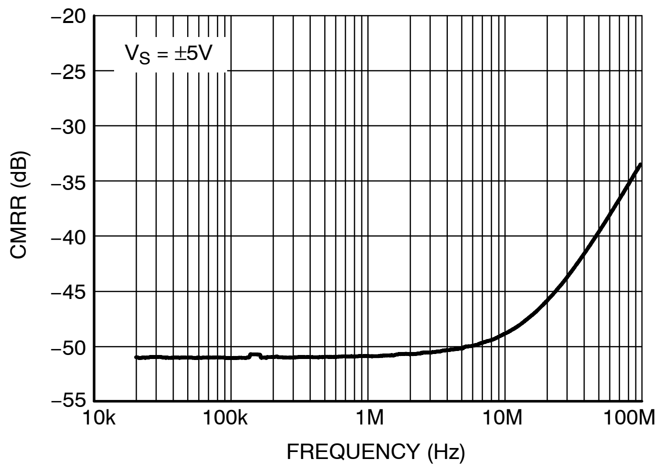


Figure 14. CMRR vs. Frequency

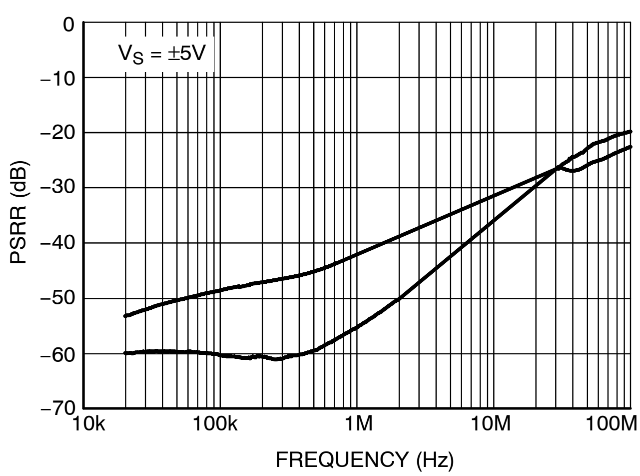


Figure 15. PSRR vs. Frequency

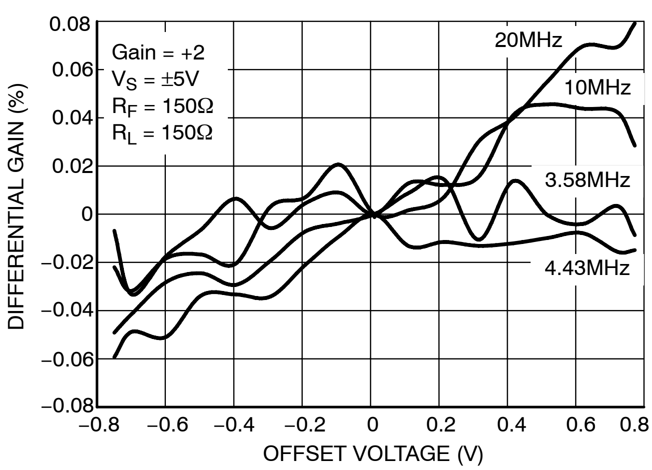


Figure 16. Differential Gain

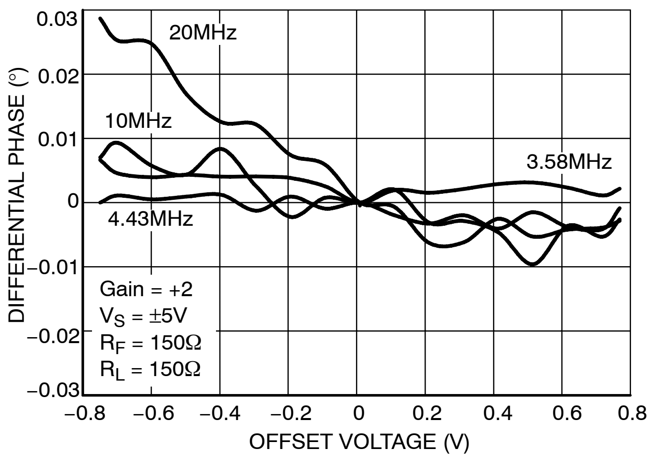


Figure 17. Differential Phase

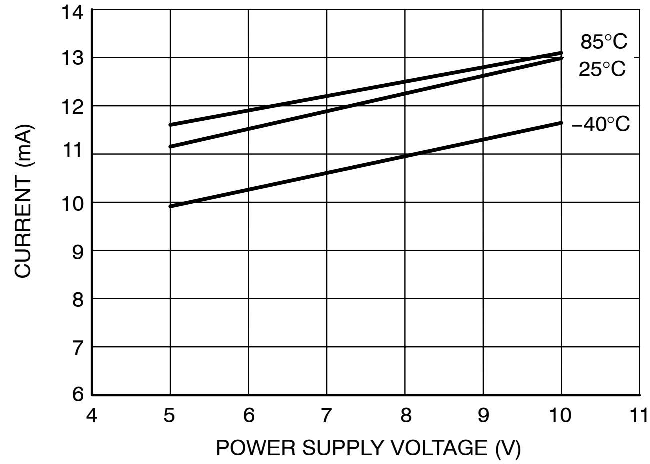


Figure 18. Supply Current Per Amplifier vs. Power Supply (Enabled)

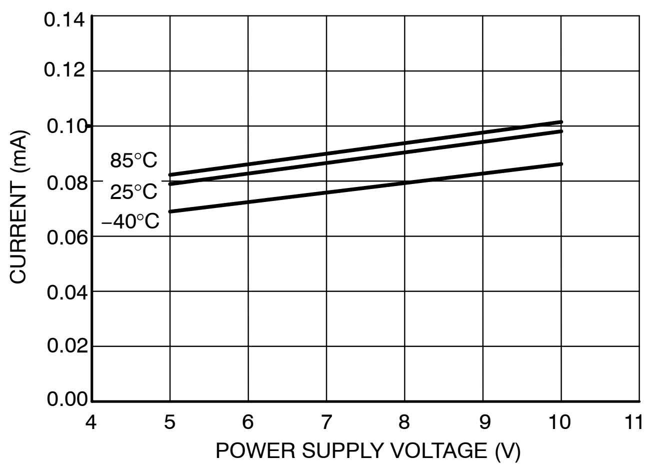


Figure 19. Supply Current Per Amplifier vs. Temperature (Disabled)

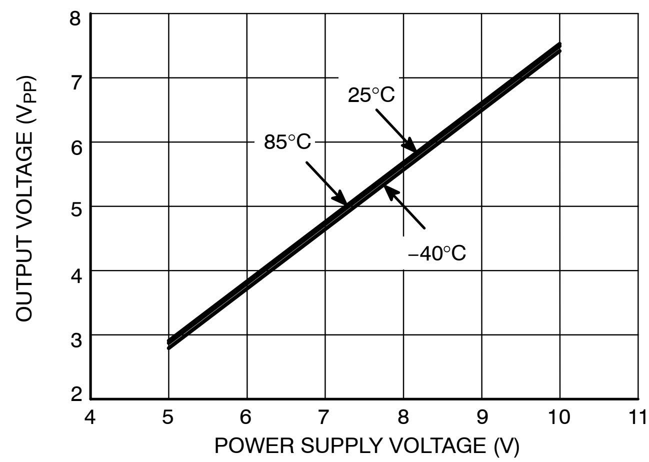


Figure 20. Output Voltage Swing vs. Supply Voltage

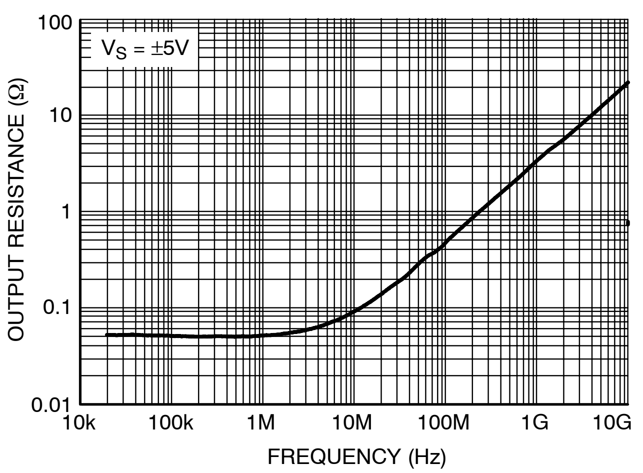


Figure 21. Output Resistance vs. Frequency

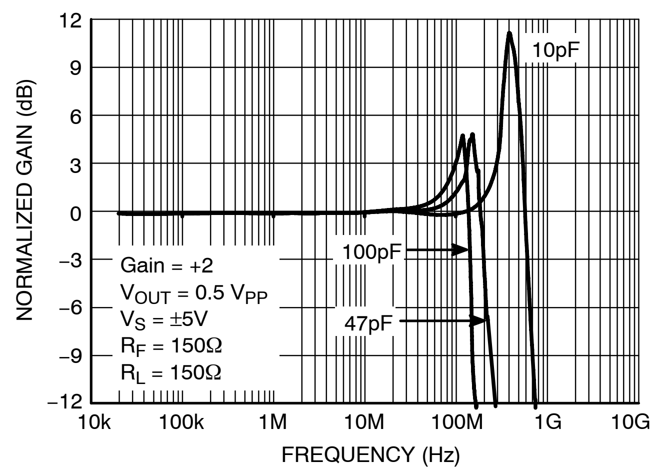


Figure 22. Frequency Response vs. Capacitive Load

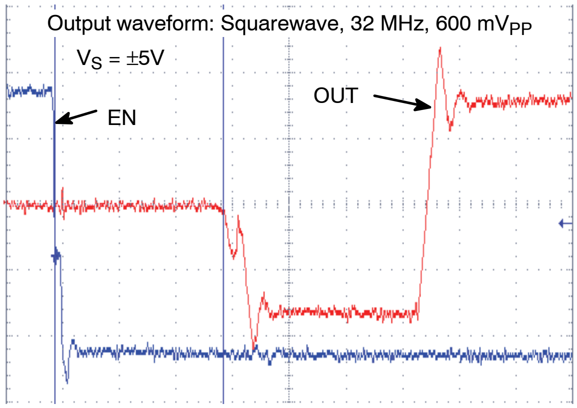


Figure 23. Turn ON Time Delay
Vertical: 500 mV/div (Enable), 200 mV/div (Output)
Horizontal: 5 ns/div

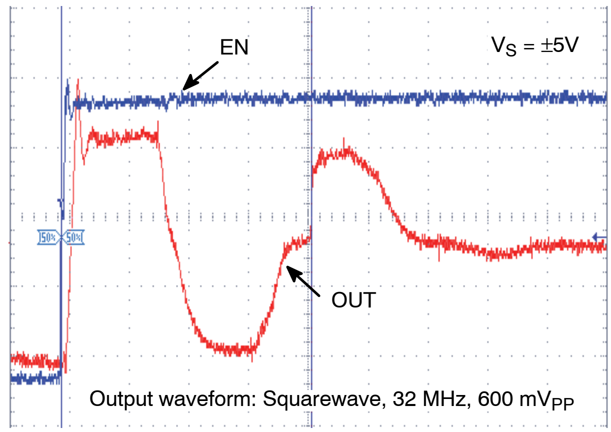


Figure 24. Turn OFF Time Delay
Vertical: 500 mV/div (Enable), 200 mV/div (Output)
Horizontal: 10 ns/div

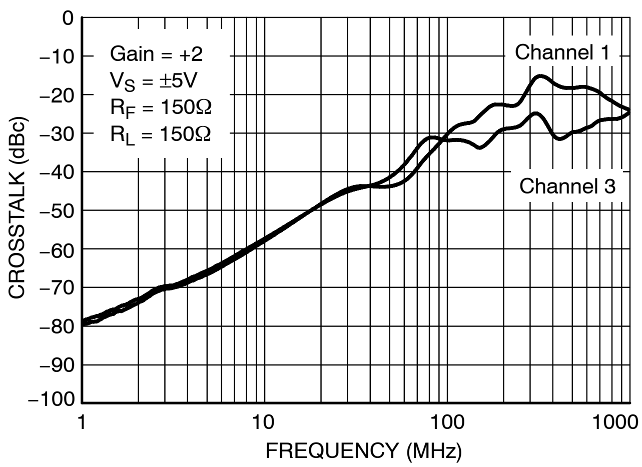


Figure 25. Crosstalk vs Frequency
(Crosstalk measured on Channel 2 with input signal on Channel 1 and 3)

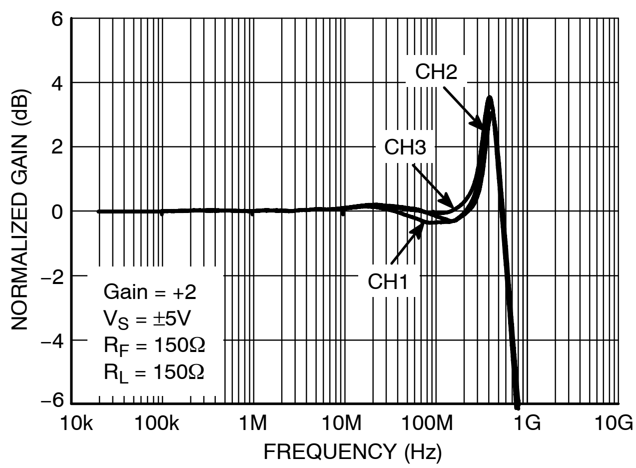


Figure 26. Channel Matching (dB) vs Frequency

Printed Circuit Board Layout Techniques

Proper high speed PCB design rules should be used for all wideband amplifiers as the PCB parasitics can affect the overall performance. Most important are stray capacitances at the output and inverting input nodes as it can effect peaking and bandwidth. A space (3/16″ is plenty) should be left around the signal lines to minimize coupling. Also, signal lines connecting the feedback and gain resistors should be short enough so that their associated inductance does not cause high frequency gain errors. Line lengths less than 1/4″ are recommended.

Video Performance

This device designed to provide good performance with NTSC, PAL, and HDTV video signals. Best performance is obtained with back terminated loads as performance is degraded as the load is increased. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage.

ESD Protection

All device pins have limited ESD protection using internal diodes to power supplies as specified in the attributes table (see Figure 27). These diodes provide moderate protection to input overdrive voltages above the supplies. The ESD diodes can support high input currents with current limiting series resistors. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response. Under closed−loop operation, the ESD diodes have no effect on circuit performance. However, under certain conditions the ESD diodes will be evident. If the device is driven into a slewing condition, the ESD diodes will clamp large differential voltages until the feedback loop restores closed−loop operation. Also, if the device is powered down and a large input signal is applied, the ESD diodes will conduct.

NOTE: Human Body Model for +IN and –IN pins are rated at 0.8kV while all other pins are rated at 2.0kV.

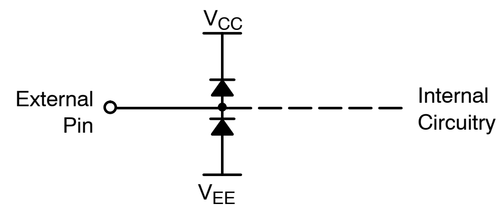
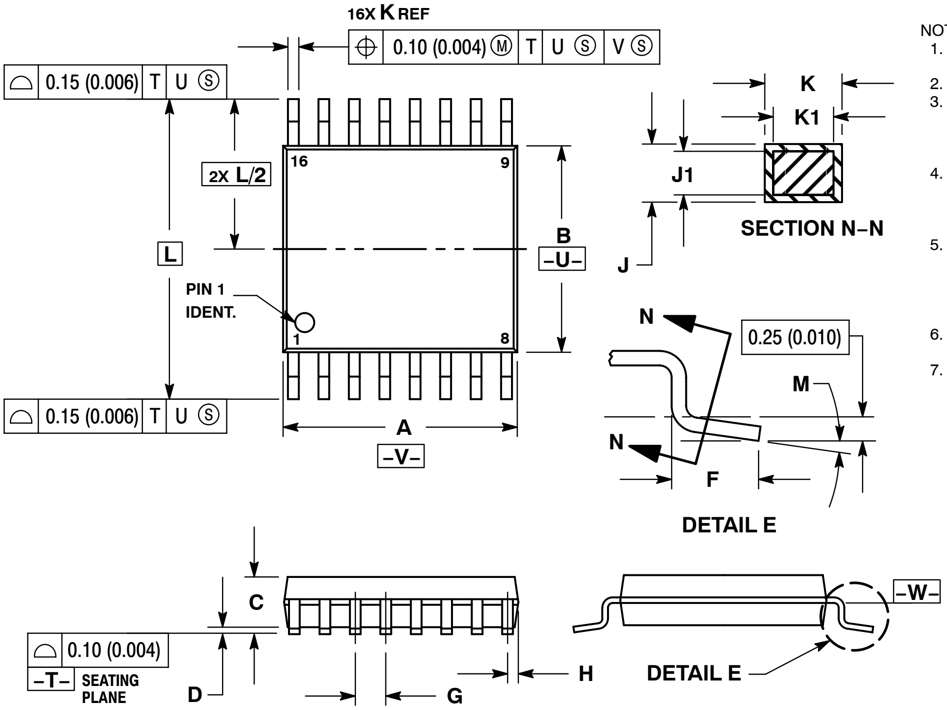


Figure 27. Internal ESD Protection

PACKAGE DIMENSIONS

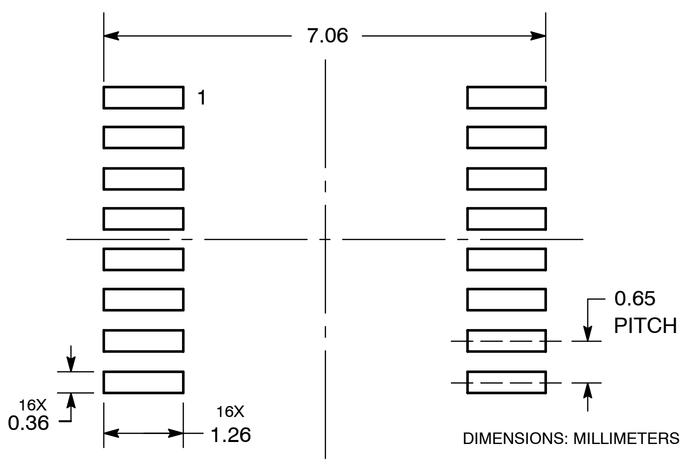
TSSOP−16
CASE 948F−01
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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