

# NTD60N03

## Power MOSFET 60 Amps, 28 Volts

### N-Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

#### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	28	Vdc
Gate-to-Source Voltage - Continuous	$V_{GS}$	$\pm 20$	Vdc
Drain Current - Continuous @ $T_C = 25^\circ\text{C}$ - Single Pulse ( $t_p = 10 \mu\text{s}$ )	$I_D$	60*	Adc
	$I_{DM}$	120	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	75	Watts
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to	$^\circ\text{C}$
		150	
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 28 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , $I_L = 17 \text{ Apk}$ , $L = 5.0 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	733	mJ
	Thermal Resistance		$^\circ\text{C/W}$
- Junction-to-Case	$R_{\theta JC}$	1.65	
- Junction-to-Ambient (Note 1)	$R_{\theta JA}$	67	
- Junction-to-Ambient (Note 2)	$R_{\theta JA}$	120	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

1. When surface mounted to an FR4 board using 1" pad size, (Cu Area 1.127 in<sup>2</sup>).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).

\*Chip current capability limited by package.

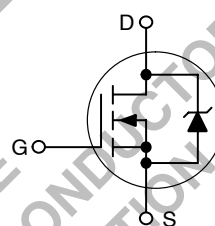


ON Semiconductor®

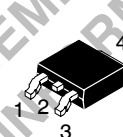
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
28 V	6.1 m $\Omega$	60 A

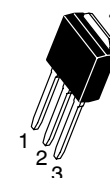
#### N-Channel



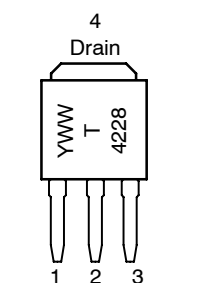
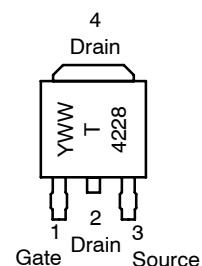
#### MARKING DIAGRAMS



DPAK  
CASE 369AA  
Style 2



DPAK  
CASE 369D  
Style 2



T4228 Device Code  
Y = Year  
WW = Work Week

1 2 3 Gate Drain Source

#### ORDERING INFORMATION

Device	Package	Shipping†
NTD60N03	DPAK	75 Units/Rail
NTD60N03T4	DPAK	2500 Tape & Reel
NTD60N03-1	DPAK Straight Lead	75 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTD60N03

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	28 -	30.6 25	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = 28 Vdc) (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = 28 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	±100	nAdc

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 -	1.9 -3.8	3.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 30 Adc) (V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 30 Adc) (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 10 Adc)	R <sub>DS(on)</sub>	- - -	6.1 9.2 6.4	7.5	mΩ
Forward Transconductance (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 10 Adc) (Note 3)	g <sub>FS</sub>	-	20	-	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 24 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	-	2150	-	pF
Output Capacitance		C <sub>oss</sub>	-	680	-	
Transfer Capacitance		C <sub>rss</sub>	-	260	-	

### SWITCHING CHARACTERISTICS (Note 4)

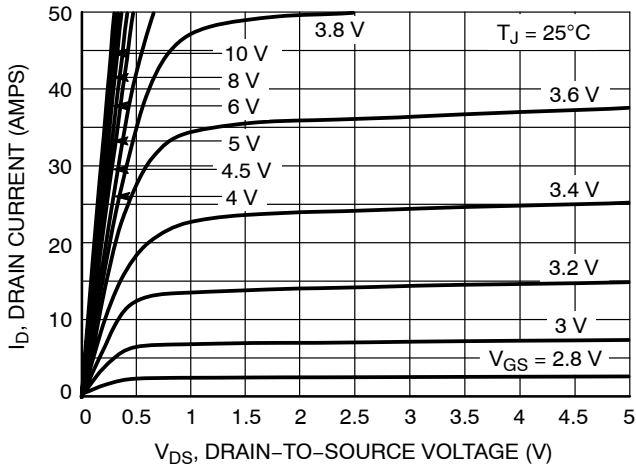
Turn-On Delay Time	(V <sub>DD</sub> = 15 Vdc, I <sub>D</sub> = 15 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 3.3 Ω)	t <sub>d(on)</sub>	-	10	-	ns
Rise Time		t <sub>r</sub>	-	18	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	32	-	
Fall Time		t <sub>f</sub>	-	15	-	
Gate Charge	(V <sub>DS</sub> = 24 Vdc, I <sub>D</sub> = 15 Adc, V <sub>GS</sub> = 4.5 Vdc) (Note 3)	Q <sub>T</sub>	-	30	-	nC
		Q <sub>1</sub>	-	6.5	-	
		Q <sub>2</sub>	-	18.4	-	

### SOURCE-DRAIN DIODE CHARACTERISTICS

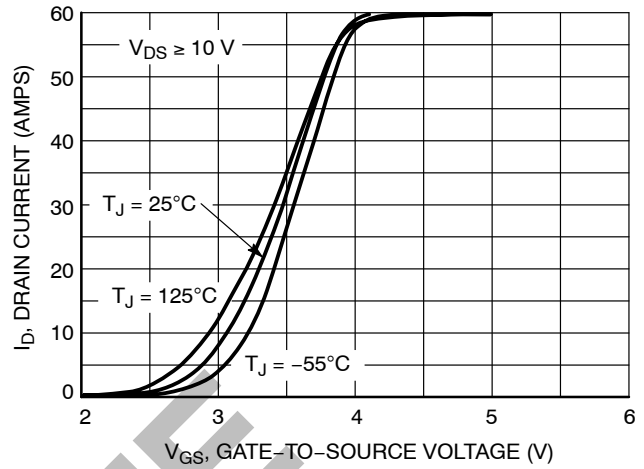
Forward On-Voltage (I <sub>S</sub> = 2.3 Adc, V <sub>GS</sub> = 0 Vdc) (Note 3) (I <sub>S</sub> = 30 Adc, V <sub>GS</sub> = 0 Vdc) (I <sub>S</sub> = 2.3 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	- - -	0.75 1.2 0.65	1.0 -	Vdc
Reverse Recovery Time  (I <sub>S</sub> = 2.3 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	-	39	-	ns
	t <sub>a</sub>	-	21	-	
	t <sub>b</sub>	-	18	-	
Reverse Recovery Stored Charge	Q <sub>rr</sub>	-	0.043	-	μC

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

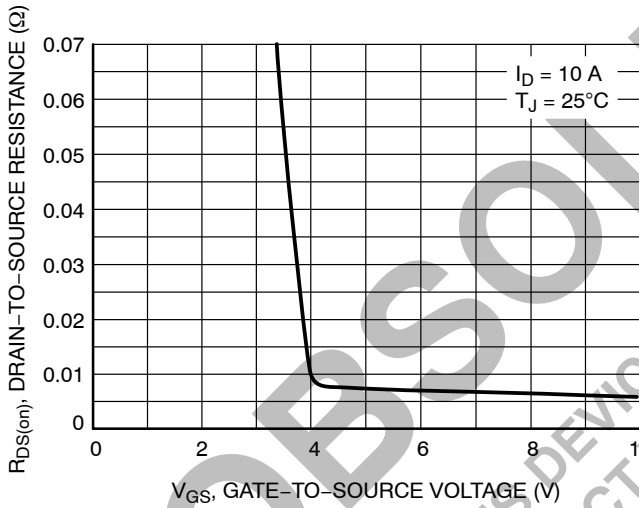
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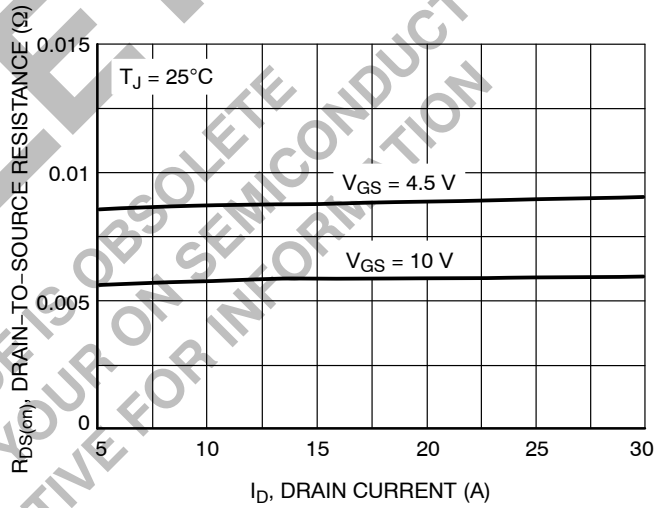
**Figure 1. On-Region Characteristics**



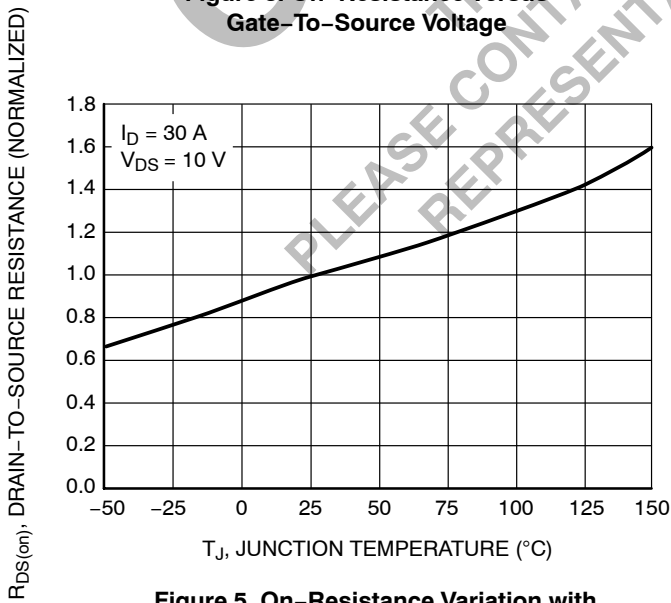
**Figure 2. Transfer Characteristics**



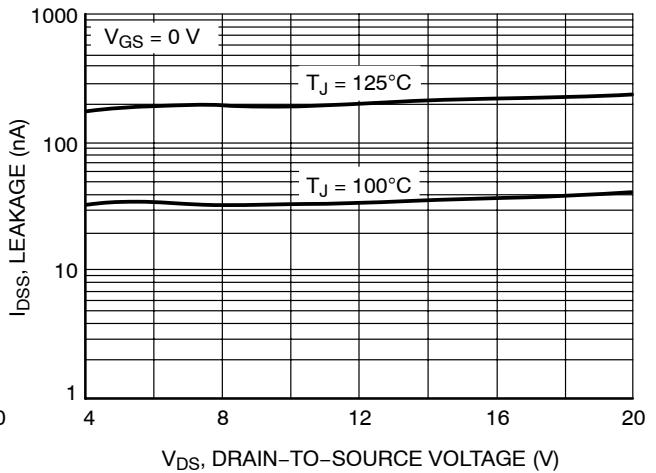
**Figure 3. On-Resistance versus Gate-to-Source Voltage**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

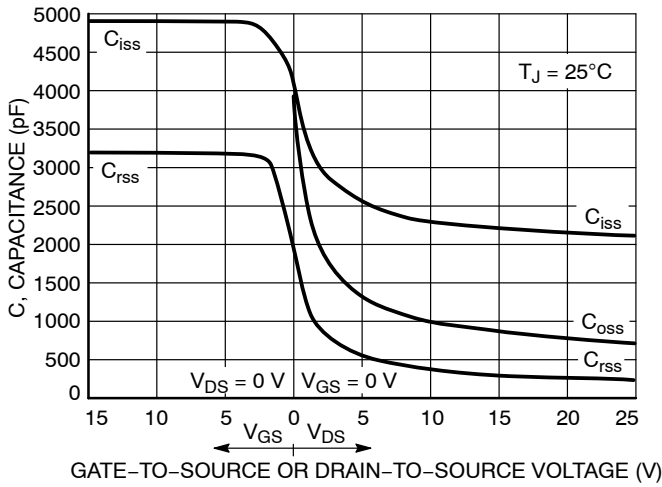


**Figure 5. On-Resistance Variation with Temperature**

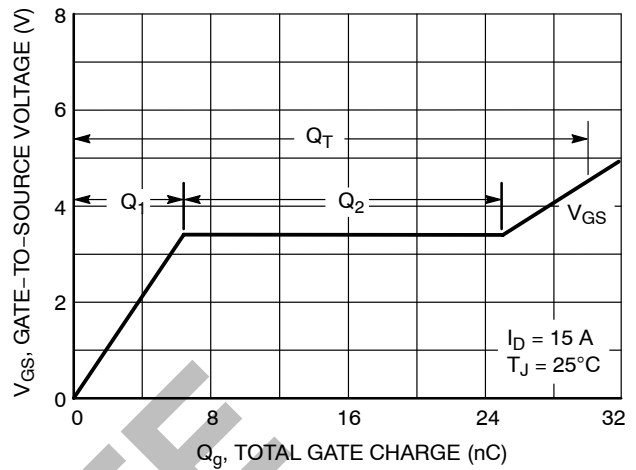


**Figure 6. Drain-to-Source Leakage Current versus Voltage**

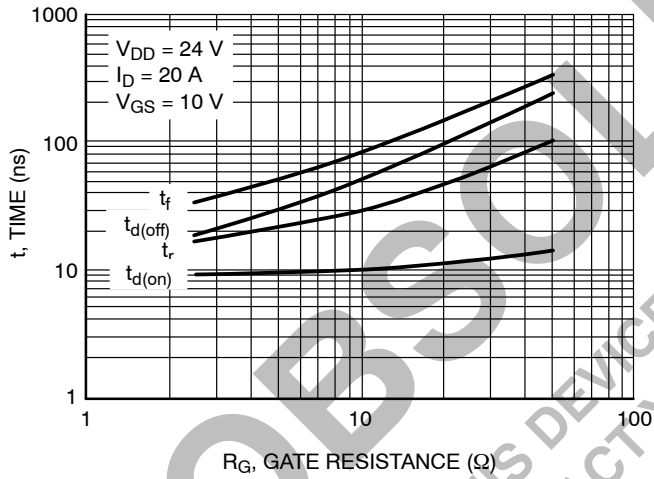
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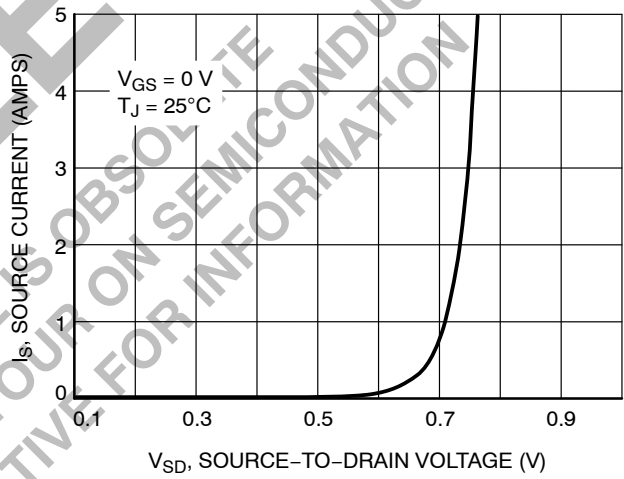
**Figure 7. Capacitance Variation**



**Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**

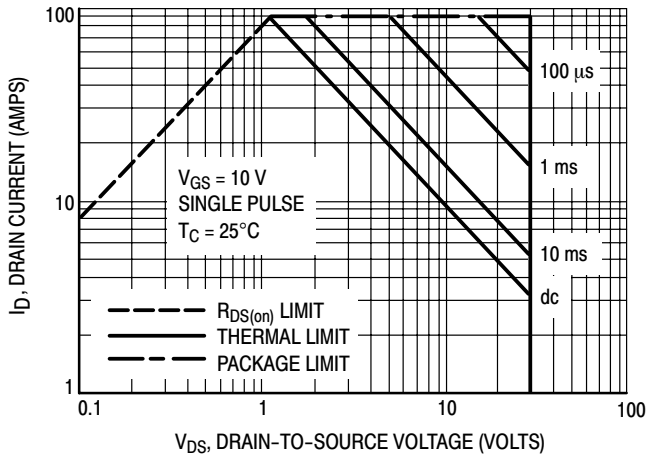


**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

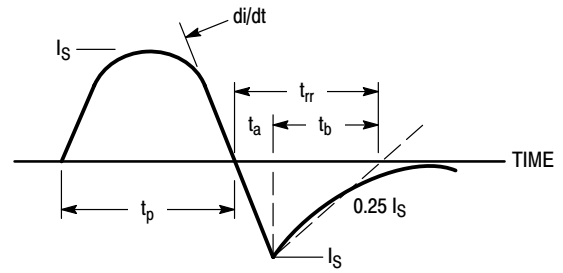


**Figure 10. Diode Forward Voltage versus Current**

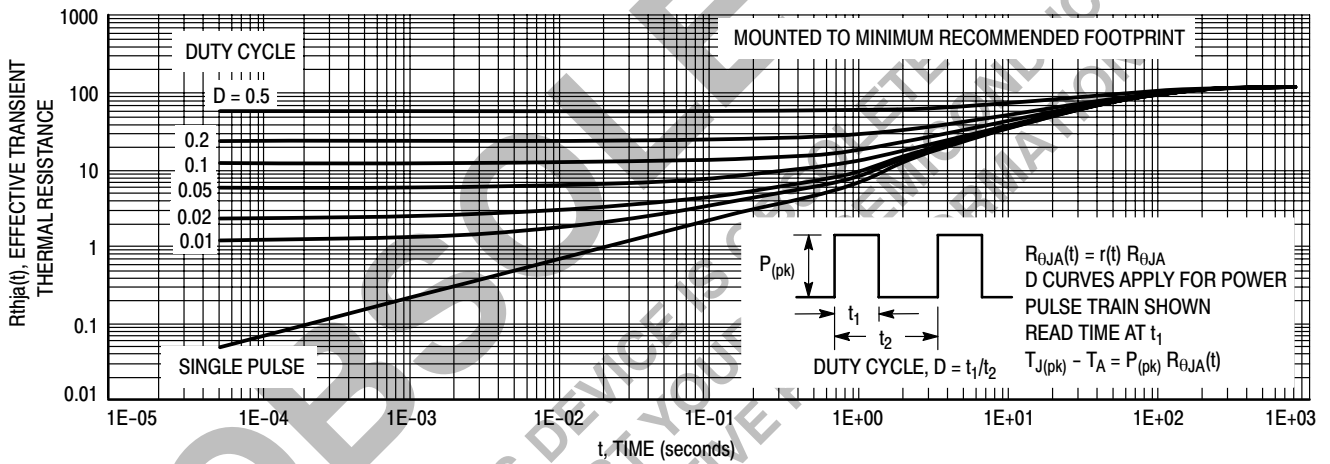
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**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Diode Reverse Recovery Waveform**



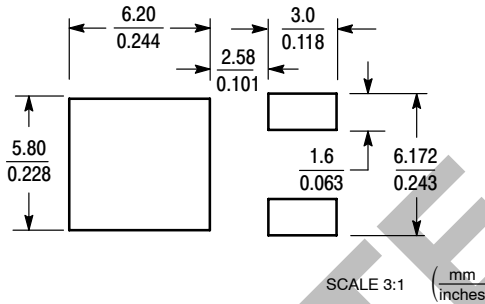
**Figure 13. Thermal Response - Various Duty Cycles**

**INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE**

**RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS**

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection

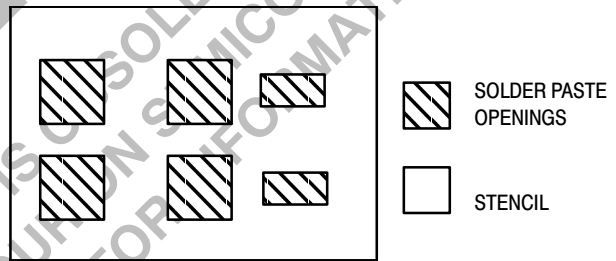
interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



**SOLDER STENCIL GUIDELINES**

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC-59, SC-70/SOT-323, SOD-123, SOT-23, SOT-143, SOT-223, SO-8, SO-14, SO-16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D<sup>2</sup>PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 14 shows a typical stencil for the DPAK and D<sup>2</sup>PAK packages. The

pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.



**Figure 14. Typical Stencil for DPAK and D<sup>2</sup>PAK Packages**

**SOLDERING PRECAUTIONS**

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.

- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

\* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D<sup>2</sup>PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows

temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

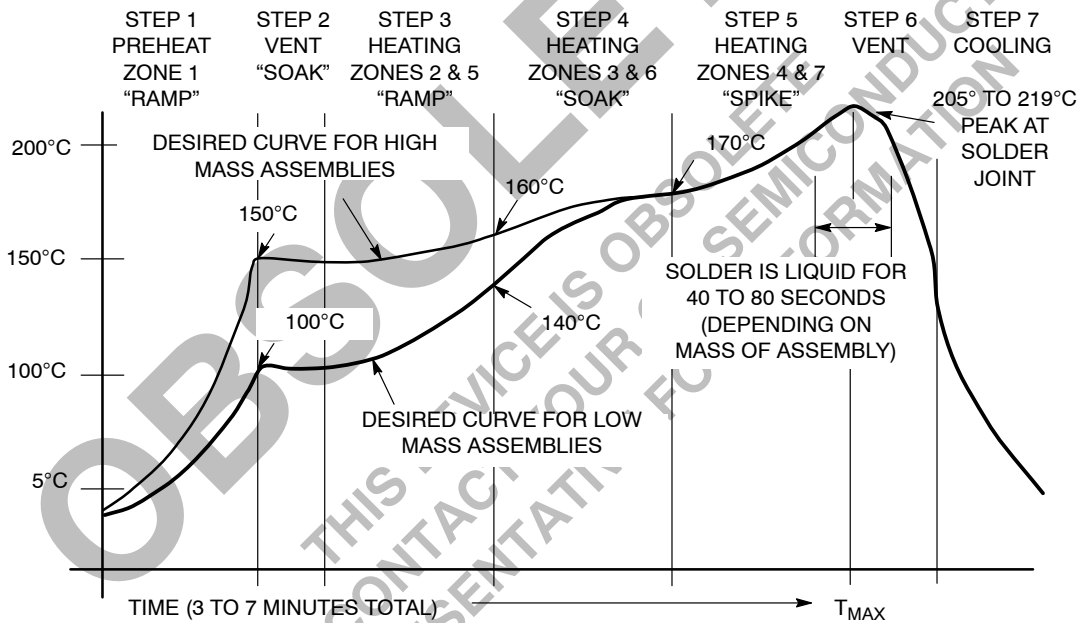
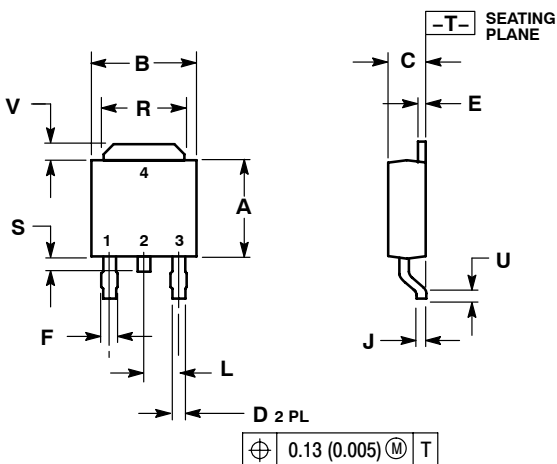


Figure 15. Typical Solder Heating Profile

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## PACKAGE DIMENSIONS

### DPAK CASE 369AA-01 ISSUE O

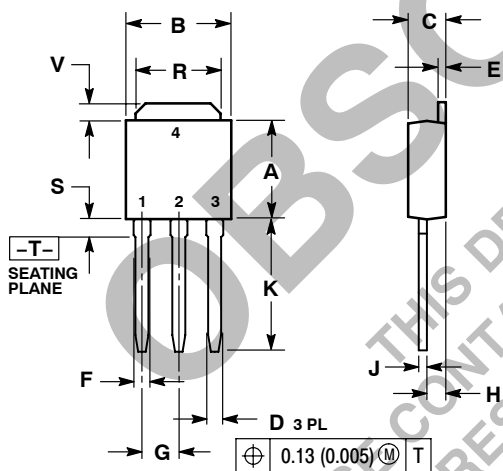


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.025	0.035	0.63	0.88
E	0.018	0.024	0.46	0.61
F	0.033	0.045	0.83	1.14
J	0.018	0.023	0.46	0.58
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

### DPAK CASE 369D-01 ISSUE O



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

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