

# NTL4502N

## Quad Power MOSFET

24 V, 15 A, N-Channel, PInPAK™ Package



ON Semiconductor®

<http://onsemi.com>

### Features

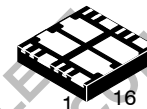
- Four N-Channel MOSFETs in a Single Package
- High Drain Current (Up to 80A per Device, Single Pulse  $t_p < 10 \mu\text{s}$ ,  $R_{\theta JC} = 1.5 \text{ }^\circ\text{C/W}$ )
- High Input Impedance for Ease of Drive
- Ultra Low On-resistance ( $R_{DS(on)}$ ) Provides Low Conduction Losses
- Very Fast Switching Times Provides Low Switching Losses
- Low Parasitic Inductance
- Low Stored Charge for Efficient Switching
- Very Low  $V_{SD}$  Ideal for Synchronous Rectification
- 200% Footprint Reduction Compared to Similar DPAK Solution for the Same Power
- Advanced Leadless Power Integrated Package (PInPAK)

### Applications

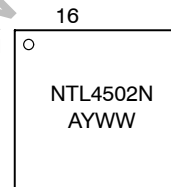
- DC-DC Converters
- Motherboard/Server Voltage Regulator
- Telecomm/Industrial Power Supply
- H-Bridge Circuits
- Low Voltage Motor Control

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX (Note 1)
24 V	8.0 m $\Omega$ @ 4.5 V	15 A
	11.2 m $\Omega$ @ 10 V	

### MARKING DIAGRAM



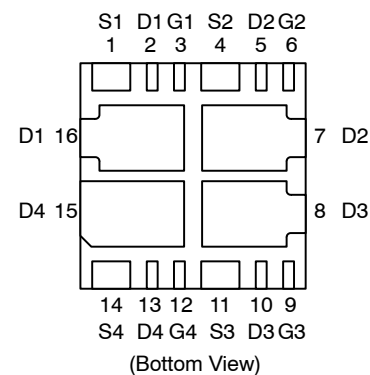
CASE 495  
PInPAK  
STYLE 1



xx = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Units	
Drain-to-Source Voltage	$V_{DSS}$	24	V	
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V	
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	15	A
		$T_A = 85^\circ\text{C}$	10.9	
	$t \leq 10 \text{ s}$	$T_A = 25^\circ\text{C}$	18.8	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	2.9	W
		$t \leq 10 \text{ s}$	4.5	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^\circ\text{C}$	11.4	A
		$T_A = 85^\circ\text{C}$	8.2	
Power Dissipation (Note 2)		$T_A = 25^\circ\text{C}$	1.7	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	32	A
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	15	A	
Single Pulse Drain-to-Source Avalanche Energy – ( $V_{DD} = 25 \text{ V}$ , $V_{GS} = 10 \text{ V}$ , $I_{PK} = 60 \text{ A}$ , $L = 0.1 \text{ mH}$ , $R_G = 1.0 \text{ k}\Omega$ )	EAS	80	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$	



### Pinout Diagram

### ORDERING INFORMATION

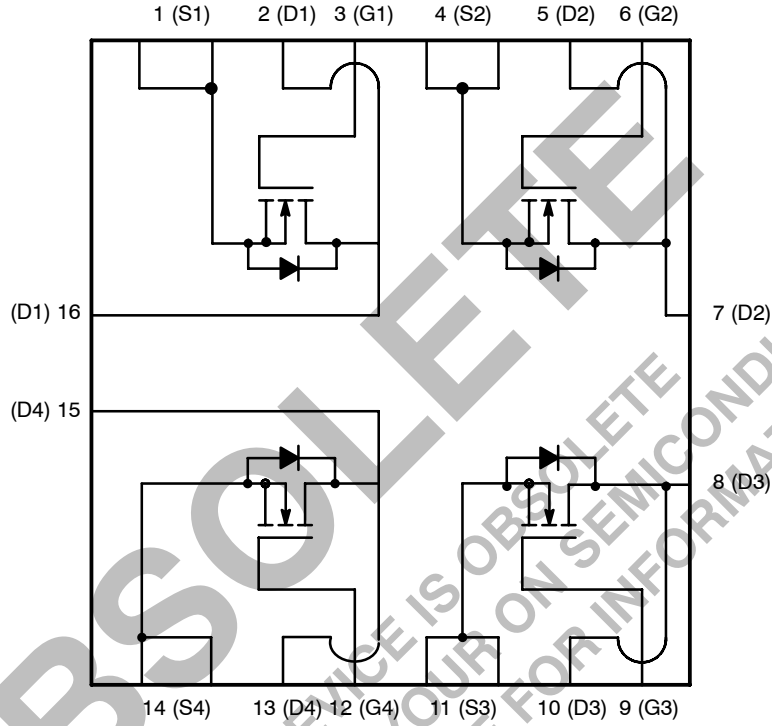
Device	Package	Shipping
NTL4502NT1	PInPAK	1500 / Reel

# NTL4502N

## THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction-to-Case (Drain)	$R_{\theta JC}$	1.5	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	43	
Junction-to-Ambient – $t_{\leq 10}$ s (Note 1)	$R_{\theta JA}$	27.5	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	75	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface-mounted on FR4 board using minimum recommended pad size (Cu area = 0.440 in sq).



**SCHEMATIC (TOP VIEW)**

# NTL4502N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	24	27.5		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			25.5		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> =25°C		1.5	μA
			T <sub>J</sub> =125°C		10	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.0	1.5	2.0	V
Gate Threshold Voltage Temperature Coefficient	V <sub>GS(th)</sub> /T <sub>J</sub>			-4.1		mV/°C
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A		11.2	13	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 15 A		8.0	11	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A		27		S

## CHARGES AND CAPACITANCES

Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz		1070	1605	pF
Output Capacitance	C <sub>oss</sub>			408	612	
Reverse Transfer Capacitance	C <sub>rss</sub>			142	213	
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A, V <sub>DS</sub> = 24 V		13		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			1.6		
Gate-to-Source Charge	Q <sub>GS</sub>			3.3		
Gate-to-Drain Charge	Q <sub>GD</sub>			7.0		

## SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 10 V (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 12 V, I <sub>D</sub> = 15 A, R <sub>G</sub> = 3.0 Ω		5.0	8.5	ns
Rise Time	t <sub>r</sub>			28	47	
Turn-Off Delay Time	t <sub>d(OFF)</sub>			22	37	
Fall Time	t <sub>f</sub>			6.0	10	

## SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 4.5 V (Note 4)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DD</sub> = 12 V, I <sub>D</sub> = 15 A, R <sub>G</sub> = 3.0 Ω		9.5	16	ns
Rise Time	t <sub>r</sub>			33	55	
Turn-Off Delay Time	t <sub>d(OFF)</sub>			14	23.5	
Fall Time	t <sub>f</sub>			7.5	12.5	

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 15 A	T <sub>J</sub> =25°C	0.8	1.2	V
			T <sub>J</sub> =125°C	0.7		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, di <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 15 A		31		ns
Charge Time	t <sub>a</sub>			17		
Discharge Time	t <sub>b</sub>			14		
Reverse Recovery Charge	Q <sub>RR</sub>			20		

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

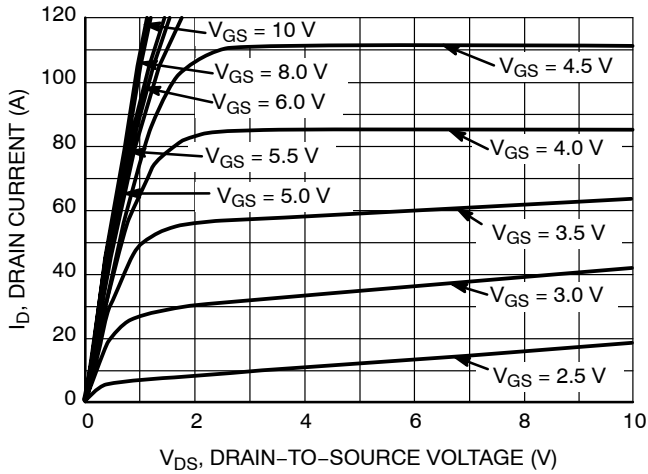


Figure 1. On-Region Characteristics

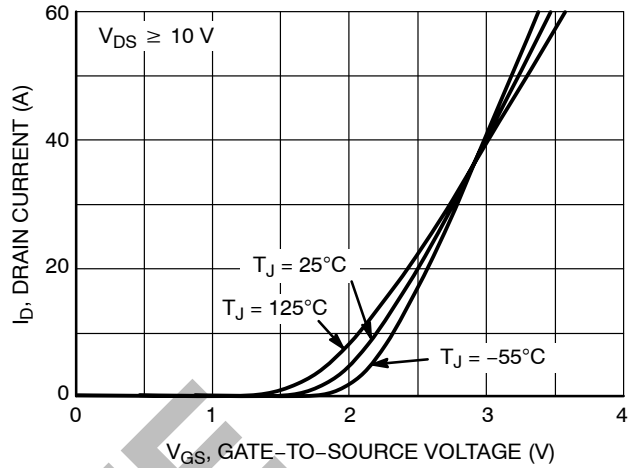


Figure 2. Transfer Characteristics

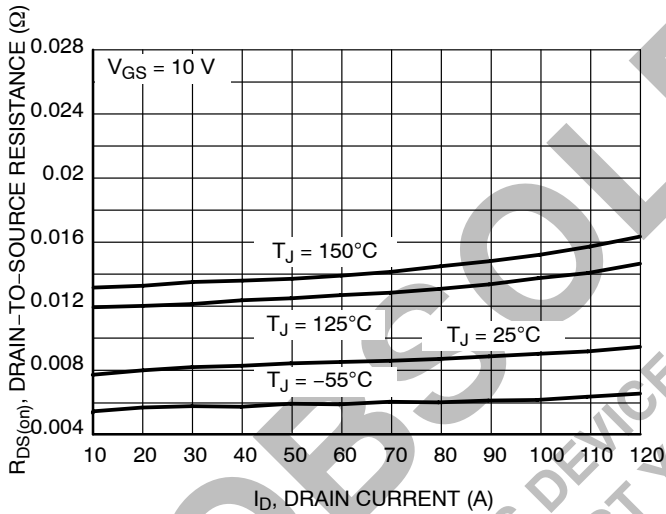


Figure 3. On-Resistance versus Drain Current and Temperature

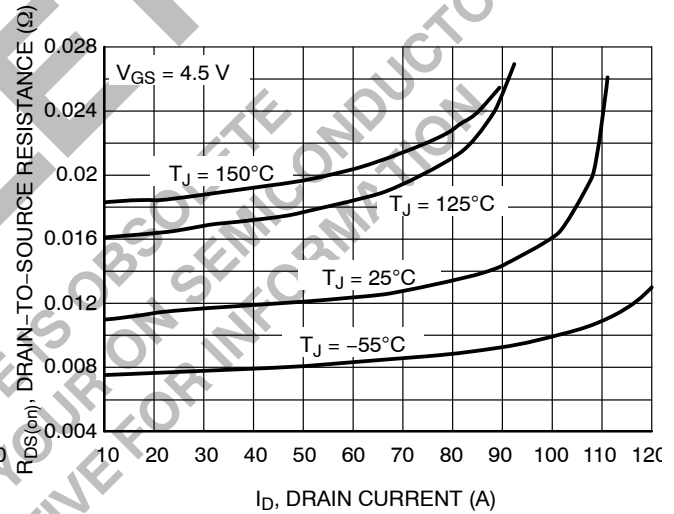


Figure 4. On-Resistance versus Drain Current and Temperature

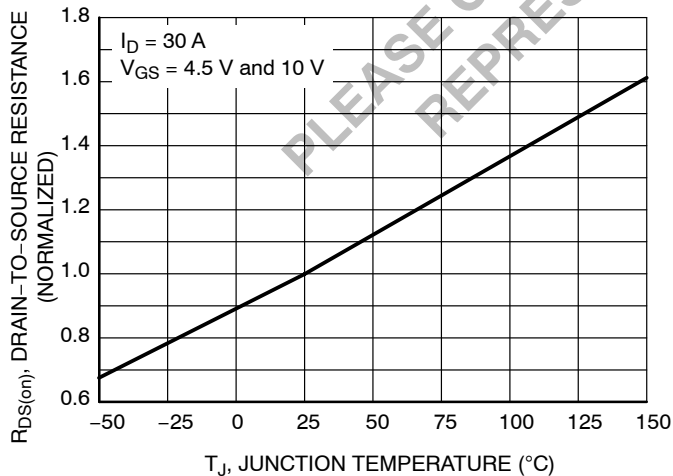


Figure 5. On-Resistance Variation with Temperature

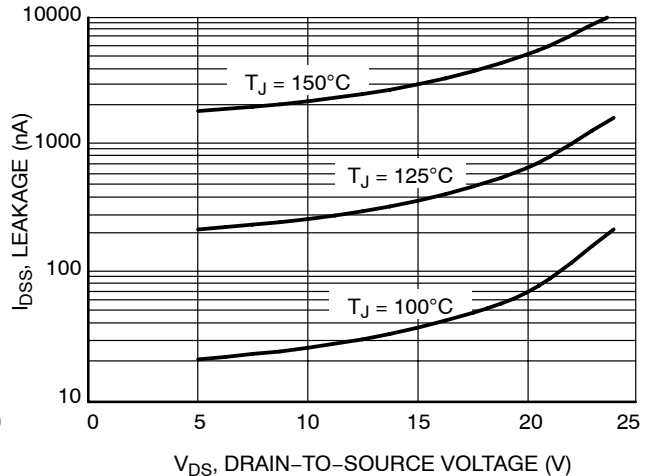


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTL4502N

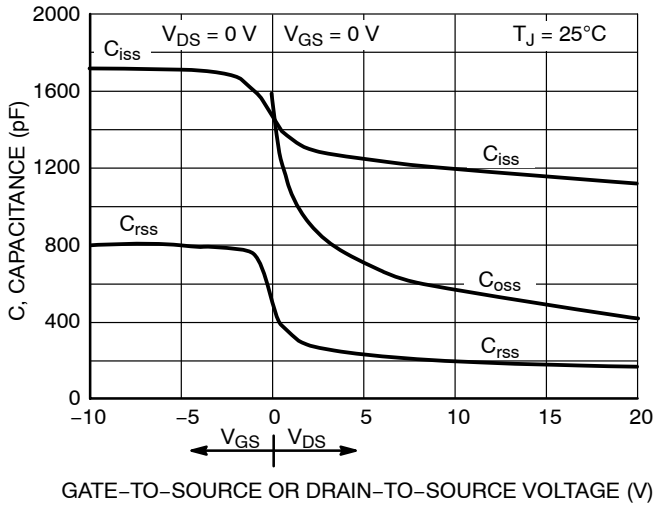


Figure 7. Capacitance Variation

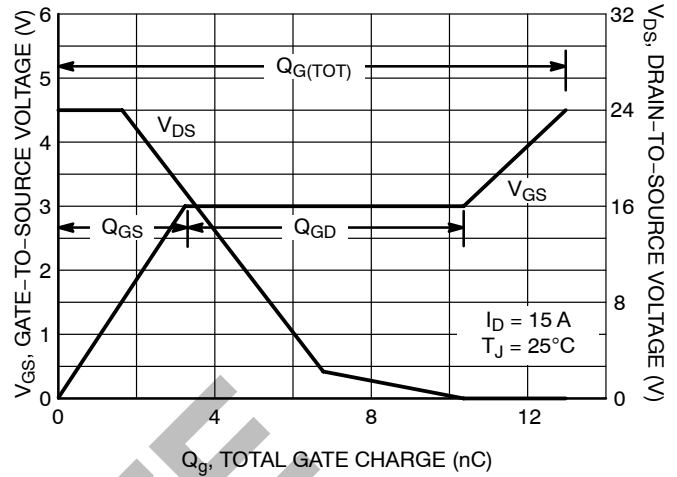


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

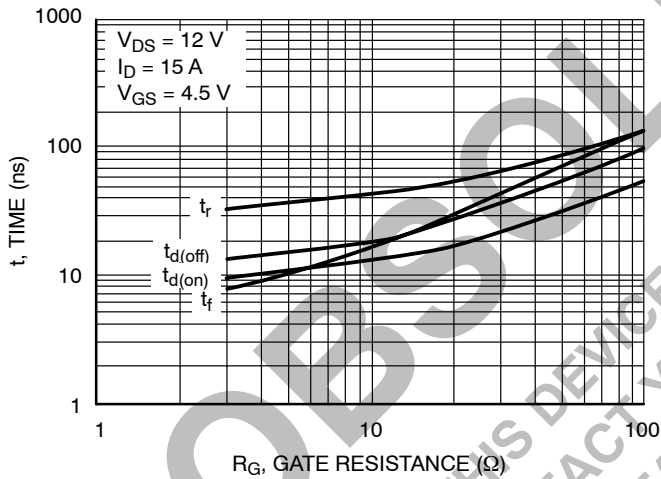


Figure 9. Resistive Switching Time Variation versus Gate Resistance

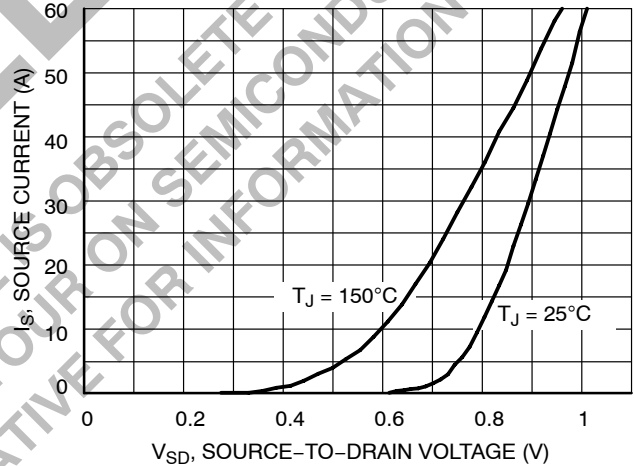


Figure 10. Diode Forward Voltage versus Current

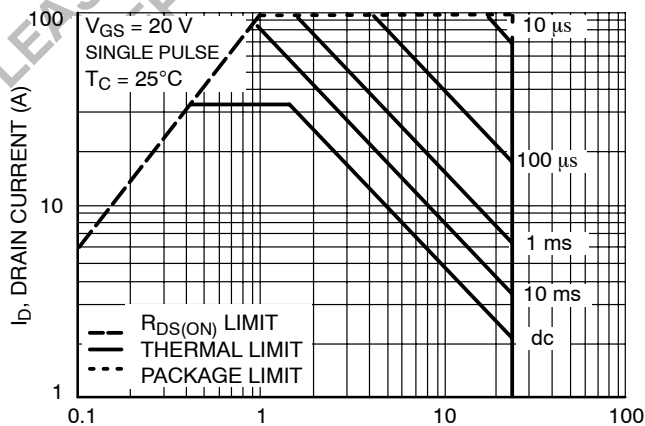
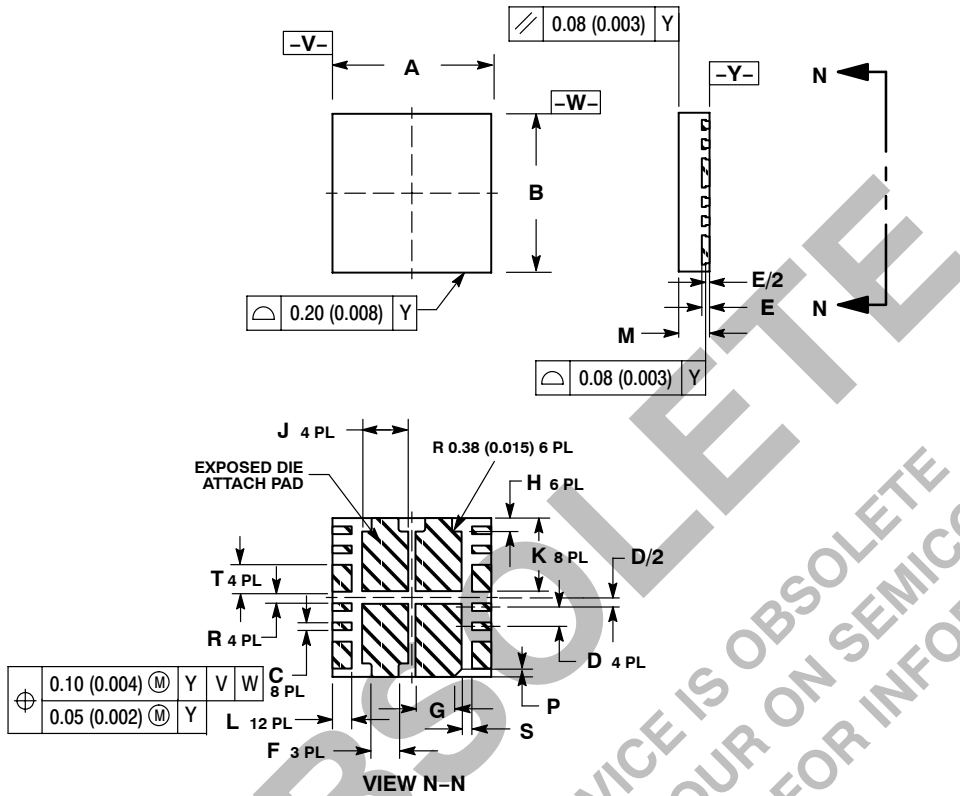


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NTL4502N

## PACKAGE DIMENSIONS

PlnPAK  
CASE 495-01  
ISSUE 0



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. COPLANARITY APPLIES TO LEAD, DIE ATTACHED PAD.
4. OPTIONAL FEATURES ARE FOR REFERENCE ONLY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.40	10.60	0.409	0.417
B	10.40	10.60	0.409	0.417
C	0.40	0.50	0.016	0.020
D	1.27 BSC		0.050 BSC	
E	0.50	0.52	0.020	0.020
F	1.70	1.90	0.067	0.075
G	2.45	2.55	0.096	0.100
H	0.80	1.00	0.031	0.039
J	2.90	3.10	0.114	0.122
K	4.75	4.95	0.187	0.195
L	1.10	1.30	0.043	0.051
M	2.00	2.20	0.079	0.087
P	0.30	0.50	0.012	0.020
R	0.70	0.90	0.028	0.035
S	0.58	0.78	0.023	0.031
T	1.68	1.78	0.066	0.070

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