P3P18S19B

Notebook LCD Panel EMI Reduction IC

ON Semiconductor®

www.onsemi.com

SOIC−8 NB
CASE 751

Product Description

The P3P18S19B is a Versatile Spread Spectrum Frequency Modulator designed specifically for input clock frequencies from 20 to 40 MHz. (Refer to “Input Frequency and Modulation Rate” Table). The P3P18S19B reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of downstream clock and data dependent signals. The P3P18S19B allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding, and other passive components that are traditionally required to pass EMI regulations.

The P3P18S19B modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘Spread Spectrum Clock Generation’.

The P3P18S19B uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

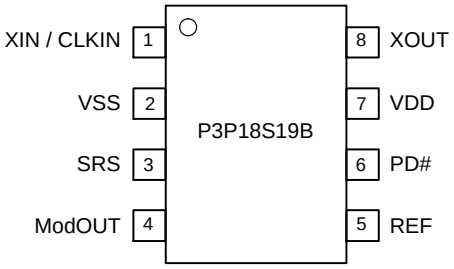
Applications

The P3P18S19B is targeted towards EMI management for memory and LVDS interfaces in mobile graphic chipsets and high−speed digital applications such as PC peripheral devices, consumer electronics, and embedded controller systems.

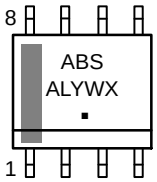
Features

- FCC Approved Method of EMI Attenuation
- Provides up to 15 dB EMI Reduction
- Generates a Low EMI Spread Spectrum Clock and a Non−spread Reference Clock of the Input Frequency
- Optimized for Frequency Range from 20 to 40 MHz
- Internal Loop Filter Minimizes External Components and Board Space
- Low Inherent Cycle−to−Cycle Jitter
- Two Spread % Selections: −1.25% to −1.75%
- 3.3 V Operating Voltage
- CMOS Design
- Supports Notebook VGA and other LCD Timing Controller Applications
- Power Down Function for Mobile Application
- Available in 8−pin SOIC Package
- These Devices are Pb−Free and are RoHS Compliant

PIN CONFIGURATION



MARKING DIAGRAM



ABS	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

Block Diagram

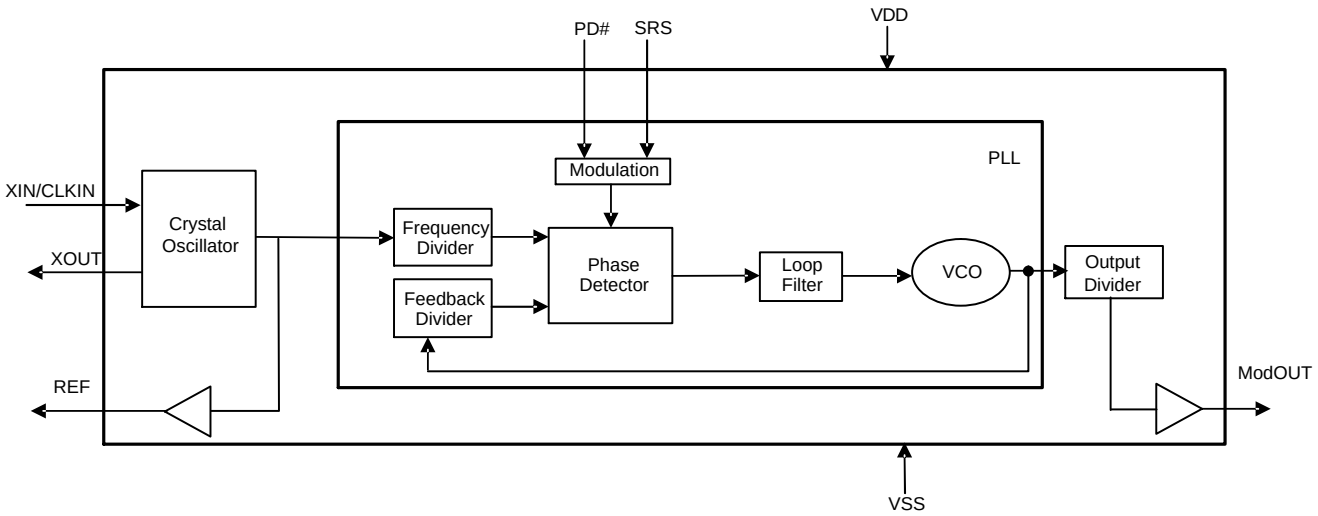


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	XIN / CLKIN	I	Crystal Connection or external frequency input. This pin has dual functions. It can be connected to either an external crystal or an external reference clock.
2	VSS	P	Ground Connection. Connect to system ground.
3	SRS	I	Spread range select. Digital logic input used to select frequency deviation (Refer to Spread Deviation Selection Table). This pin has an internal pullup resistor.
4	ModOUT	O	Spread spectrum clock output. (Refer to Input Frequency and Modulation Rate Table and Spread Deviation Selection Table)
5	REF	O	Non−modulated Reference clock output of the input frequency.
6	PD#	I	Power down control pin. Pull LOW to enable Power−Down mode. This pin has an internal pull−up resistor.
7	VDD	P	Power Supply for the entire chip.
8	XOUT	O	Crystal Connection. Input connection for an external crystal. If using an external reference, this pin must be left unconnected.

Table 2. INPUT FREQUENCY AND MODULATION RATE

Part Number	Input Frequency Range	Output Frequency Range	Modulation Rate
P3P18S19B	20 MHz to 40 MHz	20 MHz to 40 MHz	Input Frequency / 512

Table 3. SPREAD DEVIATION SELECTION

Part Number	SRS	Spread Deviation
P3P18S19B	0	−1.25% (DOWN)
	1	−1.75% (DOWN)

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22− A114−B)	2	KV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 5. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	Input Low voltage	VSS – 0.3		0.8	V
V_{IH}	Input High voltage	2.0		VDD + 0.3	V
I_{IL}	Input Low current (inputs PD#, SRS)	−60.0		−20.0	μA
I_{IH}	Input High current			1.0	μA
I_{XOL}	X_{OUT} Output low current @ 0.4 V, VDD = 3.3 V		3		mA
I_{XOH}	X_{OUT} Output high current @ 2.5 V, VDD = 3.3 V		3		mA
V_{OL}	Output Low voltage VDD = 3.3 V, I_{OL} = 20 mA			0.4	V
V_{OH}	Output High voltage VDD = 3.3 V, I_{OH} = 20 mA	2.5			V
I_{CC}	Dynamic supply current normal mode 3.3 V and 25 pF probe loading	7.1 $f_{IN\ -\ min}$		26.9 $f_{IN\ -\ max}$	mA
I_{DD}	Static supply current standby mode		4.5		mA
V_{DD}	Operating Voltage		3.3		V
t_{ON}	Power up time (first locked clock cycle after power up)		0.18		mS
Z_{OUT}	Clock Output impedance		50		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 6. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input Frequency	20		40	MHz
f_{OUT}	Output Frequency	20		40	MHz
t_{LH}*	Output Rise time (Measured from 0.8 V to 2.0 V)		0.66		nS
t_{HL}*	Output Fall time (Measured from 2.0 V to 0.8 V)		0.65		nS
t_{JC}	Jitter (Cycle−to−cycle)	−200		200	pS
t_D	Output Duty cycle	45	50	55	%

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

* t_{LH} and t_{HL} are measured into a capacitive load of 15 pF

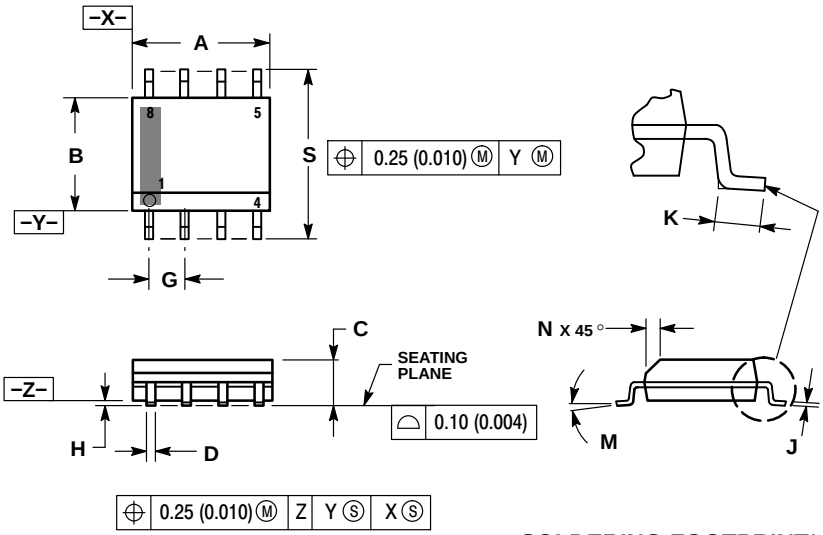
Table 7. ORDERING INFORMATION

Part Number	Marking	Package Type	Temperature
P3P18S19BF−08SR	ABS	8 pin SOIC, TAPE & REEL, Pb Free	0°C to +70°C

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

PACKAGE DIMENSIONS

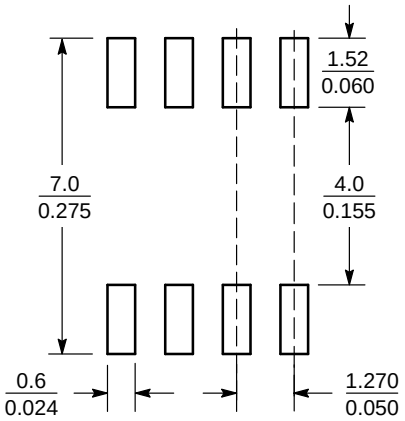
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
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Phone: 421 33 790 2910
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Phone: 81−3−5817−1050

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