ON Semiconductor®

PCS1P2860A

Multi-Output Clock Synthesizer

Features

- Generates multiple clock outputs from an inexpensive 25MHz crystal or external reference clock
- Frequency outputs:
  - o 25MHz Reference clock
  - o 125MHz
  - o 127MHz
- Zero ppm frequency synthesis error for all CLK outputs
- 3.3V ± 5%V Supply Voltage
- Low jitter design
- Packaged in 16-pin TSSOP
- Compatible with CY22393XC-MZ2
- Advanced CMOS process

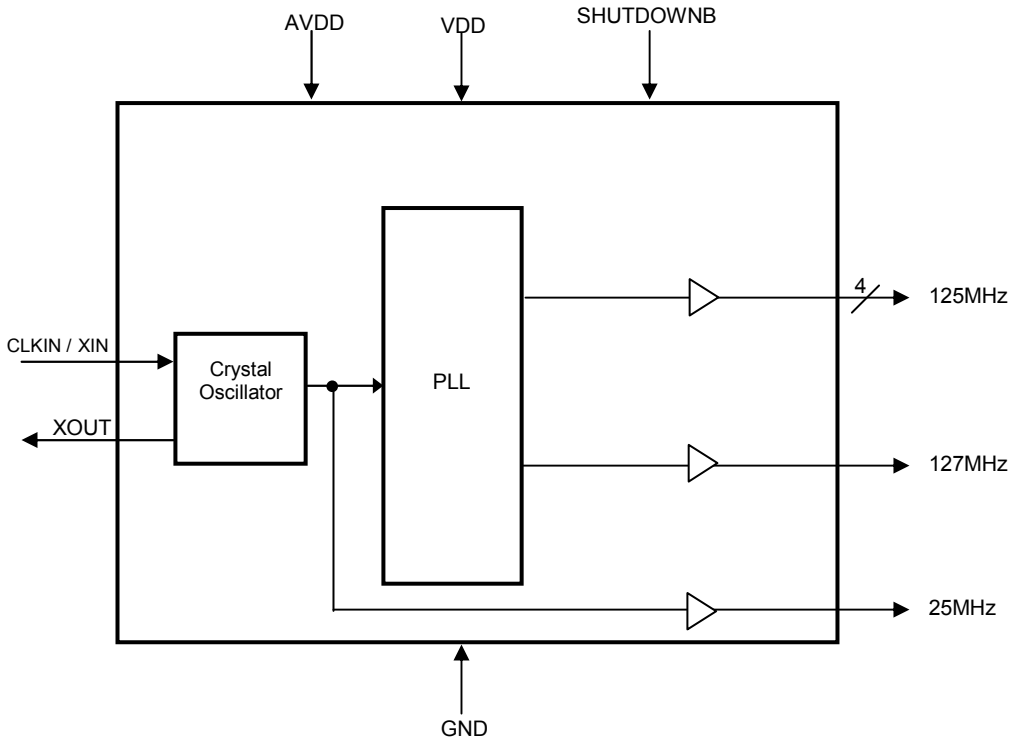
Product Description

The PCS1P2860A is a Precision multi-PLL based frequency synthesizer. Six Clock outputs are generated using an inexpensive 25MHz Crystal or external reference clock. The outputs consist of 25MHz Refout, 127MHz and four 125MHz clocks. SHUTDOWNB signal tri-states all the clocks when enabled. The device operates from a Supply Voltage of 3.3V ± 5%V. The device is available in a 16-pin TSSOP JEDEC package.

Application

PCS1P2860A is targeted for use in high-end multimedia, communications and consumer applications.

Block Diagram



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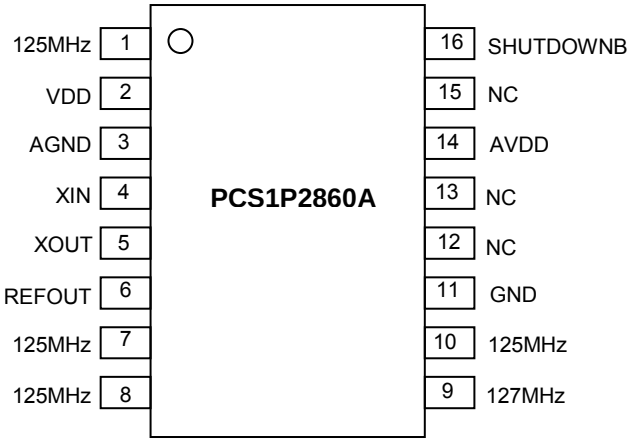
PCS1P2860/D

Pin Diagram



Pin Description

Pin #	Pin Name	Pin Type	Pin Description
1	125MHz	Output	125MHz Clock Output.
2	VDD	Power	Connect to +3.3V.
3	AGND	Power	Connect to ground.
4	XIN	Input	Crystal connection or external reference frequency input. It can be connected to a 25MHz Fundamental mode crystal.
5	XOUT	Output	Connection to crystal. If using an external reference clock, this pin must be left unconnected.
6	REFOUT	Output	25MHz Reference Clock output.
7	125MHz	Output	125MHz Clock Output.
8	125MHz	Output	125MHz Clock Output.
9	127MHz	Output	127MHz Clock Output.
10	125MHz	Output	125MHz Clock Output.
11	GND	Power	Connect to ground.
12	NC		No connection.
13	NC		No connection.
14	AVDD	Power	Connect to +3.3V.
15	NC		No connection.
16	SHUTDOWNB	Input	Output Enable bit. When this pin is made HIGH, all clocks are enabled. Tri-states all clocks when this pin is LOW.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD	Power Supply Voltage relative to Ground	-0.5 to +4.6	V
V_{IN}	Input Voltage relative to Ground (Input Pins)	-0.5 to VDD+0.3	
T_{STG}	Storage temperature	-65 to +150	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	125	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
VDD / AVDD	Operating Voltage	3.135	3.3	3.465	V
T_A	Operating Temperature (Ambient Temperature)	0		70	℃
C_L	Load Capacitance			15	pF
C_{IN}	Input Capacitance		5		pF

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VDD / AVDD	Operating Voltage		3.135	3.3	3.465	V
V_{IH}	Input High Voltage		2.2		VDD+0.3	V
V_{IL}	Input Low Voltage		GND-0.3		1.0	V
I_{IH}	Input HIGH current	VIN = VDD			30	µA
I_{IL}	Input LOW current	VIN = GND			50	µA
V_{OH}	Output High Voltage	VDD = 3.135, I_{OH} = -12mA	2.4			V
V_{OL}	Output Low Voltage	VDD = 3.135, I_{OL} = 12mA			0.4	V
I_{OZ}	Output Leakage Current	Three-state outputs			10	µA
I_{CC}	Static Current	CLKIN and SHUTDOWNB Pins pulled low			5.5	mA
I_{DD}	Dynamic Current	No Load, All Clocks on		35		mA
Z_{OUT}	Nominal output impedance			30		Ω

AC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
CLKIN / XIN	Input Frequency			25		MHz
CLK OUT	Output Frequency	Pin 6		25		MHz
		Pin 1,7,8,10		125		
		Pin 9		127		
t_{LH}[1]	Rising edge slew rate (Measured from 20% to 80%)		1.1	1.7		V/nS
t_{HL}[1]	Falling edge slew rate (Measured from 80% to 20%)		1.3	2		V/nS
T_{PJ}[1]	Peak-to-peak Period Jitter @ VDD/2			300		pS
	Synthesis Error (Output Frequency)			0		ppm
t_D[1]	Output Duty Cycle @ VDD/2		45	50	55	%
t_{LOCK}	PLL Lock Time from Power-Up				3	mS

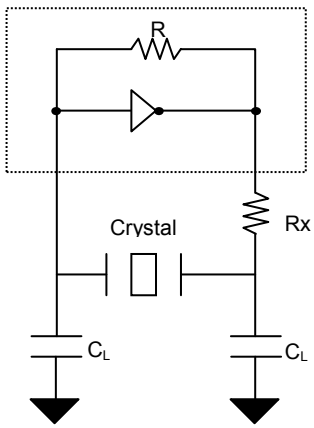
NOTE: 1. CL= 15pF for outputs < 100MHz; CL = 10pF for outputs > 100MHz;

Typical Crystal Specifications

Fundamental AT cut parallel resonant crystal	
Nominal frequency	25MHz
Frequency tolerance	± 50 ppm or better at 25℃
Operating temperature range	-25℃ to +85℃
Storage temperature	-40℃ to +85℃
Load capacitance(C_P)	18pF
Shunt capacitance	7pF maximum
ESR	25 Ω

Note: Note: C_L is Load Capacitance and Rx is used to prevent oscillations at overtone frequency of the Fundamental frequency.

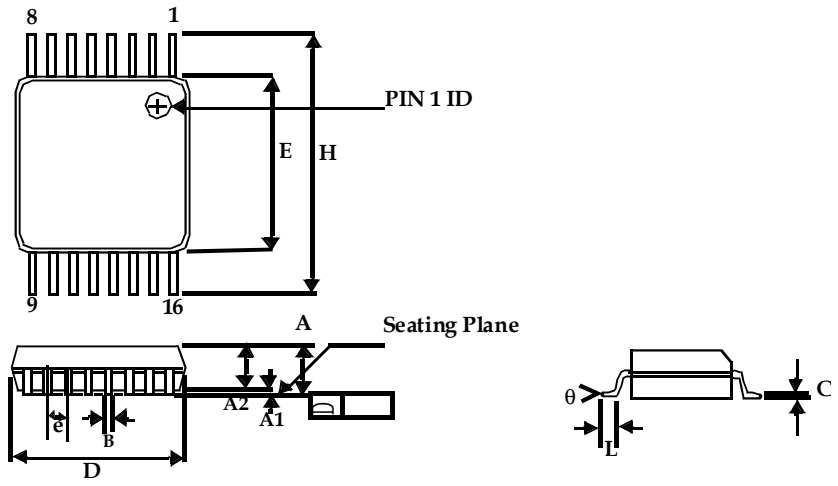
Typical Crystal Interface Circuit



$C_L = 2*(C_P – C_S)$,
Where C_P = Load capacitance of crystal
C_S = Stray capacitance due to $C_{IN,}$ PCB, Trace etc.

Package Information

16-lead Thin Shrunk Small Outline Package (4.40-MM Body)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A		0.043		1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.169	0.177	4.30	4.50
e	0.026 BSC		0.65 BSC	
H	0.252 BSC		6.40 BSC	
L	0.020	0.030	0.50	0.75
θ	0°	8°	0°	8°

Ordering Information

Part Number	Marking	Package	Temperature
PCS1P2860AG-16TR	1P28 60A	16-Pin TSSOP, TAPE & REEL, Green	0℃ to +70℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free.

PUBLICATION ORDERING INFORMATION

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