

STK534U363C-E



Advance Information

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Inverter IPM for 3-phase Motor Drive

Overview

This “Inverter IPM” is highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single SIP module (Single-In line Package). Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP). Internal Boost diodes are provided for high side gate boost drive.

Function

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status output are at low voltage levels directly compatible with microcontrollers.
- Built-in cross conduction prevention.
- Externally accessible embedded thermistor for substrate temperature measurement

Certification

- UL1557 (File number: E339285).

Specifications

Absolute Maximum Ratings at $T_c = 25^\circ\text{C}$

| Parameter | Symbol | Remarks | Ratings | Unit |
|----------------------------|-------------|--|-------------|------------------|
| Supply voltage | V_{CC} | P to U-, V-, W-, surge<500V *1 | 450 | V |
| Collector-emitter voltage | V_{CE} | P to U, V, W or U, V, W, to U-, V-, W- | 600 | V |
| Output current | I_o | P,U-,V-,W-,U,V,W terminal current | ± 10 | A |
| | | P,U-,V-,W-,U,V,W terminal current, $T_c=100^\circ\text{C}$ | ± 5 | A |
| Output peak current | I_{op} | P,U-,V-,W-,U,V,W terminal current, P.W.=1ms | ± 20 | A |
| Pre-driver voltage | $VD1,2,3,4$ | VB1 to U, VB2 to V, VB3 to W, VDD to VSS *2 | 20 | V |
| Input signal voltage | V_{IN} | HIN1, 2, 3, LIN1, 2, 3 | -0.3 to VDD | V |
| FLTEN terminal voltage | V_{FLTEN} | FLTEN terminal | -0.3 to VDD | V |
| Maximum power dissipation | P_d | IGBT per 1 channel | 31.2 | W |
| Junction temperature | T_j | IGBT, FRD, Pre-Driver IC | 150 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -40 to +125 | $^\circ\text{C}$ |
| Operating case temperature | T_c | IPM case | -20 to +100 | $^\circ\text{C}$ |
| Tightening torque | | A screw part *3 | 0.9 | Nm |
| Withstand voltage | V_{is} | 50Hz sine wave AC 1 minute *4 | 2000 | VRMS |

Reference voltage is “VSS” terminal voltage unless otherwise specified.

*1: Surge voltage developed by the switching operation due to the wiring inductance between P and U-(V-, W-) terminal.

*2: Terminal voltage: $VD1=VB1-U$, $VD2=VB2-V$, $VD3=VB3-W$, $VD4=V_{DD}-V_{SS}$.

*3: Flatness of the heat-sink should be 0.15mm and below.

*4: Test conditions : AC2500V, 1 second.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

Electrical Characteristics at $T_c = 25^\circ\text{C}$, VD1, VD2, VD3, VD4 = 15V

| Parameter | Symbol | Conditions | Test circuit | MIN | TYP | MAX | Unit |
|--|--|--|--------------|------|------|------|-------|
| Power output section | | | | | | | |
| Collector-emitter cut-off current | I _{CE} | V _{CE} = 600V | Fig.1 | - | - | 100 | μA |
| Bootstrap diode reverse current | I _{R(BD)} | V _{R(BD)} = 600V | | - | - | 100 | μA |
| Collector to emitter saturation voltage | V _{CE (SAT)} | I _c = 10A, T _j =25°C | Fig.2 | - | 1.6 | 2.4 | V |
| | | I _c = 5A, T _j =100°C | | - | 1.4 | - | |
| Diode forward voltage | V _F | I _F = 10A, T _j =25°C | Fig.3 | - | 1.4 | 2.1 | V |
| | | I _F = 5A, T _j =100°C | | - | 1.2 | - | |
| Junction to case thermal resistance | θ _{j-c(T)} | IGBT | - | - | - | 4 | °C /W |
| | θ _{j-c(D)} | FWD | | - | - | 6 | |
| Control (Pre-driver) section | | | | | | | |
| Pre-driver power dissipation | I _D | VD1,2,3 = 15V | Fig.4 | - | 0.08 | 0.4 | mA |
| | | VD4 = 15V | | - | 1.6 | 4 | |
| High level Input voltage | V _{in H} | HIN1,HIN2,HIN3, | - | 2.5 | - | - | V |
| Low level Input voltage | V _{in L} | LIN1,LIN2,LIN3 to V _{SS} | - | - | - | 0.8 | V |
| Logic 1 input leakage current | I _{IN+} | V _{IN} =+3.3V | - | - | 100 | 143 | μA |
| Logic 0 input leakage current | I _{IN-} | V _{IN} =0V | - | - | - | 2 | μA |
| FLTEN terminal sink current | I _{oSD} | FAULT:ON / V _{FLTEN} =0.1V | - | - | 2 | - | mA |
| FLTEN clearance delay time | FLTCLR | From time fault condition clear | - | 1.0 | 2.0 | 3.0 | ms |
| FLTEN Threshold | V _{EN+} | V _{EN} rising | - | - | - | 2.5 | V |
| | V _{EN-} | V _{EN} falling | - | 0.8 | - | - | V |
| ITRIP threshold voltage | V _{ITRIP} | ITRIP(16) to V _{SS} (29) | - | 0.44 | 0.49 | 0.54 | V |
| ITRIP to shutdown propagation delay | t _{ITRIP} | | - | 340 | 550 | 800 | ns |
| ITRIP blanking time | t _{ITRIPBL} | | - | 250 | 350 | - | ns |
| V _{CC} and V _{BS} supply undervoltage protection reset | V _{CCUV+} V _{BSUV+} | | - | 10.5 | 11.1 | 11.7 | V |
| V _{CC} and V _{BS} supply undervoltage protection set | V _{CCUV-} V _{BSUV-} | | - | 10.3 | 10.9 | 11.5 | V |
| V _{CC} and V _{BS} supply undervoltage hysteresis | V _{CCUVH} V _{BSUVH} | | - | 0.14 | 0.2 | - | V |

Reference voltage is " V_{SS} " terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Electrical Characteristics at $T_c = 25^\circ\text{C}$, $V_{D1}, V_{D2}, V_{D3}, V_{D4} = 15\text{V}$, $V_{CC} = 300\text{V}$, $L = 3.9\text{mH}$

| Parameter | Symbol | Conditions | Test circuit | MIN | TYP | MAX | Unit |
|------------------------------------|--------|--|--------------|-------------|-----|-----|---------------|
| Switching Character | | | | | | | |
| Switching time | t ON | $I_o = 10\text{A}$ | Fig.5 | 0.3 | 0.5 | 1.2 | μs |
| | t OFF | | | - | 0.6 | 1.5 | |
| Turn-on switching loss | Eon | $I_o = 5\text{A}$ | Fig.5 | - | 170 | - | μJ |
| Turn-off switching loss | Eoff | | | - | 80 | - | μJ |
| Total switching loss | Etot | | | - | 250 | - | μJ |
| Turn-on switching loss | Eon | $I_o = 5\text{A}$, $T_c = 100^\circ\text{C}$ | Fig.5 | - | 200 | - | μJ |
| Turn-off switching loss | Eoff | | | - | 100 | - | μJ |
| Total switching loss | Etot | | | - | 300 | - | μJ |
| Diode reverse recovery energy | Erec | $I_F = 5\text{A}$, $P = 400\text{V}$, $L = 0.5\text{mH}$, | - | - | 17 | - | μJ |
| Diode reverse recovery time | trr | $T_c = 100^\circ\text{C}$ | - | - | 62 | - | ns |
| Reverse bias safe operating area | RBSOA | $I_o = 20\text{A}$, $V_{CE} = 450\text{V}$ | - | Full square | | | - |
| Short circuit safe operating area | SCSOA | $V_{CE} = 400\text{V}$, $T_c = 100^\circ\text{C}$ | - | 4 | - | - | μs |
| Allowable offset voltage slew rate | dv/dt | Between U,V,W to U-,V-,W- | - | -50 | - | 50 | V/ns |

Reference voltage is “VSS” terminal voltage unless otherwise specified.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Notes

1. When the internal protection circuit operates, a Fault signal is turned ON (When the Fault terminal is low level, Fault signal is ON state : output form is open DRAIN) but the Fault signal does not latch. After protection operation ends, it returns automatically within about typ. 2ms and resumes operation beginning condition. So, after Fault signal detection, set all input signals to OFF (Low) at once. However, the operation of pre-drive power supply low voltage protection (UVLO: with hysteresis about 0.2V) is as follows.

Upper side:

The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn 'low'.

Lower side:

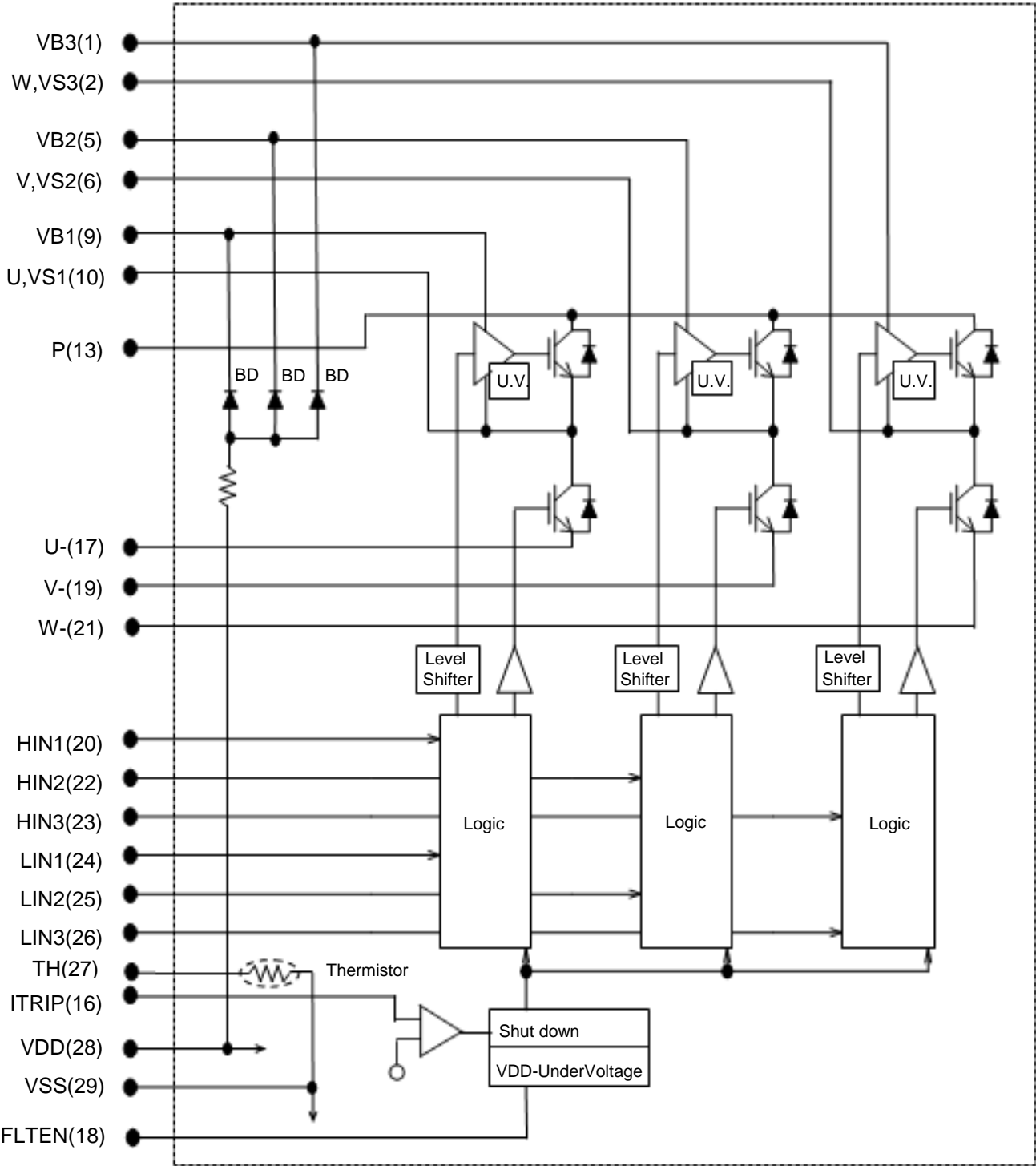
The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.

2. When assembling the IPM on the heat sink with M3 type screw, tightening torque range is 0.6 Nm to 0.8 Nm.
3. When use the over-current protection with external resistor, please set resistance value so that current protection value becomes equal to or less than the double (2 times) of the rating output electric current (I_o).

Module Pin-Out Description

| Pin | Name | Description |
|-----|--------|---|
| 1 | VB3 | High Side Floating Supply Voltage 3 |
| 2 | W, VS3 | Output 3 - High Side Floating Supply Offset Voltage |
| 3 | - | Without pin |
| 4 | - | Without pin |
| 5 | VB2 | High Side Floating Supply voltage 2 |
| 6 | V, VS2 | Output 2 - High Side Floating Supply Offset Voltage |
| 7 | - | Without pin |
| 8 | - | Without pin |
| 9 | VB1 | High Side Floating Supply voltage 1 |
| 10 | U, VS1 | Output 1 - High Side Floating Supply Offset Voltage |
| 11 | - | Without pin |
| 12 | - | Without pin |
| 13 | P | Positive Bus Input Voltage |
| 14 | - | Without pin |
| 15 | - | Without pin |
| 16 | ITRIP | Current protection pin |
| 17 | U- | Low Side Emitter Connection - Phase U |
| 18 | FLTEN | Enable input / Fault output |
| 19 | V- | Low Side Emitter Connection - Phase V |
| 20 | HIN1 | Logic Input High Side Gate Driver - Phase U |
| 21 | W- | Low Side Emitter Connection - Phase W |
| 22 | HIN2 | Logic Input High Side Gate Driver - Phase V |
| 23 | HIN3 | Logic Input High Side Gate Driver - Phase W |
| 24 | LIN1 | Logic Input Low Side Gate Driver - Phase U |
| 25 | LIN2 | Logic Input Low Side Gate Driver - Phase V |
| 26 | LIN3 | Logic Input Low Side Gate Driver - Phase W |
| 27 | TH | Thermistor output |
| 28 | VDD | +15V Main Supply |
| 29 | VSS | Negative Main Supply |

Equivalent Block Diagram



■ Switching time (The circuit is a representative example of the lower side U phase.)

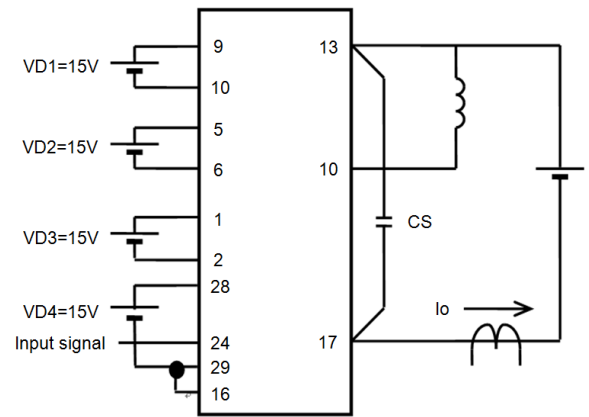
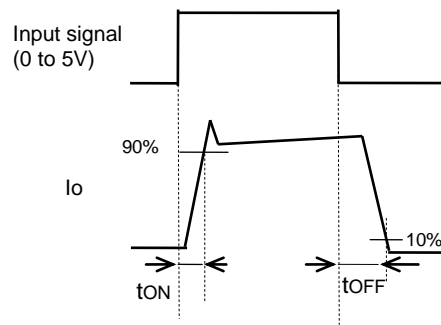


Fig.5

Input / Output Timing Chart

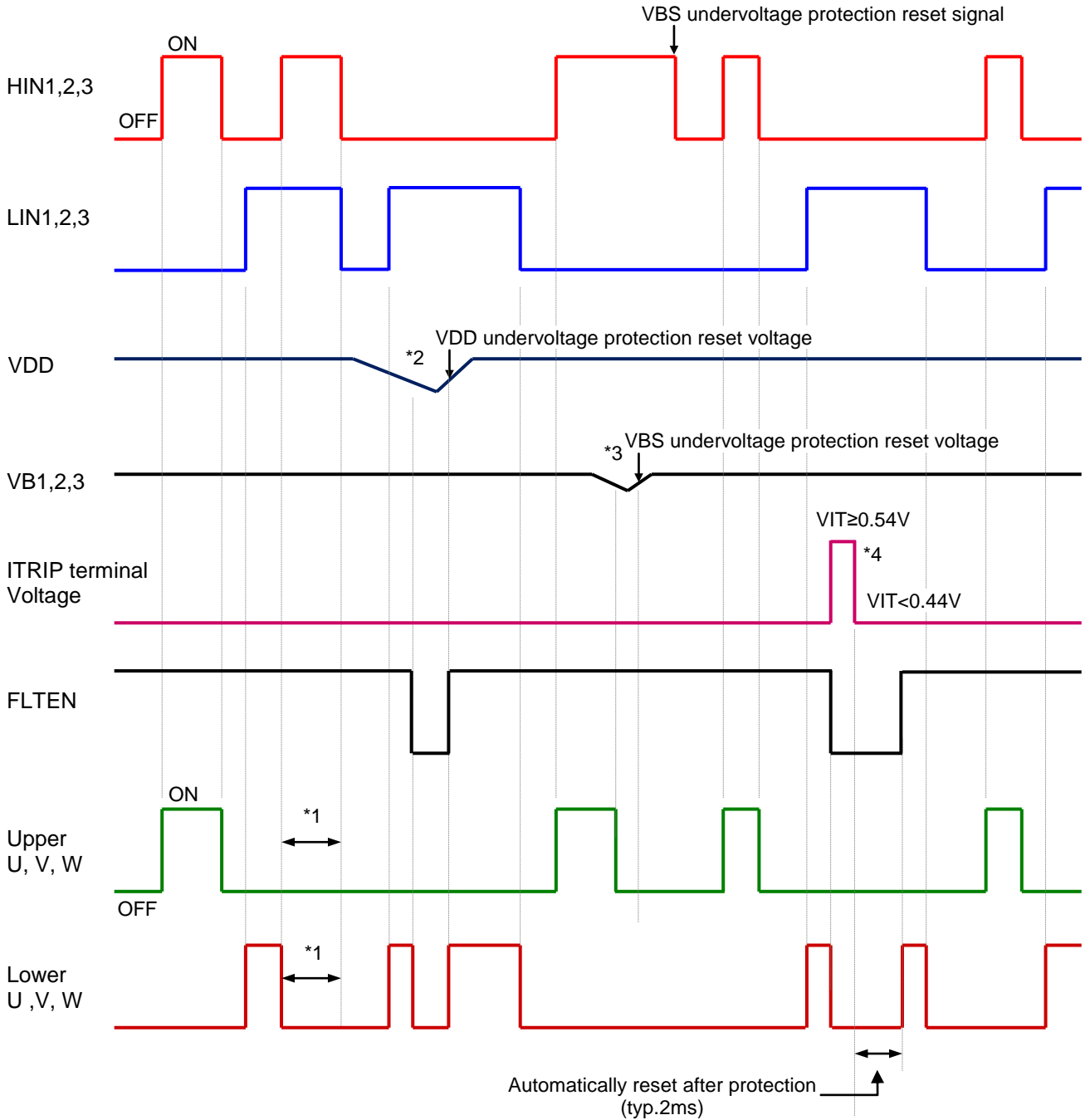


Fig. 6

Notes

- *1 shows the prevention of shoot-thru via control logic, however, more dead time must be added to account for switching delay externally.
- *2 when V_{DD} decreases all gate output signals will go low and cut off all 6 IGBT outputs. When V_{DD} rises the operation will resume immediately.
- *3 when the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.
- *4 when V_{ITRIP} exceeds threshold all IGBT's are turned off and normal operation resumes 2ms (typ) after over current condition is removed.

Logic level table

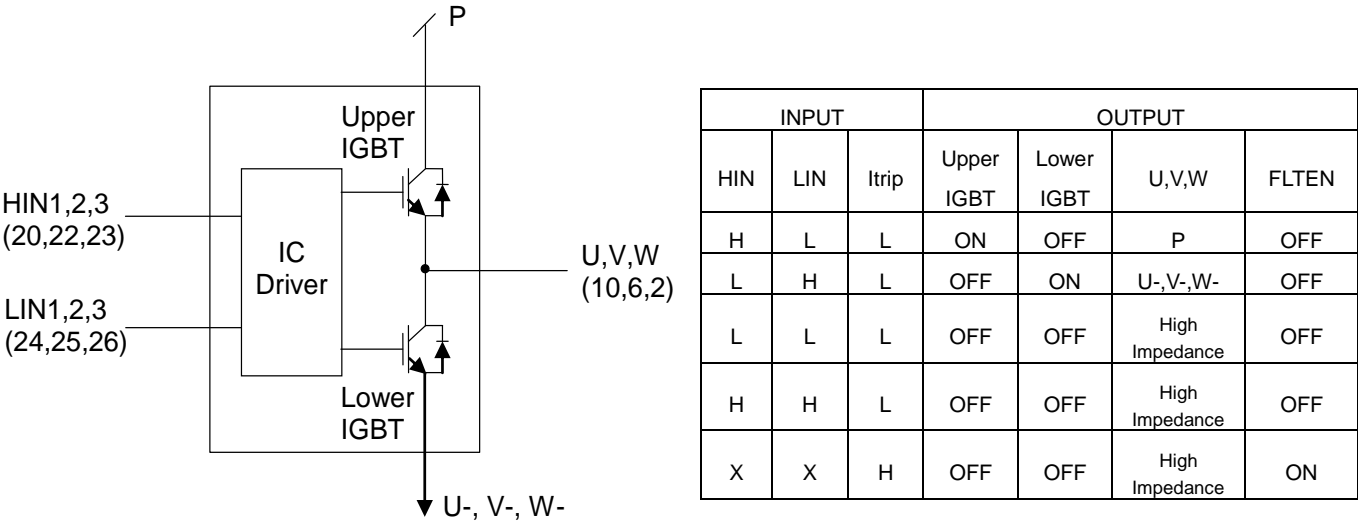


Fig. 7

Sample Application Circuit

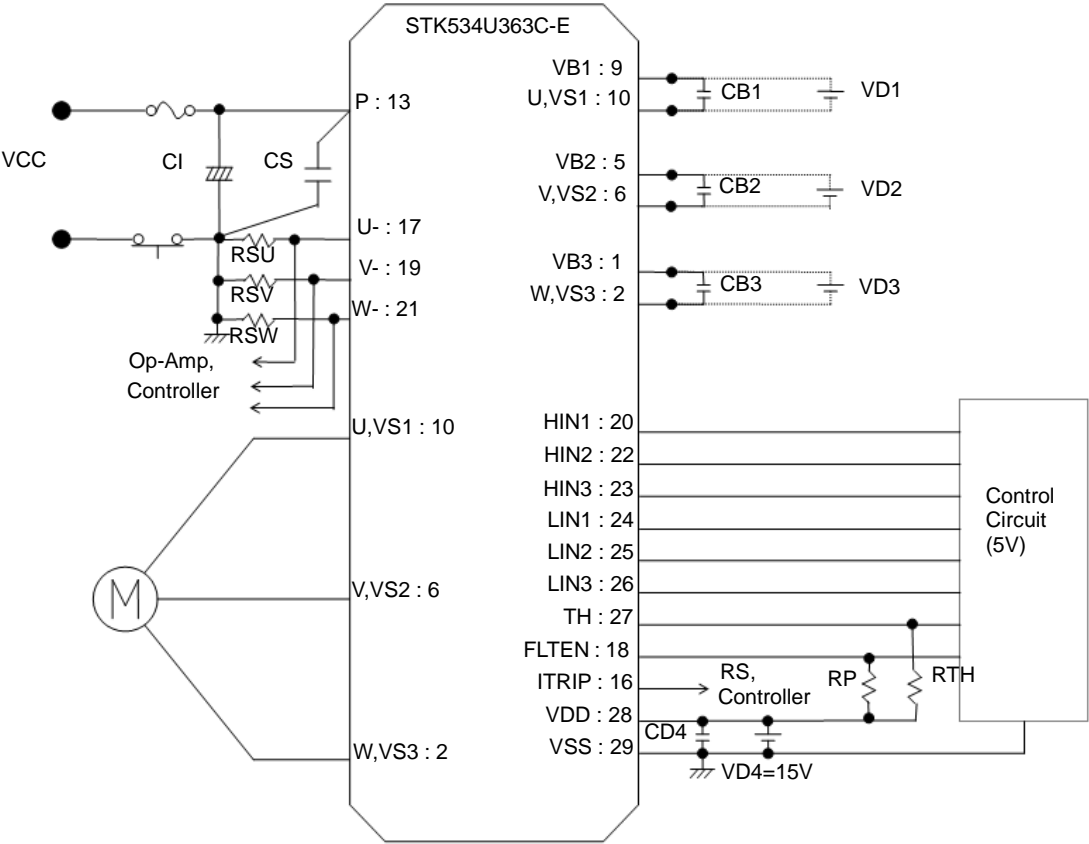


Fig.8

Recommended Operating Condition

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------|---------------|--------------------------------|------|------|------|---------|
| Supply voltage | V_{CC} | P to U-(V-,W-) | 0 | 280 | 450 | V |
| Pre-driver | VD1,2,3 | VB1 to U,VB2 to V,VB3 to W | 12.5 | 15 | 17.5 | V |
| supply voltage | VD4 | V_{DD} to V_{SS} *1 | 13.5 | 15 | 16.5 | |
| ON-state input voltage | $V_{IN(ON)}$ | HIN1,HIN2,HIN3, | 3.0 | - | 5.0 | V |
| OFF-state input voltage | $V_{IN(OFF)}$ | LIN1,LIN2,LIN3 | 0 | - | 0.3 | |
| PWM frequency | fPWM | | 1 | - | 20 | kHz |
| Dead time | DT | Turn-off to turn-on (external) | 1 | - | - | μs |
| Allowable input pulse width | PWIN | ON and OFF | 1 | - | - | μs |
| Tightening torque | | 'M3' type screw | 0.6 | - | 0.8 | Nm |

*1 Pre-drive power supply ($VD4=15\pm1.5V$) must have the capacity of $I_o=20mA$ (DC), 0.5A (Peak).

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Usage Precaution

1. This IPM includes bootstrap diode and resistors. Therefore, by adding a capacitor “CB”, a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47 μ F, however this value needs to be verified prior to production. If selecting the capacitance more than 47 μ F ($\pm 20\%$), connect a resistor (about 20 Ω) in series between each 3-phase upper side power supply terminals (VB1,2,3) and each bootstrap capacitor.
When not using the bootstrap circuit, each upper side pre-drive power supply requires an external independent power supply.
2. It is essential that wiring length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of “CS” is in the range of 0.1 to 10 μ F.
3. “FLTEN” (Pin 18) is open Drain (Active Low). This terminal serves as the shut down function of the built-in pre-driver. (When the terminal voltage is above 3V, normalcy works, and it is shut down when it is equal to or less than 0.8V.) Please make pulling up outside so that “FLTEN” terminal voltages become more than 3V. When the pull up voltage (VP) is at 5V, pull up resistor (RP) recommended more than 6.8k Ω , and in case of VP=15V, RP recommended more than 20k Ω .
4. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between VSS terminal and TH terminal, therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used. The temperature monitor example application is as follows, please refer the Fig.9, and Fig.10 below.
5. Pull down resistor of 33k Ω is provided internally at the signal input terminals. An external resistor of 2.2k to 3.3k Ω should be added to reduce the influence of external wiring noise.
6. The over-current protection feature is not intended to protect in exceptional fault condition. An external fuse is recommended for safety.
7. “ITRIP” (Pin 16) is the input terminal of the built-in comparator. When VITRIP exceeds threshold all IGBTs are turned off and normal operation resumes 2ms (typ) after over current condition is removed. Therefore, please do the protection movement detection of all input signals in OFF (LOW) promptly afterward.
8. When input pulse width is less than 1.0 μ s, an output may not react to the pulse. (Both ON signal and OFF signal)

The characteristic of thermistor

| Parameter | Symbol | Condition | Min | Typ. | Max | Unit |
|---------------------|-----------|---------------------------|------|------|------|--------------------|
| Resistance | R_{25} | $T = 25^{\circ}\text{C}$ | 97 | 100 | 103 | k Ω |
| Resistance | R_{125} | $T = 125^{\circ}\text{C}$ | 2.27 | 2.52 | 2.80 | k Ω |
| B-Constant(25-50°C) | B | | 4165 | 4250 | 4335 | K |
| Temperature Range | | | -40 | | +125 | $^{\circ}\text{C}$ |

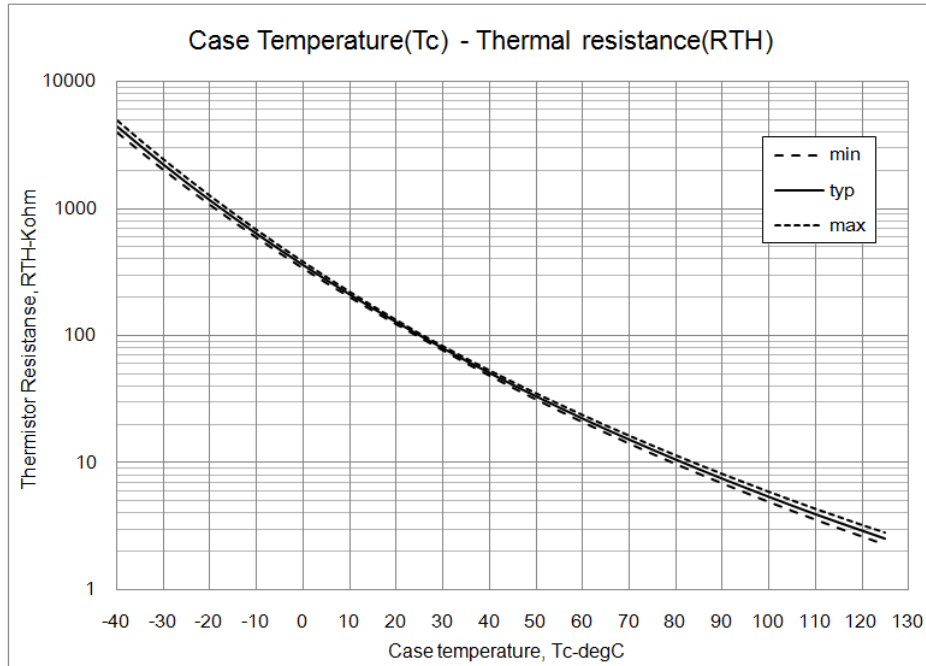


Fig.9

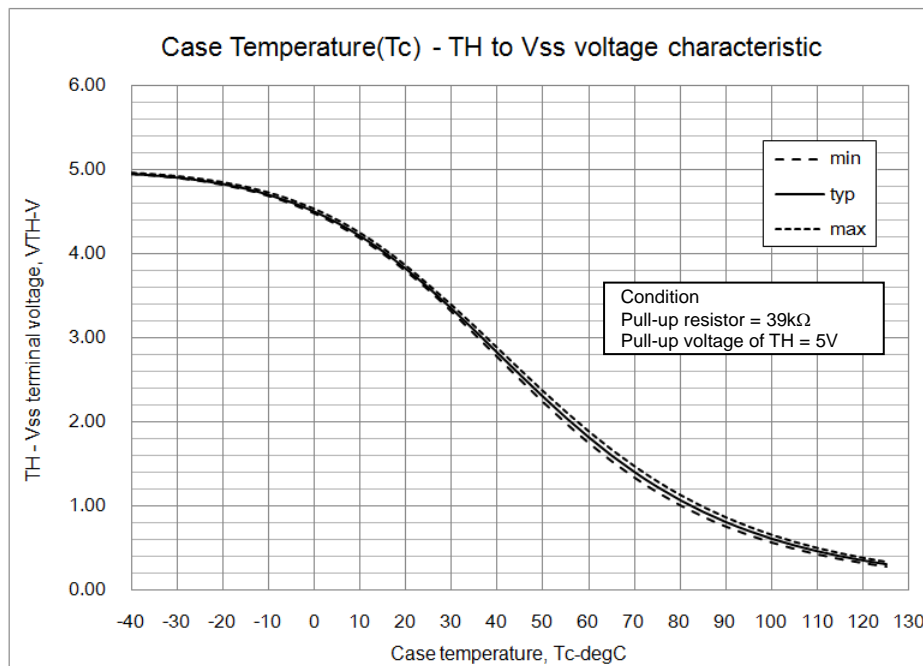


Fig.10

The characteristic of PWM switching frequency

Maximum sinusoidal phase current as function of switching frequency at $T_c=100^{\circ}\text{C}$, $V_{CC}=300\text{V}$

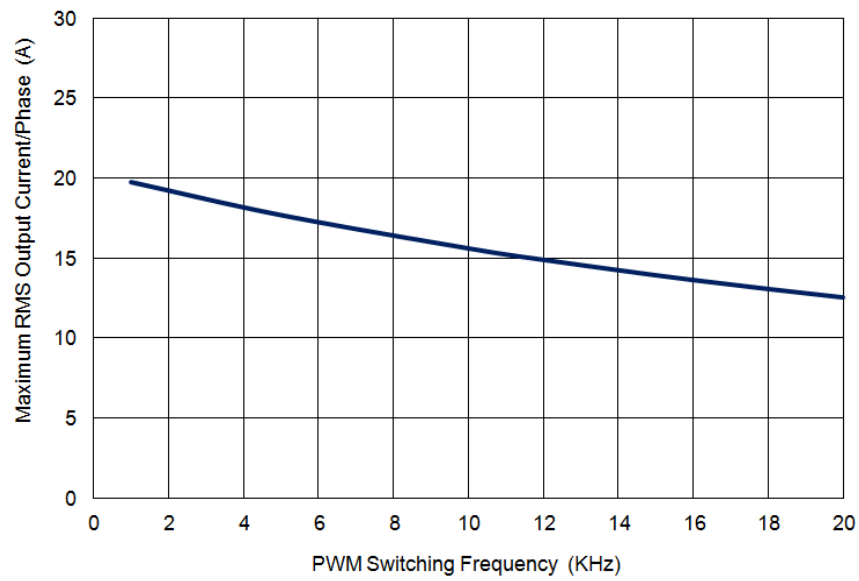


Fig.11

CB capacitor value calculation for bootstrap circuit

Calculate condition

| Item | Symbol | Value | Unit |
|--|--------|-------|------|
| Upper side power supply. | VBS | 15 | V |
| Total gate charge of output power IGBT at 15V. | Qg | 89 | nC |
| Upper side power supply low voltage protection. | UVLO | 12 | V |
| Upper side power dissipation. | IDMAX | 400 | μA |
| ON time required for CB voltage to fall from 15V to UVLO | TONMAX | - | s |

Capacitance calculation formula

Tonmax is upper arm maximum on time equal the time when the CB voltage falls from 15V to the upper limit of Low voltage protection level.

"ton-maximum" of upper side is the time that CB decreases 15V to the maximum low voltage protection of the upper side (12V).

Thus, CB is calculated by the following formula.

$$\begin{aligned} VBS * CB - Qg - IDMAX * TONMAX &= UVLO * CB \\ CB &= (Qg + IDMAX * TONMAX) / (VBS - UVLO) \end{aligned}$$

The relationship between tonmax and CB becomes as follows. CB is recommended to be approximately 3 times the value calculated above. The recommended value of Cb is in the range of 1 to 47μF, however, the value needs to be verified prior to production.

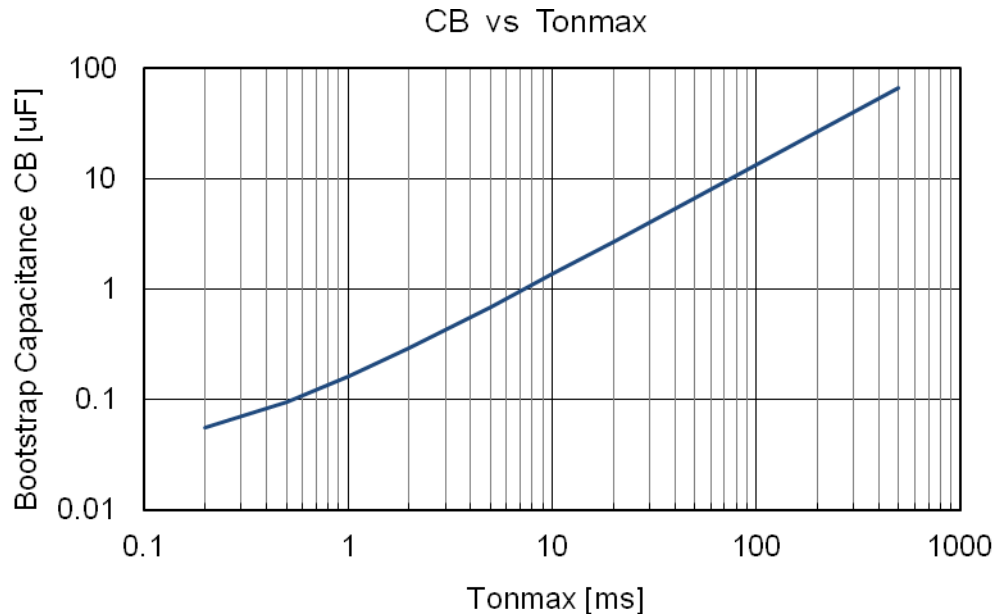


Fig.12 TONMAX vs CB characteristic

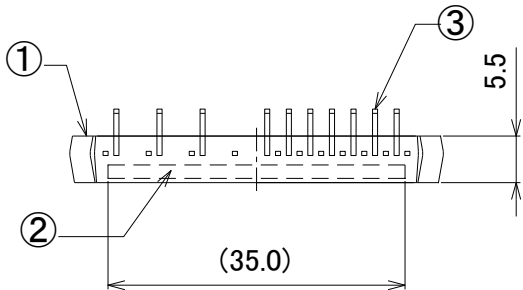
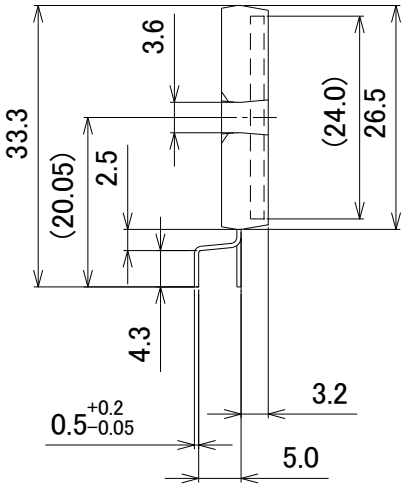
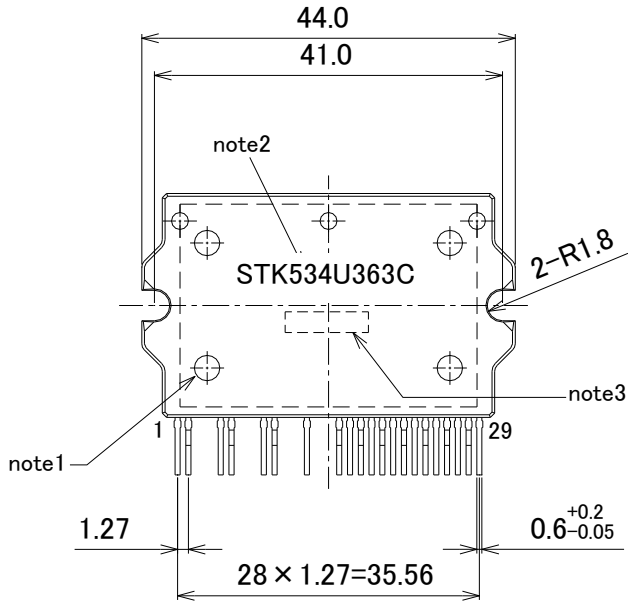
ORDERING INFORMATION

| Device | Package | Shipping (Qty / Packing) |
|---------------|----------------------------|--------------------------|
| STK534U363C-E | SIP29 44x26.5 (Pb-Free) | 11 / Tube |

Package Outline Diagram

Product Name STK534U363C-E

missing pin : 3,4,7,8,11,12,14,15



note1: Mark of mirror surface for No.1 pin identification.
 note2: The form of a character in this drawing differs from that of H-IC.
 note3: This indicates the lot code.
 The form of a character in this drawing differs from that of H-IC.

| | | |
|---------------------------|------|--|
| Unit | mm | |
| Tolerance | ±0.5 | |
| Don't scale this drawing. | | |
| Control No. | | |

| No. | Part Name | Material | Treatment |
|-----|------------|----------------|-----------|
| ① | Case | EPOXY | |
| ② | Substrate | IMST Substrate | |
| ③ | Lead Frame | Cu | Sn |

| | | | |
|------|----------|-----------|----------|
| | | | |
| | | | |
| | | | |
| Date | Revision | In charge | Approval |

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