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FAIRCHILD SEMICONDUCTOR™

October 2000
Revised September 2001

# 74LCXH245
# Low Voltage Bidirectional Transceiver with Bushold

## General Description

The LCXH245 contains eight non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is designed for low voltage (2.5V and 3.3V) $V_{CC}$ applications. The T/$\overline{R}$ input determines the direction of data flow through the device. The $\overline{OE}$ input disables both the A and B ports by placing them in a high impedance state.

The LCXH245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation. The LCXH16244 data inputs include active bushold circuitry, eliminating the need for external pull-up resistors to hold unused or floating data inputs at a valid logic level.

## Features

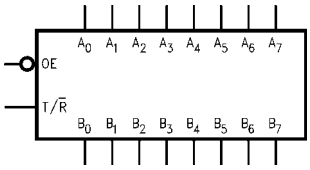
- 5V tolerant control inputs
- 2.3V–3.6V $V_{CC}$ specifications provided
- 7.0 ns $t_{PD}$ max ($V_{CC}$ = 3.3V), 10 µA $I_{CC}$ max
- Power down high impedance outputs
- ±24 mA output drive ($V_{CC}$ = 3.0V)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- Bushold on inputs eliminates the need for external pull-up/pull-down resistors
- ESD performance:
  Human body model > 2000V
  Machine model > 200V

## Ordering Code:

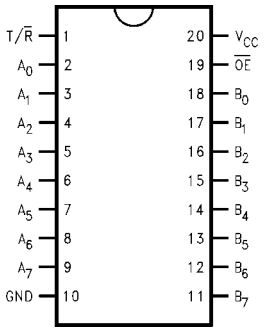
| Order Number | Package Number | Package Description |
|---|---|---|
| 74LCXH245WM | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74LCXH245SJ | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74LCXH245MSA | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide |
| 74LCXH245MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Logic Symbol




## Connection Diagram




## Pin Descriptions

| Pin Names | Description |
|---|---|
| $\overline{OE}$ | Output Enable Input |
| T/$\overline{R}$ | Transmit/Receive Input |
| $A_0$–$A_7$ | Side A Inputs or 3-STATE Outputs (Bushold) |
| $B_0$–$B_7$ | Side B Inputs or 3-STATE Outputs (Bushold) |

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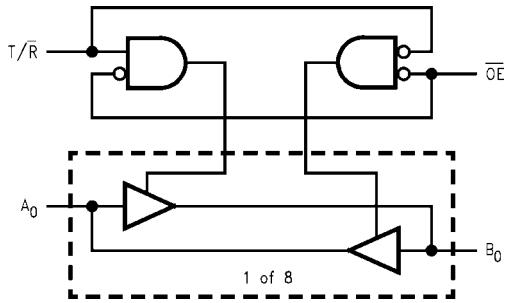
## Truth Table

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}$ | T/$\overline{R}$ | |
| L | L | Bus $B_0 – B_7$ Data to Bus $A_0 – A_7$ |
| L | H | Bus $A_0 – A_7$ Data to Bus $B_0 – B_7$ |
| H | X | HIGH Z State on $A_0 – A_7$, $B_0 – B_7$ (Note 1) |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

**Note 1:** Unused bus terminals during HIGH Z State must be held HIGH or LOW.

## Logic Diagram



## Absolute Maximum Ratings(Note 2)

| Symbol | Parameter | Value | Conditions | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 to +7.0 | | V |
| $V_I$ | T/$\overline{R}$, OE | 0.5 to +7.0 | | V |
| | I/O Ports | −0.5 to $V_{CC}$ + 0.5 | | |
| $V_O$ | DC Output Voltage | −0.5 to +7.0 | Output in 3-STATE | V |
| | | −0.5 to $V_{CC}$ + 0.5 | Output in HIGH or LOW State (Note 3) | |
| $I_{IK}$ | DC Input Diode Current | −50 | $V_I$ < GND | mA |
| $I_{OK}$ | DC Output Diode Current | −50 | $V_O$ < GND | mA |
| | | +50 | $V_O$ > $V_{CC}$ | |
| $I_O$ | DC Output Source/Sink Current | ±50 | | mA |
| $I_{CC}$ | DC Supply Current per Supply Pin | ±100 | | mA |
| $I_{GND}$ | DC Ground Current per Ground Pin | ±100 | | mA |
| $T_{STG}$ | Storage Temperature | −65 to +150 | | °C |

## Recommended Operating Conditions (Note 4)

| Symbol | Parameter | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Operating | 2.0 | 3.6 | V |
| | | Data Retention | 1.5 | 3.6 | |
| $V_I$ | Input Voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output Voltage | HIGH or LOW State | 0 | $V_{CC}$ | V |
| | | 3-STATE | 0 | 5.5 | |
| $I_{OH}/I_{OL}$ | Output Current | $V_{CC}$ = 3.0V − 3.6V | | ±24 | mA |
| | | $V_{CC}$ = 2.7V - 3.0V | | ±12 | |
| | | $V_{CC}$ = 2.3V - 2.7V | | ±8 | |
| $T_A$ | Free-Air Operating Temperature | | −40 | 85 | °C |
| $\Delta t/\Delta V$ | Input Edge Rate, $V_{IN}$ = 0.8V − 2.0V, $V_{CC}$ = 3.0V | | 0 | 10 | ns/V |

**Note 2:** The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 3:** $I_O$ Absolute Maximum Rating must be observed.

**Note 4:** Floating or unused control inputs must be HIGH or LOW.

## DC Electrical Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ | $T_A$ = −40°C to +85°C | | Units |
|---|---|---|---|---|---|---|
| | | | (V) | Min | Max | |
| $V_{IH}$ | HIGH Level Input Voltage | | 2.3 − 2.7 | 1.7 | | V |
| | | | 2.7 − 3.6 | 2.0 | | |
| $V_{IL}$ | LOW Level Input Voltage | | 2.3 − 2.7 | | 0.7 | V |
| | | | 2.7 - 3.6 | | 0.8 | |
| $V_{OH}$ | HIGH Level Output Voltage | $I_{OH}$ = −100 µA | 2.3 - 3.6 | $V_{CC}$ − 0.2 | | V |
| | | $I_{OH}$ = −8 mA | 2.3 | 1.8 | | |
| | | $I_{OH}$ = −12 mA | 2.7 | 2.2 | | |
| | | $I_{OH}$ = −18 mA | 3.0 | 2.4 | | |
| | | $I_{OH}$ = −24 mA | 3.0 | 2.2 | | |
| $V_{OL}$ | LOW Level Output Voltage | $I_{OL}$ = 100 µA | 2.3 − 3.6 | | 0.2 | V |
| | | $I_{OL}$ = 8mA | 2.3 | | 0.6 | |
| | | $I_{OL}$ = 12 mA | 2.7 | | 0.4 | |
| | | $I_{OL}$ = 16 mA | 3.0 | | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3.0 | | 0.55 | |
| $I_I$ | Input Leakage Current | $V_I$ = $V_{CC}$ or GND | 2.3 − 3.6 | | ±5.0 | µA |

## DC Electrical Characteristics (Continued)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = -40°C$ to $+85°C$ | | Units |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $I_{I(HOLD)}$ | Bushold Input Minimum Drive Hold Current | $V_{IN} = 0.7V$ | 2.3 | 45 | | µA |
| | | $V_{IN} = 1.7V$ | | −45 | | |
| | | $V_{IN} = 0.8V$ | 3.0 | 75 | | |
| | | $V_{IN} = 2.0V$ | | −75 | | |
| $I_{I(OD)}$ | Bushold Input Over-Drive Current to Change State | (Note 6) | 2.7 | 300 | | µA |
| | | (Note 7) | | −300 | | |
| | | (Note 6) | 3.6 | 450 | | |
| | | (Note 7) | | −450 | | |
| $I_{OZ}$ | 3-STATE I/O Leakage | $V_O = V_{CC}$ or GND | 2.3 – 3.6 | | ±5.0 | µA |
| $I_{CC}$ | Quiescent Supply Current | $V_I = V_{CC}$ or GND | 2.3 – 3.6 | | 10 | µA |
| | | $3.6V \le V_I, V_O \le 5.5V$ (Note 5) | 2.3 – 3.6 | | ±10 | |
| $\Delta I_{CC}$ | Increase in $I_{CC}$ per Input | $V_{IH} = V_{CC} - 0.6V$ | 2.3 - 3.6 | | 500 | µA |

**Note 5:** Outputs disabled or 3-STATE only.

**Note 6:** An external driver must source at least the specified current to switch from LOW-to-HIGH.

**Note 7:** An external driver must sink at least the specified current to switch from HIGH-to-LOW.

## AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$ | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | $V_{CC} = 3.3V \pm 0.3V$ | | $V_{CC} = 2.7V$ | | $V_{CC} = 2.5V \pm 0.2V$ | | |
| | | $C_L = 50$ pF | | $C_L = 50$ pF | | $C_L = 30$ pF | | |
| | | Min | Max | Min | Max | Min | Max | |
| $t_{PHL}$ | Propagation Delay | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | ns |
| $t_{PLH}$ | $A_n$ to $B_n$ or $B_n$ to $A_n$ | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 8.4 | |
| $t_{PZL}$ | Output Enable Time | 1.5 | 8.5 | 1.5 | 9.5 | 1.5 | 10.5 | ns |
| $t_{PZH}$ | | 1.5 | 8.5 | 1.5 | 9.5 | 1.5 | 10.5 | |
| $t_{PLZ}$ | Output Disable Time | 1.5 | 7.5 | 1.5 | 8.5 | 1.5 | 9.0 | ns |
| $t_{PHZ}$ | | 1.5 | 7.5 | 1.5 | 8.5 | 1.5 | 9.0 | |
| $t_{OSHL}$ | Output to Output Skew | | 1.0 | | | | | ns |
| $t_{OSLH}$ | (Note 8) | | 1.0 | | | | | |

**Note 8:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ($t_{OSHL}$) or LOW-to-HIGH ($t_{OSLH}$).

## Dynamic Switching Characteristics

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = 25°C$ Typical | Units |
|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Dynamic Peak $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | 0.8 | V |
| | | $C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$ | 2.5 | 0.6 | |
| $V_{OLV}$ | Quiet Output Dynamic Valley $V_{OL}$ | $C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$ | 3.3 | −0.8 | V |
| | | $C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$ | 2.5 | −0.6 | |

## Capacitance

| Symbol | Parameter | Conditions | Typical | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{CC}$ = Open, $V_I = 0V$ or $V_{CC}$ | 7 | pF |
| $C_{I/O}$ | Input/Output Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$ | 8 | pF |
| $C_{PD}$ | Power Dissipation Capacitance | $V_{CC} = 3.3V$, $V_I = 0V$ or $V_{CC}$, f = 10 MHz | 25 | pF |

## AC LOADING and WAVEFORMS Generic for LCX Family

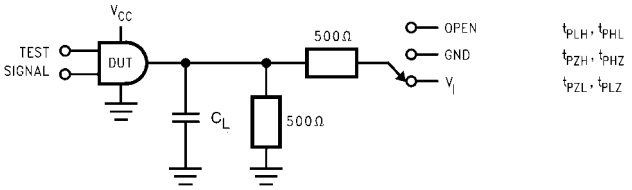
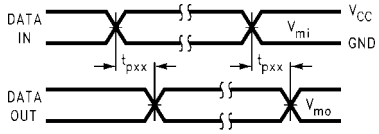
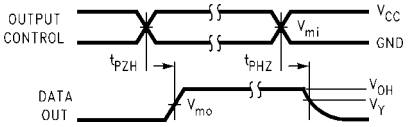



**FIGURE 1. AC Test Circuit ($C_L$ includes probe and jig capacitance)**

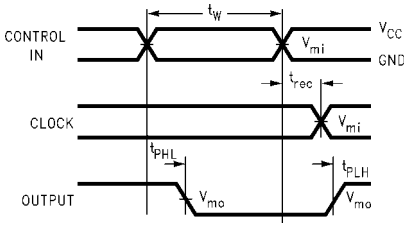
| Test | Switch |
|---|---|
| $t_{PLH}$, $t_{PHL}$ | Open |
| $t_{PZL}$, $t_{PLZ}$ | 6V at $V_{CC}$ = 3.3 ± 0.3V; and 2.7V<br>$V_{CC}$ x 2 at $V_{CC}$ = 2.5 ± 0.2V |
| $t_{PZH}$, $t_{PHZ}$ | GND |



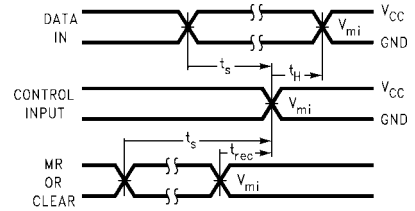

**Waveform for Inverting and Non-Inverting Functions**



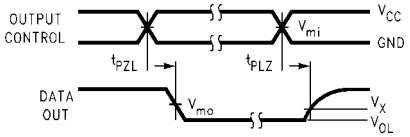

**3-STATE Output High Enable and Disable Times for Logic**



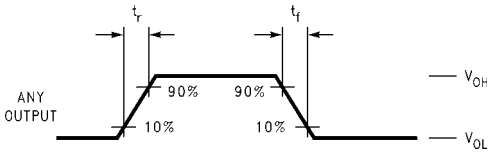

**Propagation Delay. Pulse Width and $t_{rec}$ Waveforms**




**Setup Time, Hold Time and Recovery Time for Logic**




**3-STATE Output Low Enable and Disable Times for Logic**

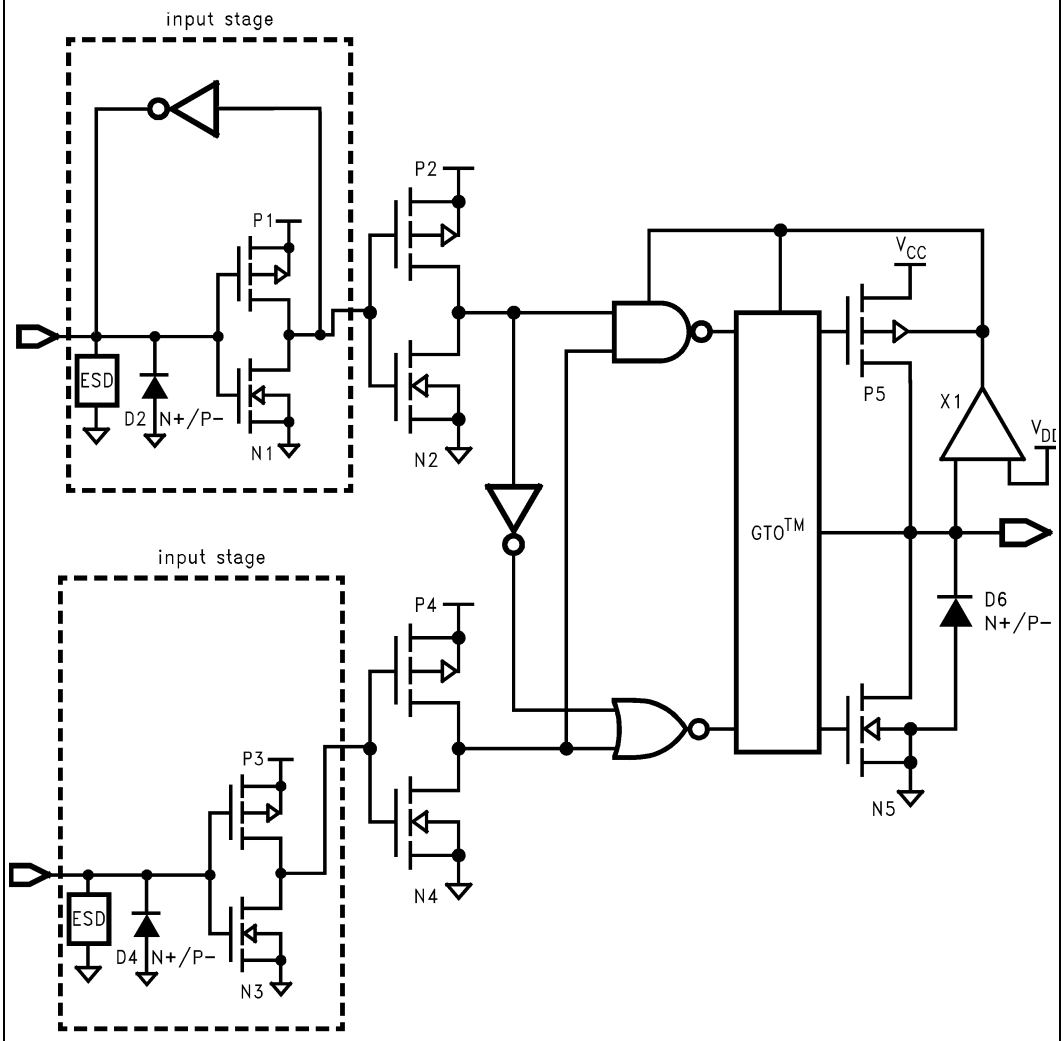



**$t_{rise}$ and $t_{fall}$**

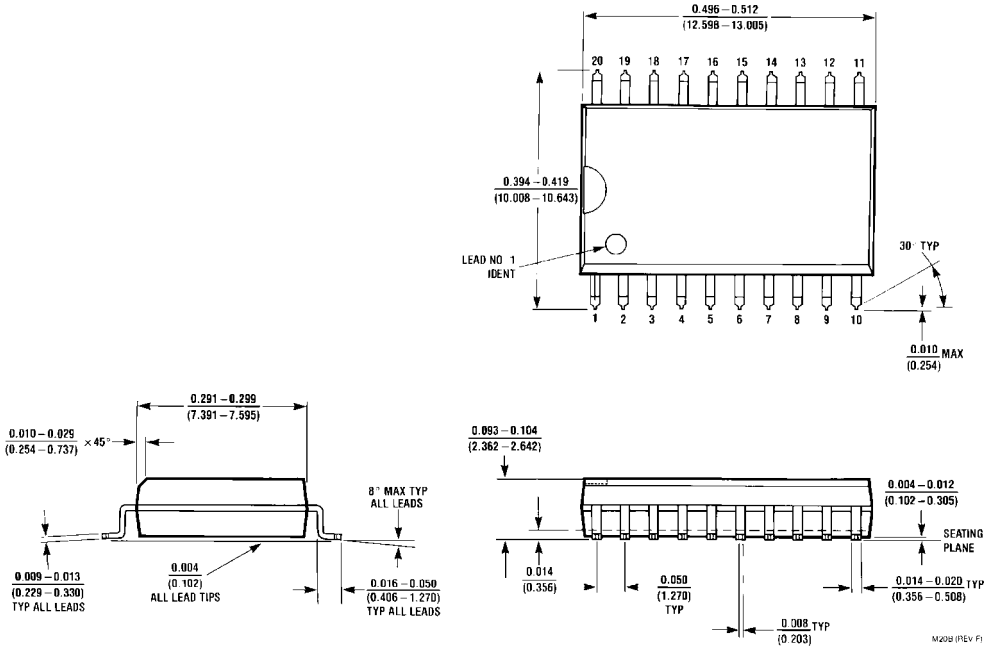
**FIGURE 2. Waveforms**
**(Input Characteristics; f =1MHz, $t_r$ = $t_f$ = 3ns)**

| Symbol | $V_{CC}$ | | |
|---|---|---|---|
| | 3.3V ± 0.3V | 2.7V | 2.5V ± 0.2V |
| $V_{mi}$ | 1.5V | 1.5V | $V_{CC}$/2 |
| $V_{mo}$ | 1.5V | 1.5V | $V_{CC}$/2 |
| $V_x$ | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.3V | $V_{OL}$ + 0.15V |
| $V_y$ | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.3V | $V_{OH}$ − 0.15V |

## Schematic Diagram Generic for LCXH Family (with Bushold)

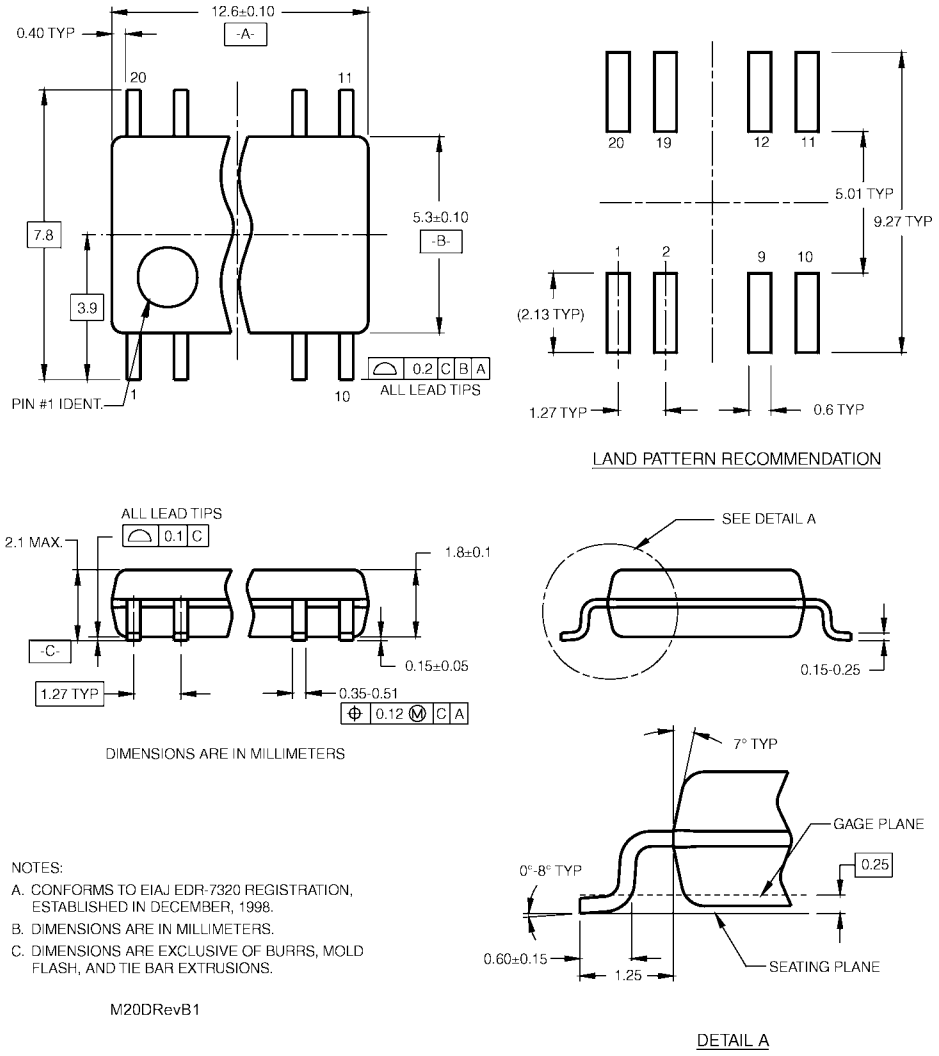


## Physical Dimensions inches (millimeters) unless otherwise noted




**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**
**Package Number M20B**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

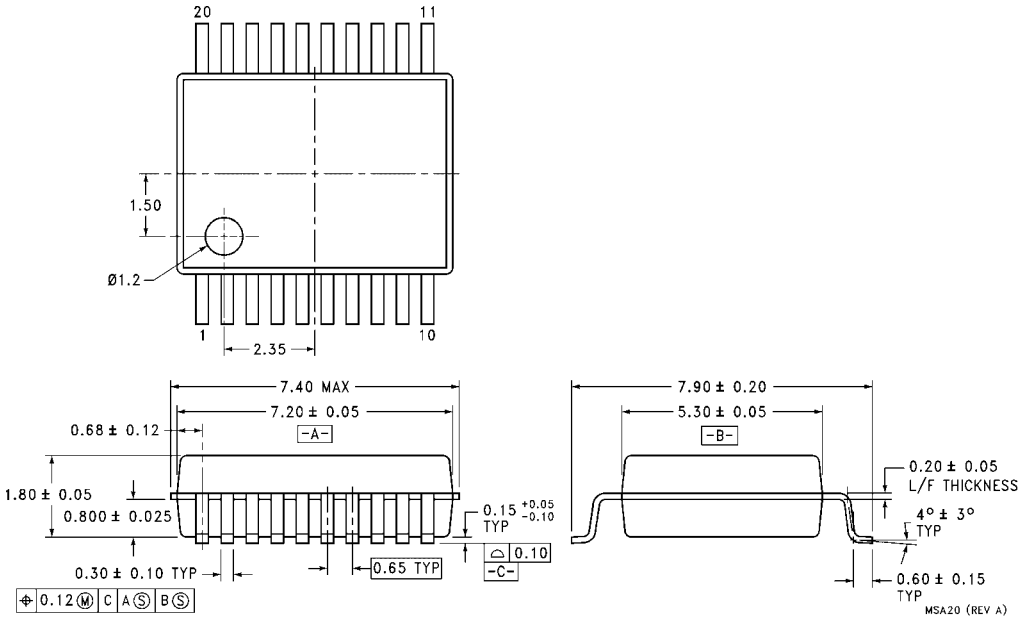
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

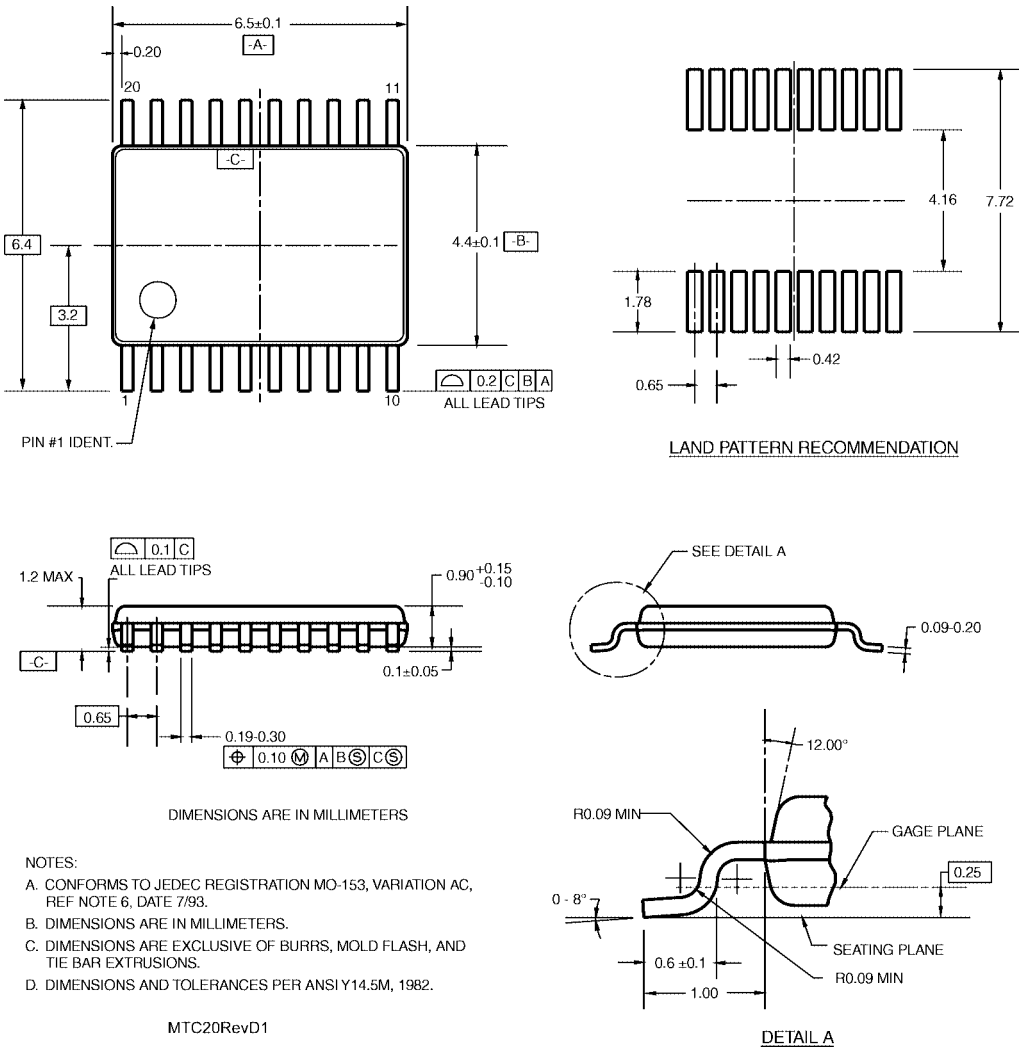
**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M20D**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number MSA20**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




DIMENSIONS ARE IN MILLIMETERS

NOTES:

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C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC20**



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