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#### April 2016

# 74LVX3245 8-Bit, Dual-Supply Translating Transceiver with 3-State Outputs

#### **Features**

- Bidirectional Interface Between 3 V and 5 V Buses
- Inputs Compatible with TTL Level
- 3 V Data Flow at A-Port and 5 V Data Flow at B-Port
- Outputs Source / Sink: 24 mA
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Implements Proprietary EMI Reduction Circuitry
- Functionally Compatible with the 74 Series 245

#### Description

The 74LVX3245 is a dual-supply, 8-bit translating transceiver designed to interface between a 3 V bus and a 5 V bus in a mixed 5 V supply environment. The Transmit/ Receive (T/R) input determines the direction of data flow. Transmit (active-HIGH) enables data from A-ports to B-ports; receive (active-LOW) enables data from B-ports to A-ports. The output enable input, when HIGH, disables both A- and B-ports by placing them in a high-impedance condition. The A-port interfaces with the 3 V bus; the B-port interfaces with the 5 V bus.

The 74LVX3245 is suitable for mixed-voltage applications, such as notebook computers using 3.3 V CPU and 5V peripheral components.

#### **Related Resources**

AN-5001 — Using Fairchild's LVX Low-Voltage Dual-Supply CMOS Translating Transceivers

### **Ordering Information**

Part Number	Operating Temperature Range	Package	Packing Method
74LVX3245QSC		24-Lead Quarter-Size Outline Package	Tubes
74LVX3245QSCX		(QSOP), JEDEC MO-137, 0.150" Wide	Tape and Reel
74LVX3245MTC	-40 to +85°C	24-Lead Thin-Shrink Small-Outline	Tubes
74LVX3245MTCX		Package (TSSOP), JEDEC MO-153, 4.4 mm Wide	Tape and Reel



# **Pin Definitions**

Pin #	Name	Description
1	V <sub>CCA</sub>	Supply Voltage
2	T/R	Transmit/Receive Input
3, 4, 5, 6, 7, 8, 9, 10	$\begin{array}{c} A_0, \ A_1, \ A_2, \ A_3, \ A_4, \\ A_5, \ A_6, \ A_7 \end{array}$	Port-A Inputs or 3-State Outputs
11, 12, 13	GND	Ground
14, 15, 16, 17, 18, 19, 20, 21	$\begin{array}{c} B_7,  B_6,  B_5,  B_4,  B_3, \\ B_2,  B_1,  B_0 \end{array}$	Port-B Inputs or 3-State Outputs
22	/OE	Output Enable Input
23	NC	No Connect
24	V <sub>CCB</sub>	Supply Voltage



#### Table 1. Truth Table

In	puts	Outputs
/OE	T/R	
L	L	Bus B Data to Bus A
L	н	Bus A Data to Bus B
Н	X	HIGH-Z State

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

# Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Pa	Min.	Max.	Unit		
$V_{CCA}, V_{CCB}$	Supply Voltage			-0.5	7.0	V
V <sub>IN</sub>	DC Input Voltage; (/OE, T/R)			-0.5	V <sub>CCA</sub> +0.5	V
V	DC Input / Output Voltage		An	-0.5	V <sub>CCA</sub> to +0.5	V
V I/O	DC mput / Output Voltage		Bn	-0.5	V <sub>CCB</sub> to +0.5	v
I <sub>IN</sub>	DC Input Diode Current (/OE and	E and T/R)			±20	mA
Ι <sub>ΟΚ</sub>	DC Output Diode Current			±50	mA	
lo	DC Output Source or Sink Currer	nt	t			mA
		Output Pin			±50	
I <sub>CC</sub> or I <sub>GND</sub>	DC V <sub>CC</sub> or Ground Current	Maximum Current at	I <sub>CCA</sub>		±100	mA
		Maximum Current at	I <sub>CCB</sub>		±200	
T <sub>STG</sub>	Storage Temperature Range				+150	°C
I <sub>SINK</sub>	DC Latch-Up Source or Sink Current				±300	mA
TJ	Maximum Junction Temperature Under Bias				+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JE	SD22-A114		2500	V

# **Recommended Operating Conditions**

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit	
V <sub>CCA</sub>	Supply Voltage	2.7	3.6	V	
V <sub>CCB</sub>	Supply voltage	4.5	5.5	V	
VI	Input Voltage (/OE and T/R)	0	V <sub>CCA</sub>	V	
V	An An		0	V <sub>CCA</sub>	V
V I/O	De linput / Output Voltage	0	V <sub>CCB</sub>	V	
TA	Operating Temperature, Free Air	-40	+85	°C	
$\Delta t / \Delta V$	Minimum Input Edge Rate (V_IN from 30 to 70% of V <sub>CC</sub> , V <sub>CC</sub> 4.5 V, and 5.5 V)		8	ns/V	

Note:

1. Unused pins (inputs and I/O's) must be held HIGH or LOW. They may not float.

Symbol	l Paramotor		Conditions	$V_{CCA}$	$V_{CCB}$	T <sub>A</sub> = -	25°C	T <sub>A</sub> =-40 to+85°C	Uni
Зушрог	Parame	ter	Conditions	(V)	(V)	Typ. Guar		ranteed Limits	Uni
Maria		$A_n, T/R$ ,		3.6	5.0		2.0	2.0	
V IHA	Minimum	/OE	$V_{OUT} \le 0.1 \text{ V or}$	2.7	5.0		2.0	2.0	V
Maria	Input Voltage	Р	$\geq$ V <sub>CC</sub> - 0.1 V	3.3	4.5		2.0	2.0	v
VIHB		Dn		3.3	5.5		2.0	2.0	
V		A <sub>n</sub> , T/R ,		3.6	5.0		0.8	0.8	
VILA	Minimum	/OE	$V_{OUT} \le 0.1 \text{ V or}$	2.7	5.0		0.8	0.8	
N/	Input Voltage	<b>_</b>	$\geq$ V <sub>CC</sub> - 0.1 V	3.3	4.5		0.8	0.8	V
VILB		Bn		3.3	5.5		0.8	0.8	
			Ι <sub>ΟUT</sub> =-100 μΑ	3.0	4.5	2.99	2.90	2.90	
	1		I <sub>OH</sub> =-24 mA	3.0	4.5	2.65	2.35	2.25	
V <sub>OHA</sub>	Minimum HIG	HLevel	I <sub>0н</sub> =-12 mA	2.7	4.5	2.50	2.30	2.20	
	Output Voltage	e	I <sub>OH</sub> =-24 mA	2.7	4.5	2.30	2.10	2.00	V
- /			Ι <sub>ουτ</sub> =-100 μΑ	3.0	4.5	4.50	4.40	4.40	-
Vонв			I <sub>0н</sub> =-24 mA	3.0	4.5	4.25	3.86	3.76	1
			ο= Ιουτ=100 μΑ	3.0	4.5	0.002	0.100	0.100	-
			loн=24 mA	3.0	4.5	0.210	0.360	0.440	
V <sub>OLA</sub>	Minimum I OM		I <sub>он</sub> =12 mA	2.7	4.5	0.110	0.360	0.440	
	Output Voltage		loн =24 mA	2.7	4.5	0.220	0.420	0.500	١
				3.0	4.5	0.002	0 100	0.100	
$V_{OLB}$			lou=24 mA	3.0	4.5	0.180	0.360	0.440	
I <sub>IN</sub>	Maximum Inpu Leakage Curre /OE, T/R	ut ent;	V <sub>IN</sub> =V <sub>CCB</sub> , GND	3.6	5.5		±0.1	±1.0	μ
I <sub>OZA</sub>	Maximum 3-State Output Leakage; An		V <sub>IN</sub> =V <sub>IL</sub> , V <sub>IH</sub> ; /OE= V <sub>CCA</sub> ; V <sub>O</sub> =V <sub>CCA</sub> , GND	3.6	5.5		±0.5	±5.0	μ
I <sub>OZB</sub>	Maximum 3-State Output Leakage; B <sub>n</sub>		V <sub>IN</sub> =V <sub>IL</sub> , V <sub>IH</sub> ; /OE= V <sub>CCA</sub> ; V <sub>O</sub> =V <sub>CCB</sub> , GND	3.6	5.5		±0.5	±5.0	μ
	cc Maximum B <sub>n</sub> I <sub>CCT</sub> /Input at A <sub>n</sub> , T/R , /OE		V <sub>IN</sub> =V <sub>CCB</sub> -2.1 V	3.6	5.5	1.00	1.35	1.50	
Δlcc			V <sub>IN</sub> =V <sub>CCA</sub> -0.6 V	3.6	5.5		0.35	0.50	m
I <sub>CCA</sub>	Quiescent V <sub>CCA</sub> Supply Current		$\begin{array}{l} A_n = V_{CCA} \text{ or } GND, \\ B_n = V_{CCB} \text{ or } GND, \\ /OE = GND, \\ T/R = GND \end{array}$	3.6	5.5		5	50	
I <sub>CCB</sub>	Quiescent V <sub>CCB</sub> Supply Current		$A_n = V_{CCA}$ or GND, $B_n = V_{CCB}$ or GND, OE = GND, $T/B = V_{CCA}$	3.6	5.5		8	80	μı

Continued on the following page...

DC Electrical Characteristics (Continued)								
Symbol	Baramatar	Conditions	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = -25°C	T <sub>A</sub> =-40 to+85°C		Unit
Symbol	Farameter			Typ. Guaranteed Limits		nteed Limits	Unit	
V <sub>OLPA</sub>	Quiet Output Maximum		3.3	5.0		0.8		V
V <sub>OLPB</sub>	Dynamic V <sub>OL</sub> <sup>(2, 3)</sup>		3.3	5.0		1.5		v
V <sub>OLVA</sub>	Quiet Output Minimum		3.3	5.0		-0.8		V
V <sub>OLVB</sub>	Dynamic V <sub>OL</sub> <sup>(2, 3)</sup>		3.3	5.0		-1.2		v
VIHDA	Minimum HIGH Level		3.3	5.0		2.0		
VIHDB	Dynamic Input Voltage <sup>(2, 4)</sup>		3.3	5.0		2.0		V
VILDA	Maximum LOW Level		3.3	5.0		0.8		
V <sub>ILDB</sub>	Dynamic Input Voltage <sup>(2, 4)</sup>		3.3	5.0		0.8		V

Notes:

Worst-case package. 2.

3.

Maximum number of outputs defined as (n). Data inputs are driven 0 V to V<sub>CC</sub> level; one output at GND. Maximum number of data inputs (n) switching. (n-1) inputs switching 0 V to V<sub>CC</sub> level. Input-under-test switching; V<sub>CC</sub> level to threshold (V<sub>IHD</sub>), 0V to threshold (V<sub>ILD</sub>), f=1 MHz. 4.

AC Elect	rical Characte	ristics	5						
Symbol	Parameter	$\begin{array}{c} T_{A} = +25^{\circ}C, \ C_{L} = 50 \ pF, \\ V_{CCA} = 3.3 \ V_{^{(5)}}, \\ V_{CCB} = 5.0 \ V^{^{(6)}} \end{array}$		$\begin{array}{c} T_{A} = -40 \text{ to } +85^{\circ}\text{C}, \\ C_{L} = 50 \text{ pF}, \\ V_{CCA} = 3.3 \text{ V}^{(5)}, \\ V_{CCB} = 5.0 \text{ V}^{(6)} \end{array}$		T <sub>A</sub> =-40 to +85°C, C <sub>L</sub> =50 pF, V <sub>CCA</sub> =2.7 V, V <sub>CCB</sub> =5.0 V		Unit	
		Min.	Тур.	Max.	Min.	Max.	Min.	Max.	
	Propagation	1.0	5.4	8.0	1.0	8.5	1.0	9.0	
	Delay A to B	1.0	5.6	7.5	1.0	8.0	1.0	8.5	
IPHL, IPLH	Propagation Delay B to A	1.0	5.1	7.5	1.0	8.0	1.0	8.5	ns
		1.0	5.7	7.5	1.0	8.0	1.0	8.5	
	Output Enable Time /OE to B	1.0	4.8	8.0	1.0	8.5	1.0	9.0	- ns
		1.0	6.3	8.5	1.0	9.0	1.0	9.5	
ιρζ <u>L</u> , ιρζΗ	Output Enable	1.0	6.3	8.5	1.0	9.0	1.0	9.5	
	Time /OE to A	1.0	6.8	9.0	1.0	9.5	1.0	10.0	
1	Output Disable	1.0	5.3	7.5	1.0	8.0	1.0	8.5	
tpнz, tplz	Time /OE to B	1.0	4.2	7.0	1.0	7.5	1.0	8.0	ns
	Output Disable	1.0	5.3	8.0	1.0	8.5	1.0	9.0	
	Time /OE to A	1.0	3.7	6.5	1.0	7.0	1.0	7.5	
toshl, toslh	Output to Output Skew, Data to Output <sup>(7)</sup>		1.0	1.5		1.5		1.5	ns

#### Notes:

5. Voltage range 3.3 V is  $3.3 \text{ V} \pm 0.3 \text{ V}$ .

6. Voltage range 5.0 V is 5.0 V  $\pm$  0.5 V.

 Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>). Parameter guaranteed by design.

# Capacitance

Symbol	Parameter	Conditions	Тур.	Unit	
CIN	Input Capacitance	V <sub>CC</sub> = Open	4.5	pF	
C <sub>I/O</sub>	Input / Output Capacitance	V <sub>CCA</sub> = 3.3 V, V <sub>CCB</sub> = 5.0 V	15	pF	
C <sub>PD</sub>	Power Dissipation Capacitance <sup>(8)</sup>	A to B B to A	V <sub>CCA</sub> = 3.3 V, V <sub>CCB</sub> = 5.0 V	55 40	pF

Note:

8.  $C_{PD}$  is measured at 10 MHz.

## 8-Bit Dual-Supply Translating Transceiver

The 74LVX3245 is a dual-supply device capable of bidirectional signal translation. This level shifting ability provides an efficient interface between low-voltage CPU local bus with memory and a standard bus defined by  $5 \vee I/O$  levels. The device control inputs can be controlled by the low-voltage CPU and core logic or a bus arbitrator with  $5 \vee I/O$  levels.

Manufactured on a sub-micron CMOS process, the 74LVX3245 is ideal for mixed voltage applications such as notebook computers using 3.3 V CPUs and 5 V peripheral devices.



Figure 4. Application Example

#### **Power-Up Considerations**

To ensure that the system does not experience unnecessary  $I_{CC}$  current draw, bus contention, or oscillations during power up; the following guidelines should be followed to (*refer to Table 2*):

- Power up the control side of the device first (V<sub>CCA</sub>).
- /OE should ramp with or ahead of V<sub>CCA</sub>. This helps guard against bus contention.
- The Transmit/Receive (T/R) control pin should ramp with V<sub>CCA</sub>. This ensures that the A-port data pins are configured as inputs. With V<sub>CCA</sub> receiving power first, the I/O port should be configured as an input to help guard against bus contention and oscillations.
- A-side data inputs should be driven to a valid logic level. This prevents excessive current draw.

The above steps ensure that there are no bus contentions or oscillations, and therefore no excessive current draw occurs during the power-up cycling. These steps help prevent possible damage to the translator devices and potential damage to other system components.

	Table 2.	Low Voltage Translator Power-Up Sequencing
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Device	V <sub>CCA</sub>	V <sub>CCB</sub>	T/R	/OE	A-Side I/O	B-Side I/O	Floatable Pin Allowed
74LVX3245	3 V (Power-Up First)	5 V Configurable	Ramp with V <sub>CCA</sub>	Ramp with V <sub>CCA</sub>	Logic 0 V or V <sub>CCA</sub>	Outputs	No





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