



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

FAN73832

Half-Bridge Gate-Drive IC

Features

- Floating Channel for Bootstrap Operation to +600V
- Typically 350mA/650mA Sourcing/Sinking Current Driving Capability for Both Channels
- Extended Allowable Negative V_S Swing to -9.8V for Signal Propagation at $V_{DD}=V_{BS}=15V$
- High-Side Output in Phase of IN Signal
- Built-in UVLO Functions for Both Channels
- Built-in Common-Mode dv/dt Noise Canceling Circuit
- Internal 400ns Minimum Dead-Time at $R_{DT}=20K\Omega$
- Programmable Turn-on Delay-Time Control (Dead-Time)

Applications

- SMPS
- Motor Drive Inverter
- Fluorescent Lamp Ballast
- HID Ballast

Description

The FAN73832 is a half-bridge, gate-drive IC with shut-down and programmable dead-time control functions for driving MOSFETs and IGBTs, operating up to +600V.

Fairchild's high-voltage process and common-mode noise canceling technique provide stable operation of high-side driver under high dv/dt noise circumstances.

An advanced level-shift circuit allows high-side gate driver operation up to $V_S=-9.8V$ (typical) for $V_{BS}=15V$.

The UVLO circuits for both channels prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

Output drivers typically source/sink 350mA/650mA, respectively, which is suitable for all kinds of half- and full-bridge inverters.

8-SOP



8-DIP



Ordering Information

Part Number	Package	Pb-Free	Operating Temperature Range	Packing Method
FAN73832M ⁽¹⁾	8-SOP	Yes	-40°C ~ 125°C	Tube
FAN73832MX ⁽¹⁾				Tape & Reel
FAN73832N	8-DIP			Tube

Note:

1. These devices passed wave soldering test by JESD22A-111.

Typical Application Diagrams

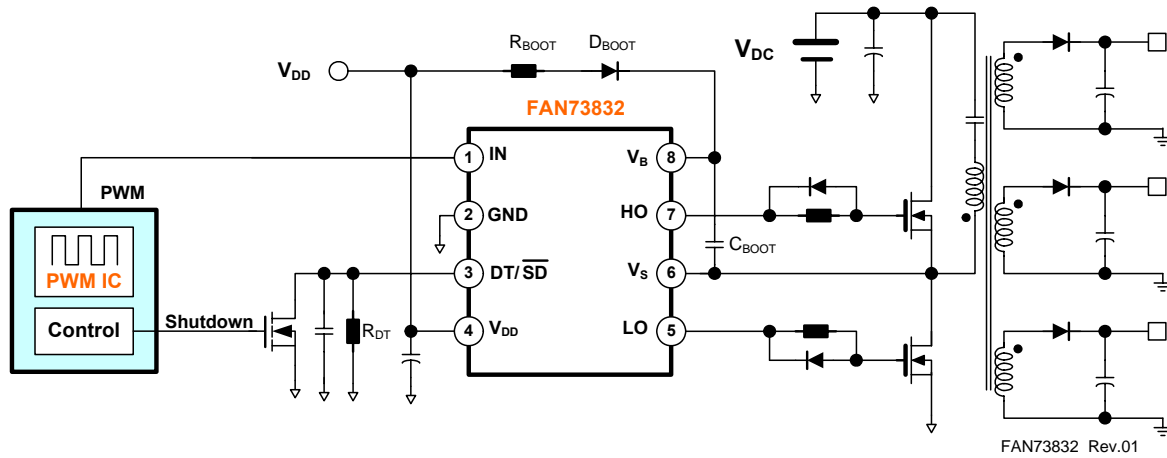


Figure 1. Application Circuit for Half-Bridge Switching Power Supply

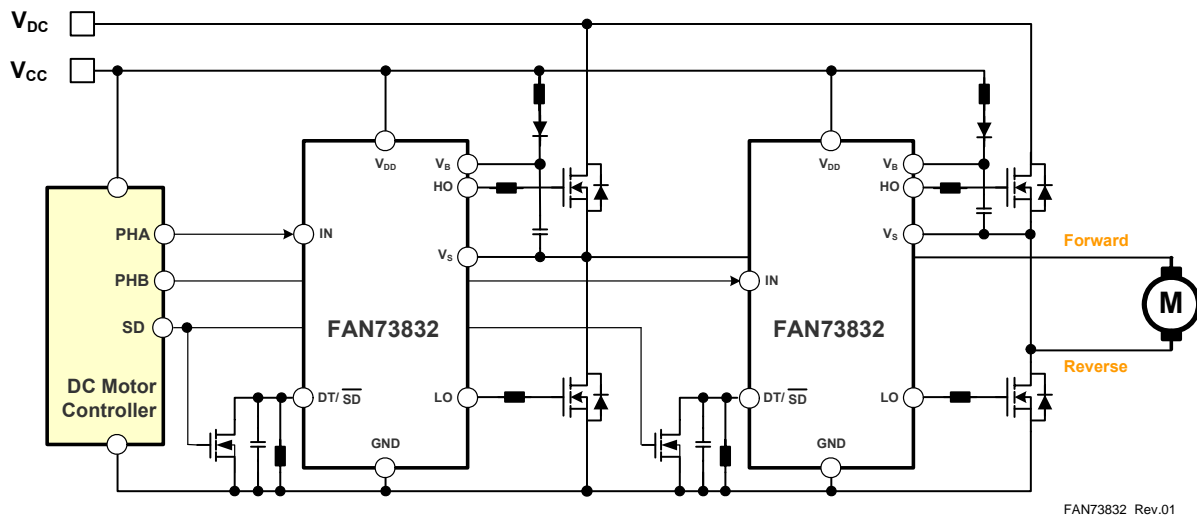


Figure 2. Application Circuit for Full-Bridge DC Motor Driver

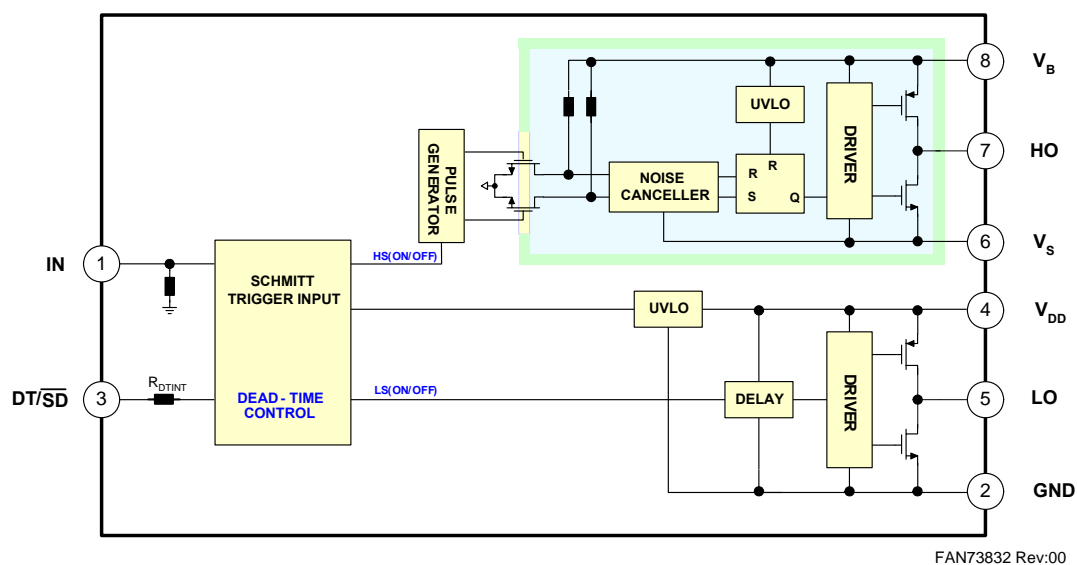


Figure 3. Functional Block Diagram of FAN73832

Pin Assignments

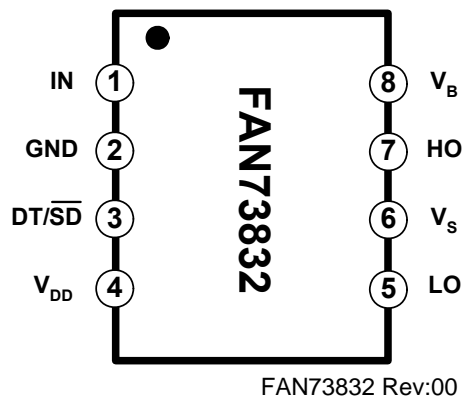


Figure 4. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	IN	Logic Input
2	GND	Ground
3	DT/ $\overline{\text{SD}}$	Dead-Time Control with External Resistor and Shutdown Function
4	V _{DD}	Low-Side Supply Voltage
5	LO	Low-Side Driver Output
6	V _S	High-Side Floating Supply Return
7	HO	High-Side Driver Output
8	V _B	High-Side Floating Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A=25^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter		Min.	Max.	Unit
V_S	High-side offset voltage		V_B-25	$V_B+0.3$	V
V_B	High-side floating supply voltage		-0.3	625	V
V_{HO}	High-side floating output voltage HO		$V_S-0.3$	$V_B+0.3$	V
V_{DD}	Low-side and logic-fixed supply voltage		-0.3	25	V
V_{LO}	Low-side output voltage LO		-0.3	$V_{DD}+0.3$	V
V_{IN}	Logic input voltage (IN)		-0.3	$V_{DD}+0.3$	V
$V_{DT/\overline{SD}}$	Dead-time and shutdown control voltage		-0.3	5.0	V
GND	Logic ground		$V_{DD}-25$	$V_{DD}+0.3$	V
dV_S/dt	Allowable offset voltage slew rate			50	V/ns
$P_D^{(2)(3)(4)}$	Power dissipation	8-SOP		0.625	W
		8-DIP		1.25	
θ_{JA}	Thermal resistance, junction-to-ambient	8-SOP		200	$^{\circ}\text{C/W}$
		8-DIP		100	
T_J	Junction temperature			150	$^{\circ}\text{C}$
T_{STG}	Storage temperature			150	$^{\circ}\text{C}$

Notes:

- Mounted on 76.2 x 114.3 x 1.6mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:
 JESD51-2: Integral circuits thermal test method environmental conditions - Natural convection
 JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages
- Do not exceed P_D under any circumstances.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min.	Max.	Unit
V_B	High-side floating supply voltage		V_S+15	V_S+20	V
V_S	High-side floating supply offset voltage		$6-V_{DD}$	600	V
V_{DD}	Low-side supply voltage		15	20	V
V_{HO}	High-side (HO) output voltage		V_S	V_B	V
V_{LO}	Low-side (LO) output voltage		GND	V_{DD}	V
V_{IN}	Logic input voltage (IN)		GND	V_{DD}	V
T_A	Ambient temperature		-40	125	$^{\circ}\text{C}$

Electrical Characteristics

V_{BIAS} (V_{DD} , V_{BS})=15.0V, R_{DT} =20K Ω , T_A =25°C, unless otherwise specified. The V_{IN} and I_{IN} parameters are referenced to GND. The V_O and I_O parameters are referenced to V_S and COM and are applicable to the respective outputs HO and LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SUPPLY CURRENT SECTION						
I _{QBS}	Quiescent V _{BS} supply current	V _{IN} =0V or 5V		35	90	μA
I _{QDD}	Quiescent V _{DD} supply current	V _{IN} =0V or 5V, R _{DT} =20KΩ		300	450	
I _{SD} ⁽⁵⁾	Shutdown supply current	DT/ \overline{SD} =GND		650	900	
I _{PBS}	Operating V _{BS} supply current	f _{IN} =20kHz, rms value		400	700	
I _{PDD}	Operating V _{DD} supply current	f _{IN} =20kHz, rms value		650	850	
I _{LK}	Offset supply leakage current	V _B =V _S =600V			10	
POWER SUPPLY SECTION						
V _{DDUV+} V _{BSUV+}	V _{DD} and V _{BS} supply under-voltage positive going threshold		10.7	11.6	12.5	V
V _{DDUV-} V _{BSUV-}	V _{DD} and V _{BS} supply under-voltage negative going threshold		10.0	10.8	11.6	V
V _{DDUVH} V _{BSUVH}	V _{DD} supply under-voltage lockout hysteresis			0.8		V
DEAD-TIME CONTROL SECTION						
R _{DTINT}	Internal dead-time setting resistance			20		KΩ
V _{DT}	Normal voltage at DT	R _{DT} =20KΩ		3.0		V
GATE DRIVER OUTPUT SECTION						
V _{OH}	High-level output voltage, V _{BIAS} -V _O	I _O =20mA			1.0	V
V _{OL}	Low-level output voltage, V _O				0.6	V
I _{O+}	Output high short-circuit pulse current	V _O =0V, V _{IN} =5V with PW<10μs	250	350		mA
I _{O-}	Output low short-circuit pulsed current	V _O =15V, V _{IN} =0V with PW<10μs	500	650		mA
V _S	Allowable negative V _S pin voltage for IN signal propagation to HO			-9.8	-7.0	V
LOGIC INPUT SECTION (INPUT and SHUTDOWN)						
V _{IH}	Logic "1" input voltage		2.9			V
V _{IL}	Logic "0" input voltage				1.2	V
I _{IN+}	Logic "1" input bias current	V _{IN} =5V		50	100	μA
I _{IN-}	Logic "0" input bias current	V _{IN} =0V			2.0	μA
$\overline{SD+}$	Shutdown "1" input voltage				1.2	V
$\overline{SD-}$	Shutdown "0" input voltage		2.9			V
R _{PD}	Input pull-down resistance			100		KΩ

Note:

5. This parameter guaranteed by design.

Dynamic Electrical Characteristics

V_{BIAS} (V_{DD} , V_{BS})=15.0V, V_S =GND, C_L =1000pF, R_{DT} =20K Ω and T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{ON}	Turn-on propagation delay	$V_S=0V$, $R_{DT}=20K\Omega$		580	730	ns
t_{OFF}	Turn-off propagation delay	$V_S=0V$ or 600V ⁽⁵⁾ , $R_{DT}=20K\Omega$		180	230	
t_R	Turn-on rise time	$C_L=1000pF$		50	100	
t_F	Turn-off fall time	$C_L=1000pF$		30	80	
$t_{SD}^{(5)}$	Shutdown propagation delay			100	180	
DT1, DT2	Dead-time LO OFF to HO ON & HO OFF to LO ON	$R_{DT}=20K\Omega$	300	400	500	ns
		$R_{DT}=200K\Omega$	1.20	1.68	2.30	μs
DMT	Dead-time matching	$R_{DT}=20K\Omega$		0	60	ns
		$R_{DT}=200K\Omega$		0	150	

Note:

5. These parameters guaranteed by design.

Typical Characteristics

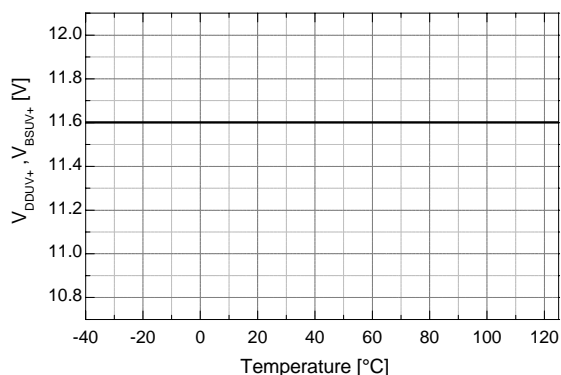


Figure 5. V_{DD}/V_{BS} UVLO (+) vs. Temperature

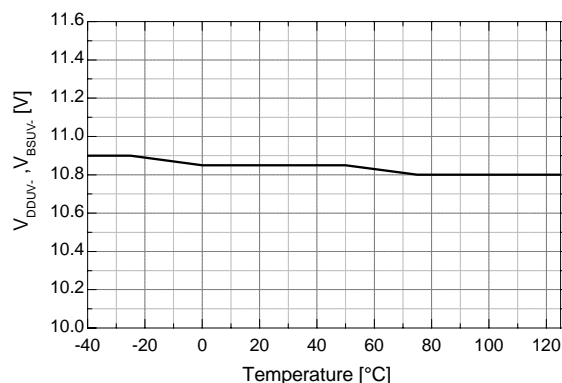


Figure 6. V_{DD}/V_{BS} UVLO (-) vs. Temperature

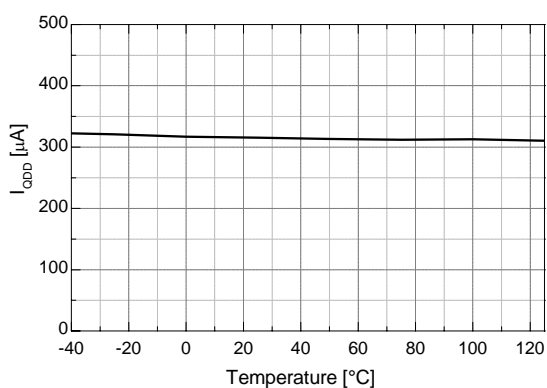


Figure 7. V_{DD} Quiescent Current vs. Temperature

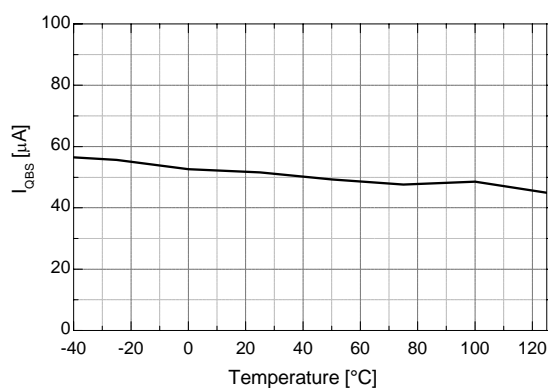


Figure 8. V_{BS} Quiescent Current vs. Temperature

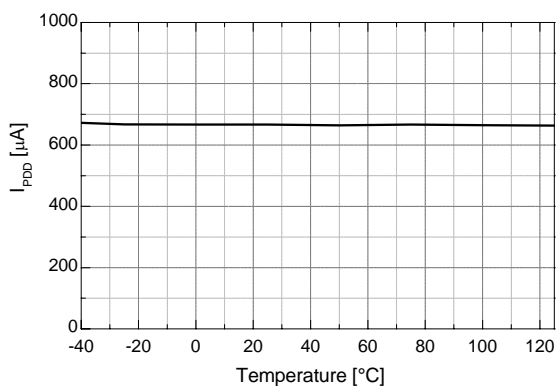


Figure 9. V_{DD} Operating Current vs. Temperature

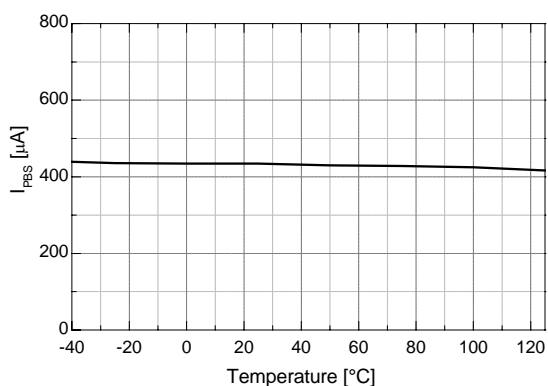


Figure 10. V_{BS} Operating Current vs. Temperature

Typical Characteristics (Continued)

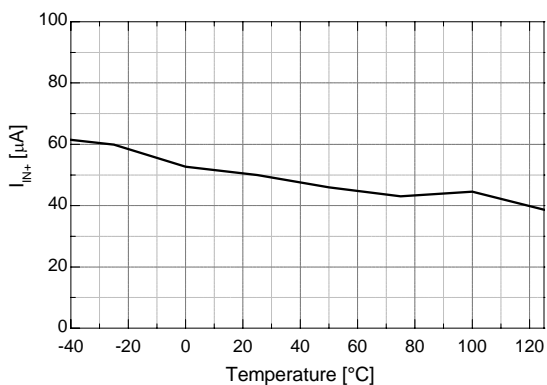


Figure 11. Logic Input Current vs. Temperature

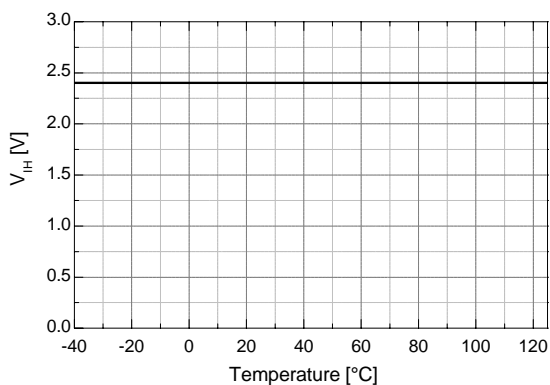


Figure 12. Logic Input High Voltage vs. Temperature

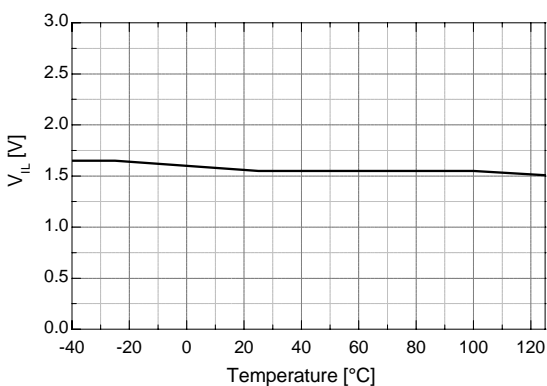


Figure 13. Logic Input Low Voltage vs. Temperature

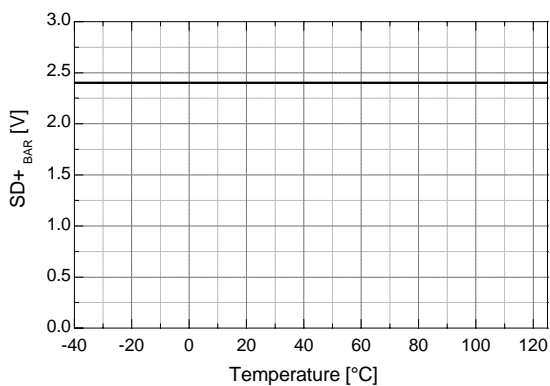


Figure 14. \overline{SD} Positive Threshold vs. Temperature

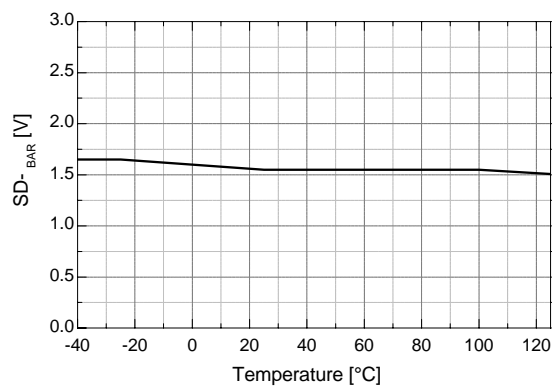


Figure 15. \overline{SD} Negative Threshold vs. Temperature

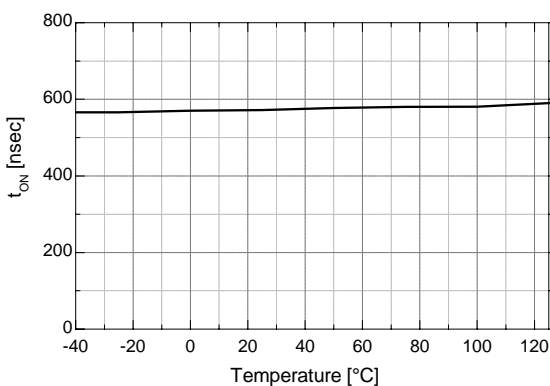


Figure 16. Turn-on Delay Time vs. Temperature

Typical Characteristics (Continued)

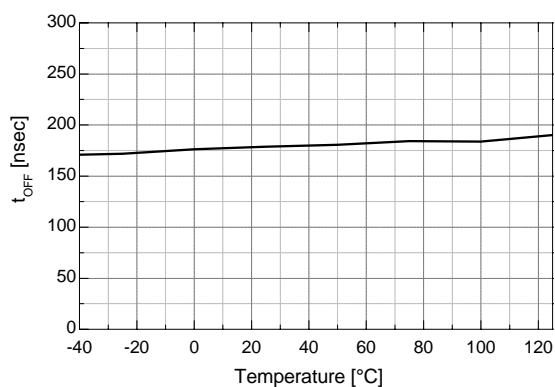


Figure 17. Turn-off Delay Time vs. Temperature

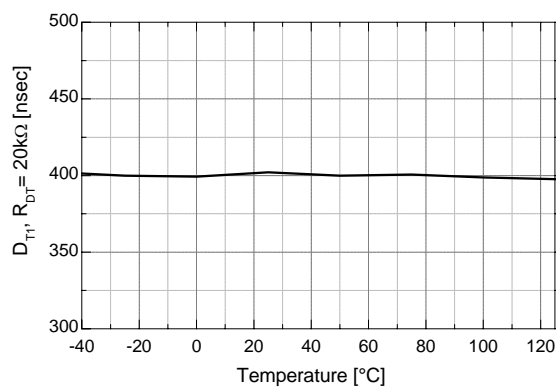


Figure 18. Dead-Time ($R_{DT}=20k\Omega$) vs. Temperature

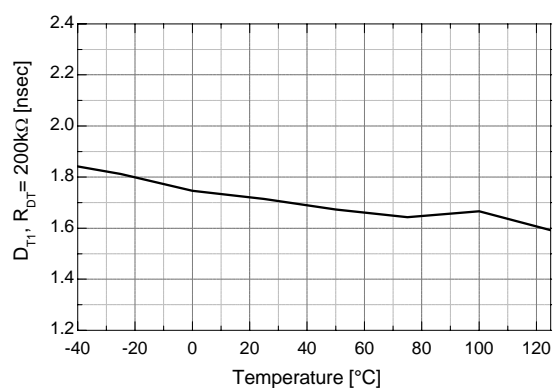


Figure 19. Dead Time ($R_{DT}=200k\Omega$) vs. Temperature

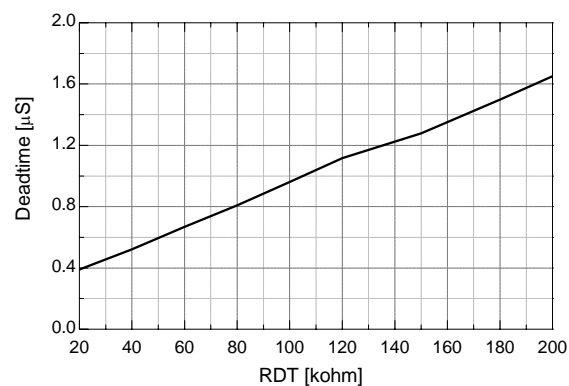


Figure 20. R_{DT} vs. Dead-Time

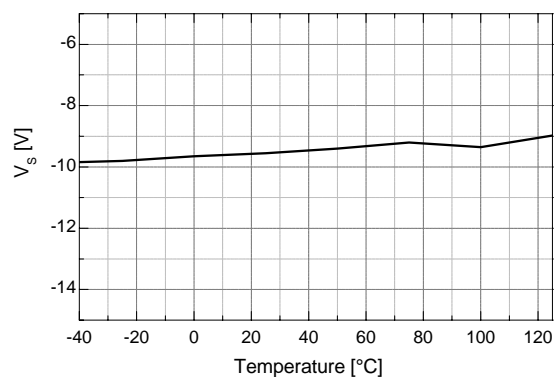


Figure 21. Allowable Negative V_S Voltage for Signal Propagation to High Side vs. Temperature

Switching Time Definitions

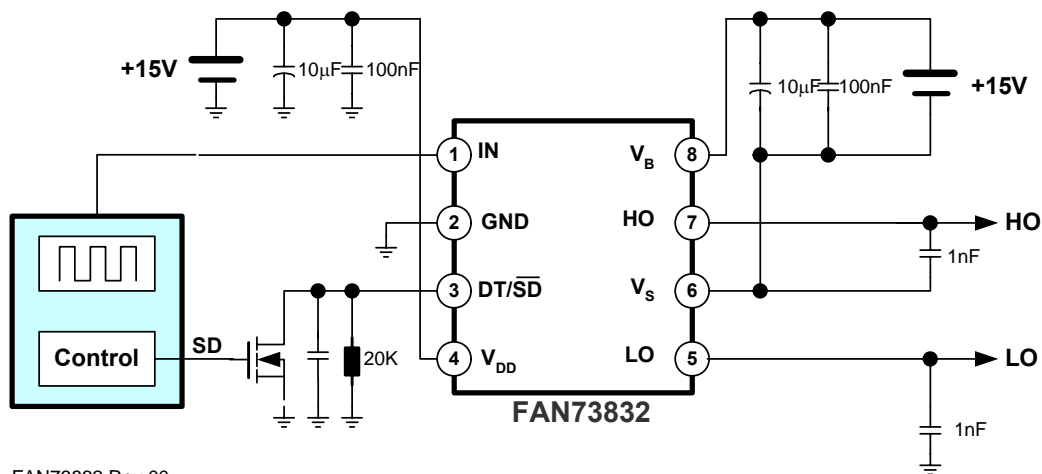


Figure 22. Switching Time Test Circuit

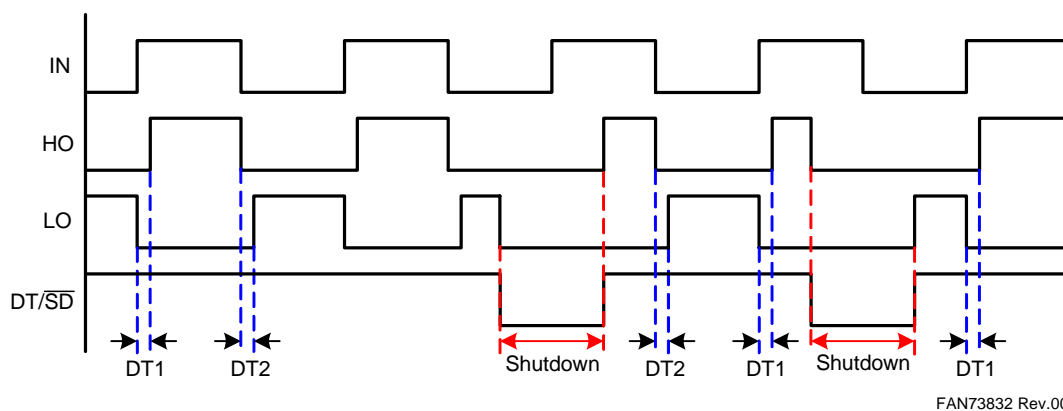


Figure 23. Input / Output Waveforms

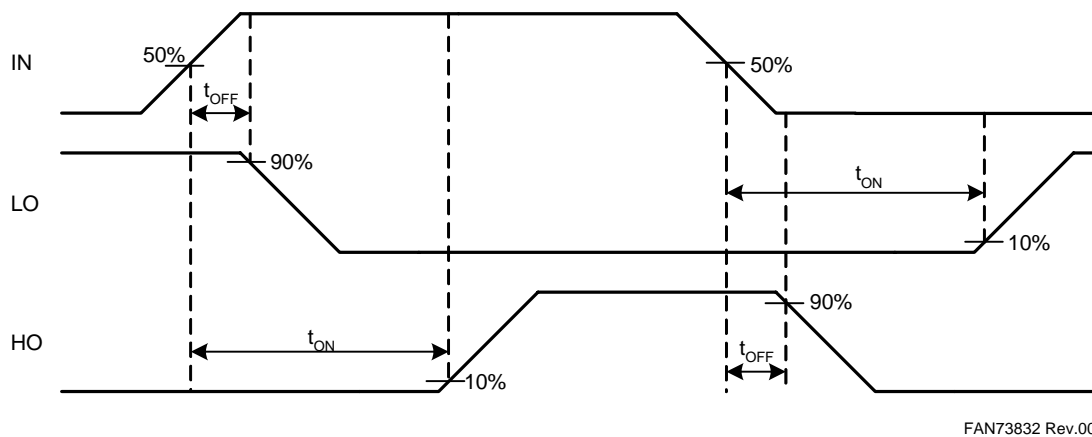


Figure 24. Switching Time Waveform Definitions

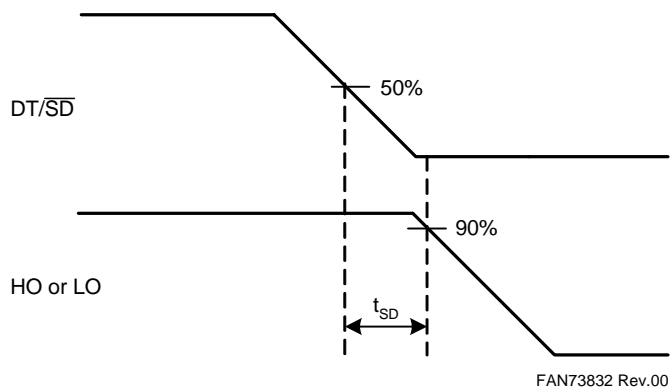


Figure 25. Shutdown Waveform Definition

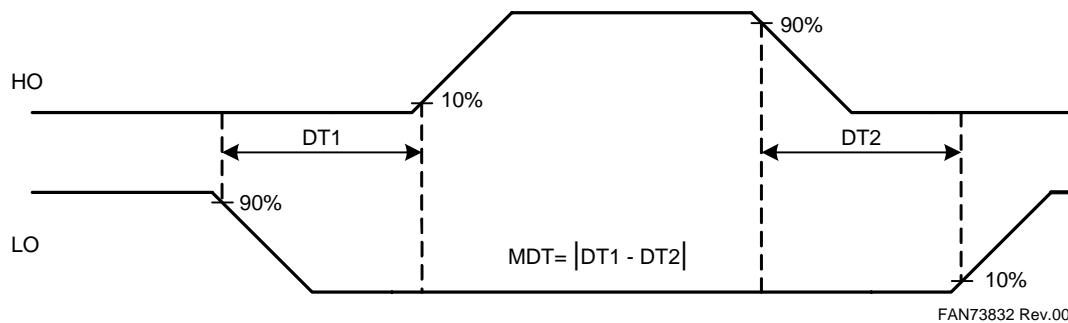


Figure 26. Dead-Time Control Waveform Definition

Typical Application Information

1. Normal Operating Consideration

The FAN73832 is a single PWM input, half-bridge, gate-drive IC with programmable dead-time and shutdown functions.

The dead-time is set with a resistor (R_{DT}) at the DT/\overline{SD} pin. The wide dead-time programming range provides the flexibility to optimize drive signal timing for a selection of switching devices (MOSFET or IGBT) and applications.

The turn-on time delay circuitry (Dead-Time) accommodates resistor values from $20k\Omega$ to $200k\Omega$ with a dead-time proportional to the R_{DT} resistance.

If the DT/\overline{SD} pin voltage decreases below 1.2V in the normal operation, the IC enters shutdown mode.

The external dead-time setting resistor (R_{DT}) is at least above $20K\Omega$ for normal operation in typical applications.

2. Under-Voltage Lockout (UVLO)

The FAN73832 has an under-voltage lockout (UVLO) protection circuit for high- and low-side channels to prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage. The UVLO circuitry monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (V_{BS}) antepenuit.

3. Layout Consideration

For optimum performance of the high- and low-side gate drivers, considerations must be taken during printed circuit board (PCB) layout.

3.1 Supply Capacitors

If the output stages are able to quickly turn-on a switching device with a high value of current, the supply capacitors must be placed as close as possible to the device pins (V_{DD} and GND for the ground-tied supply, V_B and V_S for the floating supply) to minimize parasitic inductance and resistance.

3.2 Gate Drive Loop

Current loops behave like an antenna, able to receive and transmit noise. To reduce the noise coupling/emission and improve the power switch turn-on and off performances, gate drive loops must be reduced as much as possible.

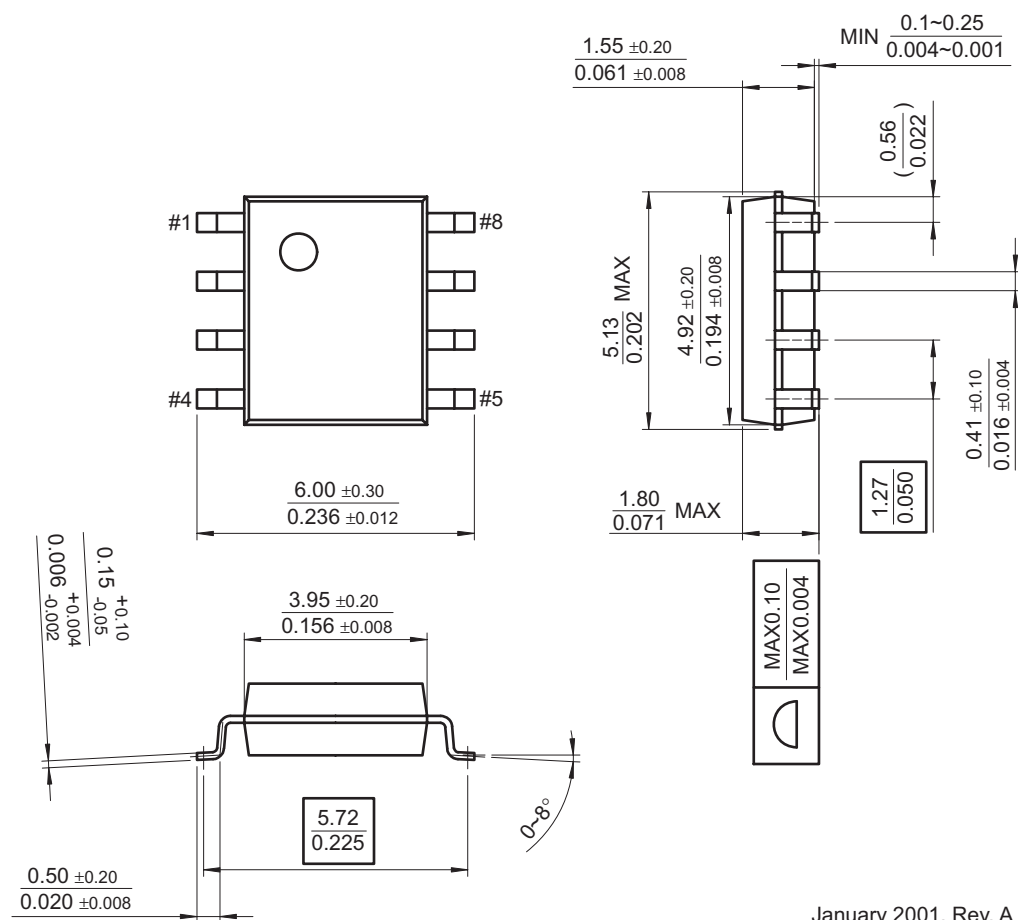
3.3 Ground Plane

Ground plane must not be placed under or nearby the high-voltage floating side to minimize noise coupling.

Mechanical Dimensions

8-SOP

Dimensions are in millimeters (inches) unless otherwise noted.




January 2001, Rev. A
8sop225_dim.pdf

Figure 27. 8-Lead Small Outline Package (SOP)



TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE [®]	HiSeC [™]	PowerTrench [®]	TinyLogic [®]
Across the board. Around the world. [™]	i-Lo [™]	Programmable Active Droop [™]	TINYOPTO [™]
ActiveArray [™]	ImpliedDisconnect [™]	QFET [®]	TinyPower [™]
Bottomless [™]	IntelliMAX [™]	QS [™]	TinyWire [™]
Build it Now [™]	ISOPPLANAR [™]	QT Optoelectronics [™]	TruTranslation [™]
CoolFET [™]	MICROCOUPLER [™]	Quiet Series [™]	μSerDes [™]
CROSSVOLT [™]	MicroPak [™]	RapidConfigure [™]	UHC [®]
CTL [™]	MICROWIRE [™]	RapidConnect [™]	UniFET [™]
Current Transfer Logic [™]	MSX [™]	ScalarPump [™]	VCX [™]
DOME [™]	MSXPro [™]	SMART START [™]	Wire [™]
E ² C [™]	OCX [™]	SPM [®]	
EcoSPARK [®]	OCXPro [™]	SuperFET [™]	
EnSigna [™]	OPTOLOGIC [®]	SuperSOT [™] -3	
FACT Quiet Series [™]	OPTOPLANAR [®]	SuperSOT [™] -6	
FACT [®]	PACMAN [™]	SuperSOT [™] -8	
FAST [®]	POP [™]	TCM [™]	
FASTr [™]	Power220 [®]	The Power Franchise [®]	
FPS [™]	Power247 [®]	 ™	
FRFET [®]	PowerEdge [™]	TinyBoost [™]	
GlobalOptoisolator [™]	PowerSaver [™]	TinyBuck [™]	
GTO [™]			

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild Semiconductor. The datasheet is printed for reference information only.

Rev. I23

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative