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FDA15N65 650V N-Channel MOSFET

Features

- + 16A, 650V, $\mathsf{R}_{\mathsf{DS}(\mathsf{on})}$ = 0.44 Ω @V_{GS} = 10 V
- Low gate charge (typical 48.5 nC)
- Low C_{rss} (typical 23.6 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



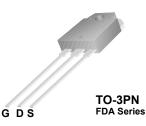
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.

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Absolute Maximum Ratings

Symbol	Parameter			FDA15N65	Unit
V _{DSS}	Drain-Source Voltage			650	V
I _D	Drain Current	- Continuous (T _C = 25°C) - Continuous (T _C = 100°C)	- Continuous (T _C = 25°C) - Continuous (T _C = 100°C)		A A
I _{DM}	Drain Current	- Pulsed	(Note 1)	64	A
V _{GSS}	Gate-Source voltage			± 30	V
E _{AS}	Single Pulsed Avalanche Energy		(Note 2)	637	mJ
I _{AR}	Avalanche Current		(Note 1)	16	А
E _{AR}	Repetitive Avalanche Energy		(Note 1)	26	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P _D	Power Dissipation	(T _C = 25°C) - Derate above 25°C		260 2.1	W W/°C
T _{J,} T _{STG}	Operating and Storage Temperature Range			-55 to +150	°C
Τ _L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	Min.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		0.48	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.24		°C/W
$R_{ hetaJA}$	Thermal Resistance, Junction-to-Ambient		40	°C/W

		Device	Pac	kage	Reel Size Tap		be Width		Quantity	
)-3PN					30			
Electric	al Char	acteristics T _c	= 25°C unle	ss otherwise no	ted					
Symbol		Parameter			Conditions		Min	Тур	Max	Units
Off Charac	teristics									
BV _{DSS}	Drain-Source Breakdown Voltage		V _{GS} = 0V, I _D = 250μA, T _J = 25°C		650			V		
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient		$I_D = 250\mu A$, Referenced to 25°C			0.65		V/∘C		
I _{DSS}	Zero Gate Voltage Drain Current		V _{DS} = 650V, V _{GS} = 0V V _{DS} = 520V, T _C = 125°C				1 10	μΑ μΑ		
I _{GSSF}	Gate-Bod	y Leakage Current, F	orward	-	/, V _{DS} = 0V				100	nA
I _{GSSR}	Gate-Bod	y Leakage Current, R	everse	$V_{GS} = -30V, V_{DS} = 0V$					-100	nA
On Charac	teristics				-					
V _{GS(th)}	Gate Threshold Voltage		V _{DS} = V _{GS} , I _D = 250μA		3.0		5.0	V		
R _{DS(on)}	Static Drain-Source On-Resistance		V _{GS} = 10V, I _D = 8A			0.36	0.44	Ω		
9 _{FS}	Forward Transconductance		$V_{DS} = 40V, I_D = 8A$ (Note 4)			19.2		S		
Dynamic C	haracteris	tics		1						
C _{iss}	Input Capacitance Output Capacitance			V _{DS} = 25V, V _{GS} = 0V,			2380	3095	pF	
C _{oss}			f = 1.0MHz			295	385	pF		
C _{rss}	Reverse Transfer Capacitance						23.6	35.5	pF	
Switching	Characteri	stics								
t _{d(on)}	Turn-On Delay Time			5V, I _D = 15A			65	140	ns	
t _r	Turn-On F	Rise Time		R _G = 21.7Ω			125	260	ns	
t _{d(off)}	Turn-Off	Delay Time						105	220	ns
t _f	Turn-Off F	all Time				(Note 4, 5)		65	140	ns
Qg	Total Gate	e Charge		V_{DS} = 520V, I _D = 15A V_{GS} = 10V (Note 4, 5)			48.5	63.0	nC	
Q _{gs}	Gate-Sou	rce Charge					14.0		nC	
Q _{gd}	Gate-Drai	n Charge					21.2		nC	
Drain-Sour	ce Diode (Characteristics and	Maximun	Ratings						
I _S	Maximum Continuous Drain-Source Dioc			de Forward	Current				16	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Fo		prward Current				64	Α		
V _{SD}	Drain-Sou	Irce Diode Forward V	oltage	V _{GS} = 0V,	I _S = 16A				1.4	V
t _{rr}	Reverse F	Recovery Time		V _{GS} = 0V,				496		ns
Q _{rr}	Reverse F	Recovery Charge		dI _F /dt =100A/μs (Note 4)			5.69		μC	

NOTES:

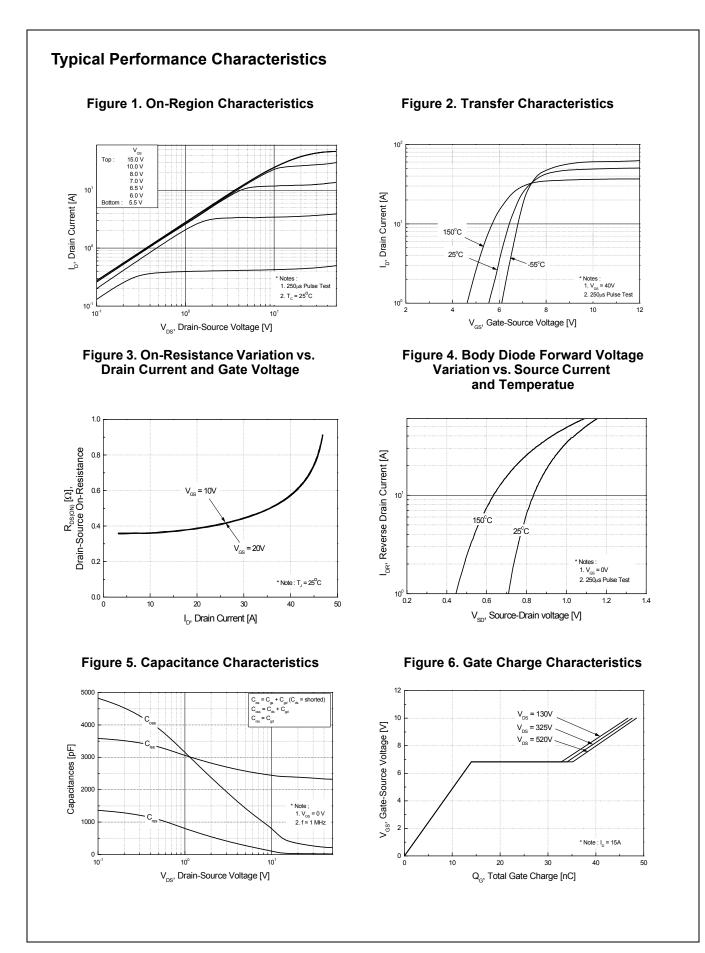
1. Repetitive Rating: Pulse width limited by maximum junction temperature

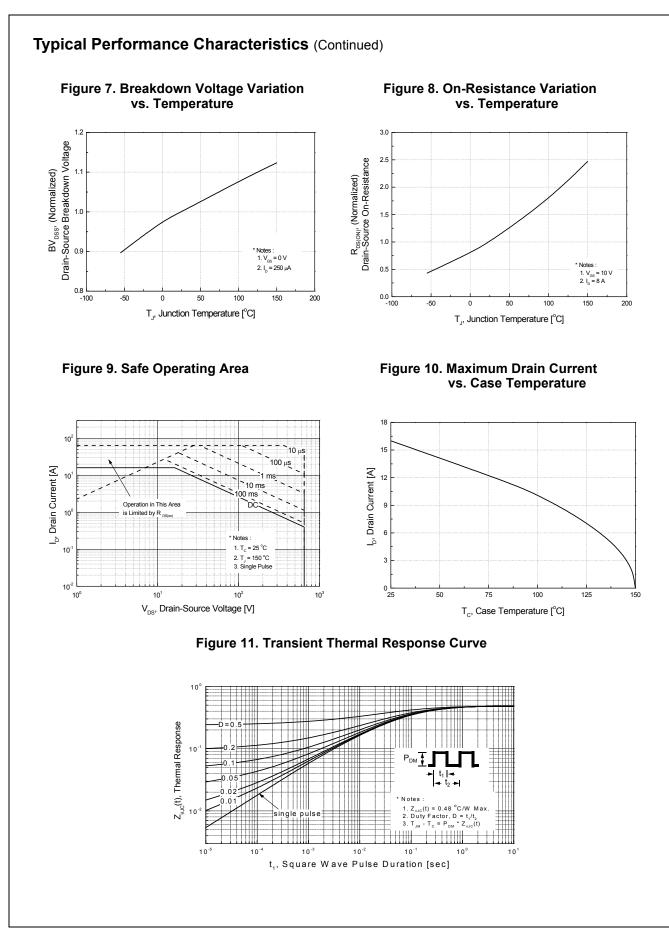
2. L = 4.6mH, I_{AS} = 16A, V_{DD} = 50V, R_G = 25 Ω , Starting T_J = 25°C

3. I_{SD} \leq 16A, di/dt \leq 200A/ $\mu s,~V_{DD} \leq BV_{DSS},~Starting~T_J$ = 25°C

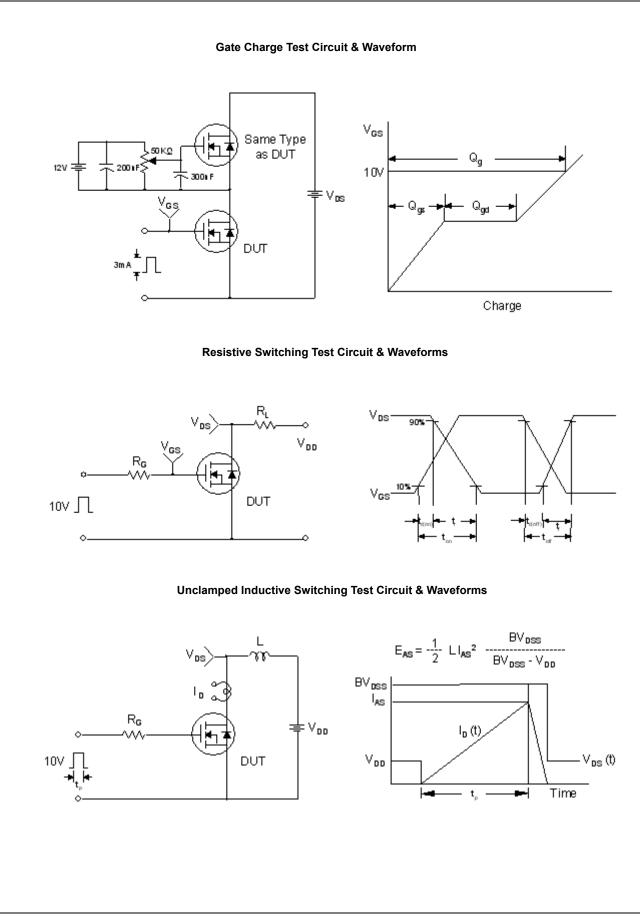
4. Pulse Test: Pulse width $\leq 300 \mu s,$ Duty Cycle $\leq 2\%$

5. Essentially Independent of Operating Temperature Typical Characteristics

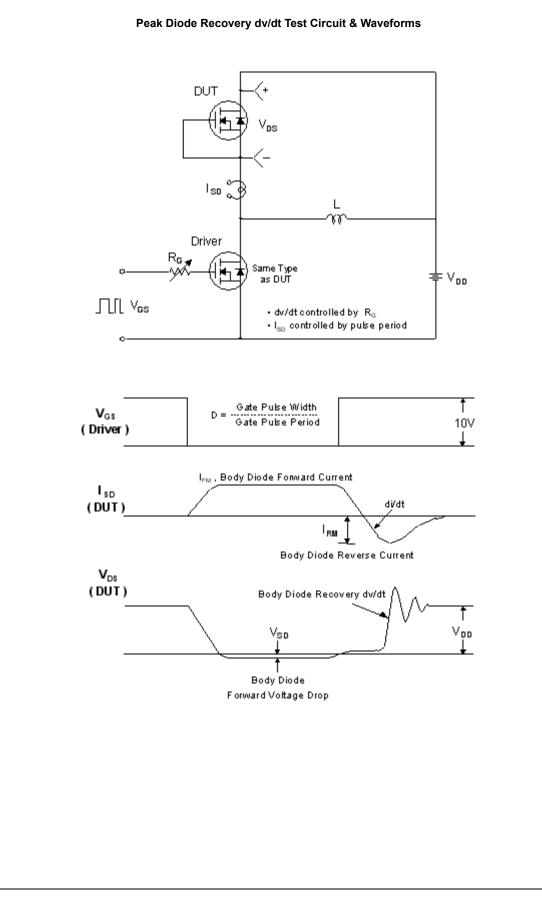


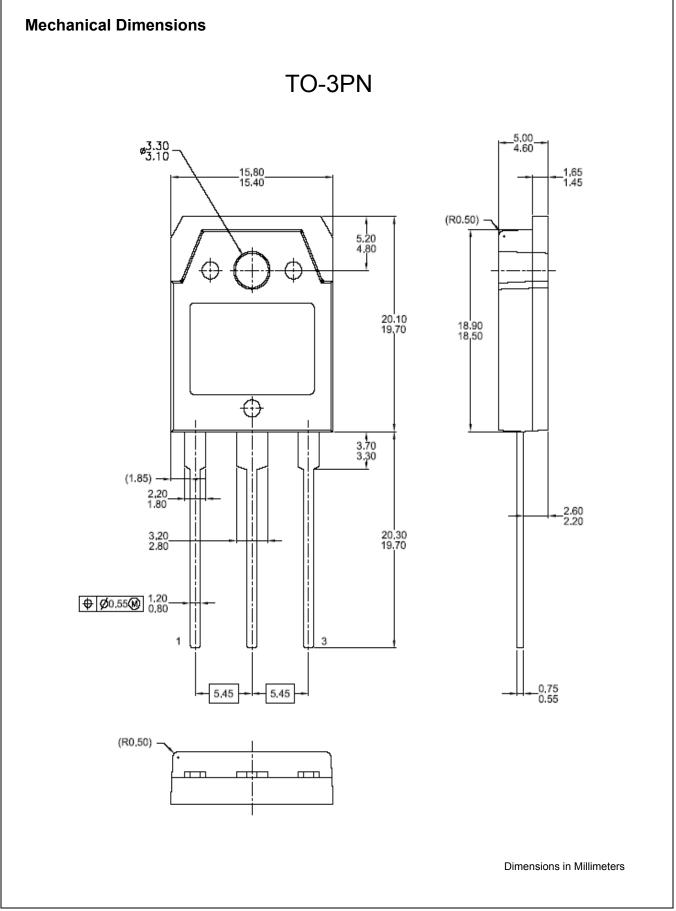


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