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FDD8424H_F085

Dual N & P-Channel PowerTrench® MOSFET
N-Channel: 40V, 20A, 24mΩ P-Channel: -40V, -20A, 54mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 24mΩ at $V_{GS} = 10V$, $I_D = 9.0A$
- Max $r_{DS(on)}$ = 30mΩ at $V_{GS} = 4.5V$, $I_D = 7.0A$

Q2: P-Channel

- Max $r_{DS(on)}$ = 54mΩ at $V_{GS} = -10V$, $I_D = -6.5A$
- Max $r_{DS(on)}$ = 70mΩ at $V_{GS} = -4.5V$, $I_D = -5.6A$
- Fast switching speed
- Qualified to AEC Q101
- RoHS Compliant

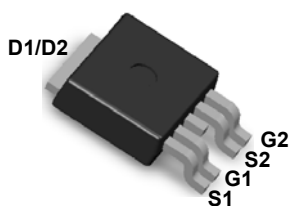


General Description

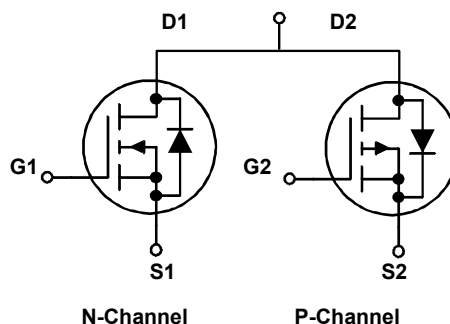
These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench- process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

Application

- Inverter
- H-Bridge



Dual DPAK 4L



N-Channel

P-Channel

MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

| Symbol | Parameter | Q1 | Q2 | Units |
|-----------------|--|-----|-----|-------|
| V _{DS} | Drain to Source Voltage | 40 | -40 | V |
| V _{GS} | Gate to Source Voltage | ±20 | ±20 | V |
| I _D | Drain Current - Continuous (Package Limited) | 20 | -20 | A |
| | | | | |

Thermal Characteristics

| | | | |
|-----------------|--|-----|--------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case, Single Operation for Q1 (Note 1) | 4.1 | $^\circ C/W$ |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case, Single Operation for Q2 (Note 1) | 3.5 | |

Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|----------------|----------|-----------|-----------|------------|------------|
| FDD8424H | FDD8424H | TO-252-4L | 13" | 12mm | 2500 units |

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|--------|-----------|-----------------|------|-----|-----|-----|-------|
|--------|-----------|-----------------|------|-----|-----|-----|-------|

Off Characteristics

| | | | | | | | |
|--------------------------------------|---|---|----------|-----------|-----------|------------------------|----------------------|
| BV_{DSS} | Drain to Source Breakdown Voltage | $I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ $I_D = -250\mu\text{A}$, $V_{GS} = 0\text{V}$ | Q1 Q2 | 40 -40 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\mu\text{A}$, referenced to 25°C $I_D = -250\mu\text{A}$, referenced to 25°C | Q1 Q2 | | 34 -32 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 32\text{V}$, $V_{GS} = 0\text{V}$ $V_{DS} = -32\text{V}$, $V_{GS} = 0\text{V}$ | Q1 Q2 | | | 1 -1 | μA |
| I_{GSS} | Gate to Source Leakage Current | $V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$ | Q1 Q2 | | | ± 100 ± 100 | nA nA |

On Characteristics

| | | | | | | | |
|--|--|--|----------|---------|----------------|----------------|----------------------|
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ $V_{GS} = V_{DS}$, $I_D = -250\mu\text{A}$ | Q1 Q2 | 1 -1 | 1.7 -1.6 | 3 -3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D = 250\mu\text{A}$, referenced to 25°C $I_D = -250\mu\text{A}$, referenced to 25°C | Q1 Q2 | | -5.3 4.8 | | mV/ $^\circ\text{C}$ |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS} = 10\text{V}$, $I_D = 9.0\text{A}$ $V_{GS} = 4.5\text{V}$, $I_D = 7.0\text{A}$ $V_{GS} = 10\text{V}$, $I_D = 9.0\text{A}$, $T_J = 125^\circ\text{C}$ | Q1 | | 19 23 29 | 24 30 37 | m Ω |
| | | $V_{GS} = -10\text{V}$, $I_D = -6.5\text{A}$ $V_{GS} = -4.5\text{V}$, $I_D = -5.6\text{A}$ $V_{GS} = -10\text{V}$, $I_D = -6.5\text{A}$, $T_J = 125^\circ\text{C}$ | Q2 | | 42 58 62 | 54 70 80 | |
| g_{FS} | Forward Transconductance | $V_{DS} = 5\text{V}$, $I_D = 9.0\text{A}$ $V_{DS} = -5\text{V}$, $I_D = -6.5\text{A}$ | Q1 Q2 | | 29 13 | | S |

Dynamic Characteristics

| | | | | | | | |
|-----------|------------------------------|--|----------|--|-------------|--------------|----------|
| C_{iss} | Input Capacitance | Q1 $V_{DS} = 20\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ | Q1 Q2 | | 750 1000 | 1000 1330 | pF |
| C_{oss} | Output Capacitance | Q2 | Q1 Q2 | | 115 140 | 155 185 | pF |
| C_{rss} | Reverse Transfer Capacitance | $V_{DS} = -20\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ | Q1 Q2 | | 75 75 | 115 115 | pF |
| R_g | Gate Resistance | $f = 1\text{MHz}$ | Q1 | | 1.1 | | Ω |
| | | | Q2 | | 3.3 | | |

Switching Characteristics

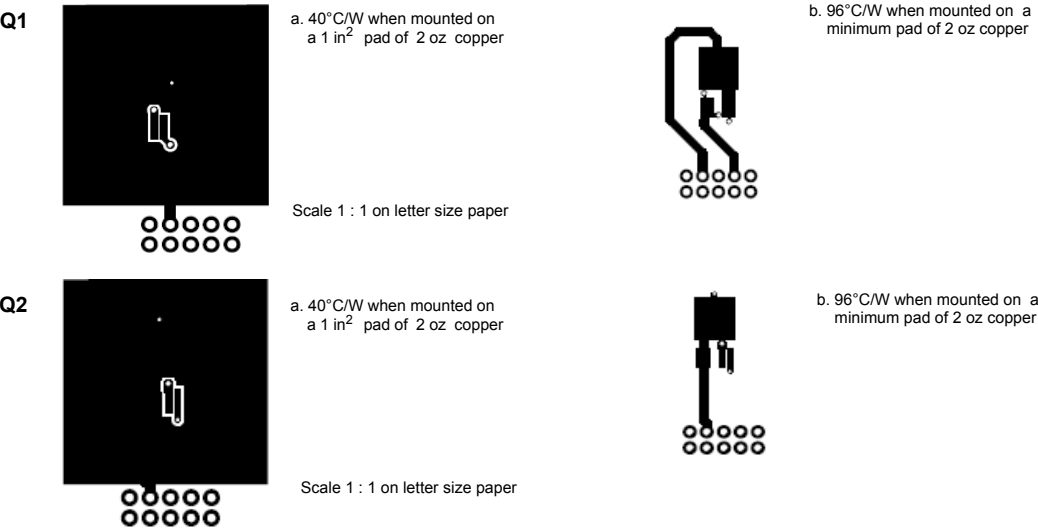
| | | | | | | | |
|--------------|-------------------------------|---|----------|--|------------|----------|----|
| $t_{d(on)}$ | Turn-On Delay Time | Q1 | Q1 Q2 | | 7 7 | 14 14 | ns |
| t_r | Rise Time | $V_{DD} = 20\text{V}$, $I_D = 9.0\text{A}$, $V_{GS} = 10\text{V}$, $R_{GEN} = 6\Omega$ | Q1 Q2 | | 13 3 | 24 10 | |
| $t_{d(off)}$ | Turn-Off Delay Time | Q2 | Q1 Q2 | | 17 20 | 31 36 | ns |
| t_f | Fall Time | $V_{DD} = -20\text{V}$, $I_D = -6.5\text{A}$, $V_{GS} = -10\text{V}$, $R_{GEN} = 6\Omega$ | Q1 Q2 | | 6 3 | 12 10 | |
| $Q_{g(TOT)}$ | Total Gate Charge | Q1 | Q1 Q2 | | 14 17 | 20 24 | nC |
| Q_{gs} | Gate to Source Charge | $V_{GS} = 10\text{V}$, $V_{DD} = 20\text{V}$, $I_D = 9.0\text{A}$ | Q1 Q2 | | 2.3 3.0 | | |
| Q_{gd} | Gate to Drain "Miller" Charge | $V_{GS} = -10\text{V}$, $V_{DD} = -20\text{V}$, $I_D = -6.5\text{A}$ | Q1 | | 3.2 | | nC |
| | | | Q2 | | 3.6 | | |

Electrical Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise noted

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---------------------------------------|---|----------|-----|--------------|-------------|-------|
| Drain-Source Diode Characteristics | | | | | | | |
| V_{SD} | Source to Drain Diode Forward Voltage | $V_{GS} = 0\text{V}, I_S = 9.0\text{A}$ (Note 2) $V_{GS} = 0\text{V}, I_S = -6.5\text{A}$ (Note 2) | Q1 Q2 | | 0.87 0.88 | 1.2 -1.2 | V |
| t_{rr} | Reverse Recovery Time | Q1 $I_F = 9.0\text{A}, di/dt = 100\text{A/s}$ | Q1 Q2 | | 25 29 | 38 44 | ns |
| Q_{rr} | Reverse Recovery Charge | Q2 $I_F = -6.5\text{A}, di/dt = 100\text{A/s}$ | Q1 Q2 | | 19 29 | 29 44 | nC |

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

3. Starting $T_J = 25^{\circ}\text{C}$, N-ch: $L = 0.3\text{mH}$, $I_{AS} = 14\text{A}$, $V_{DD} = 40\text{V}$, $V_{GS} = 10\text{V}$; P-ch: $L = 0.3\text{mH}$, $I_{AS} = -15\text{A}$, $V_{DD} = -40\text{V}$, $V_{GS} = -10\text{V}$.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

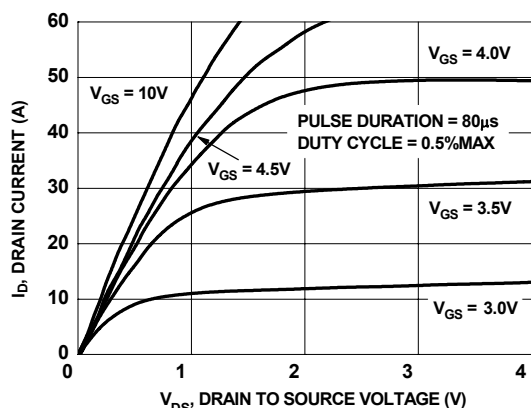


Figure 1. On-Region Characteristics

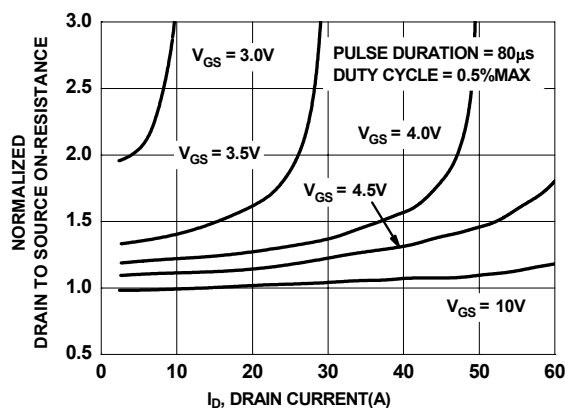


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

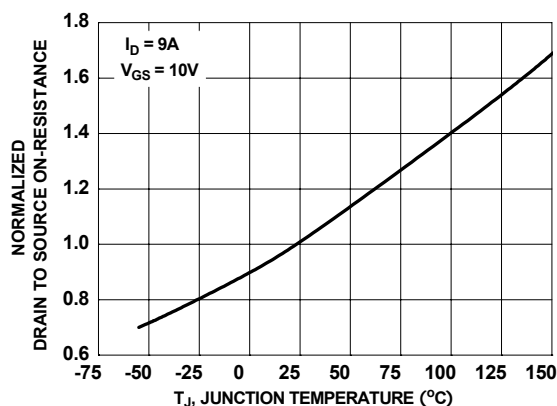


Figure 3. Normalized On-Resistance vs Junction Temperature

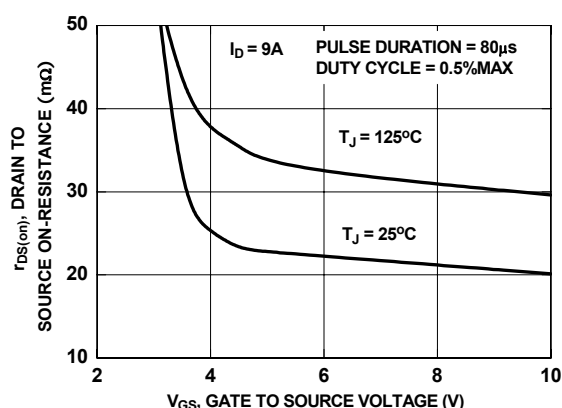


Figure 4. On-Resistance vs Gate to Source Voltage

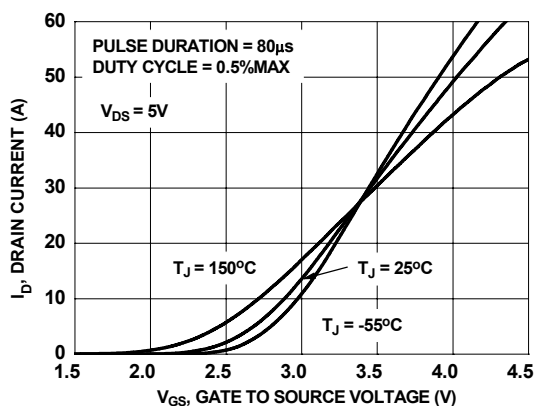


Figure 5. Transfer Characteristics

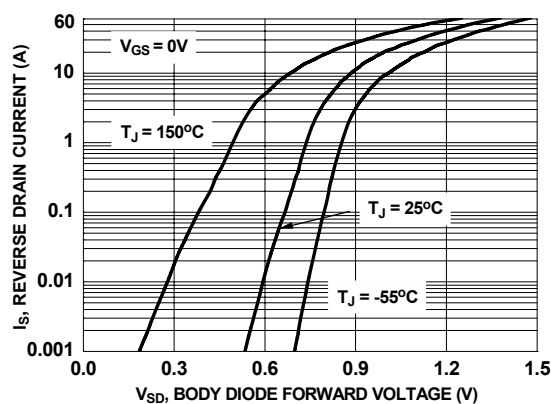


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

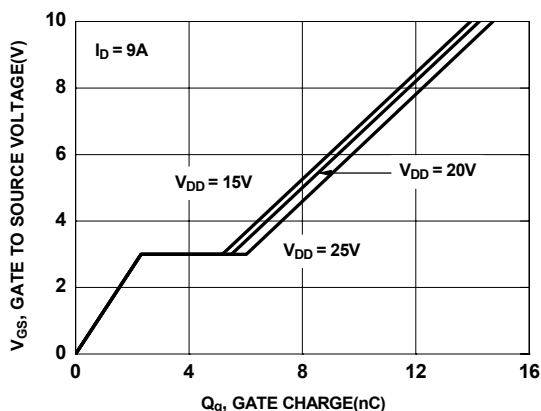


Figure 7. Gate Charge Characteristics

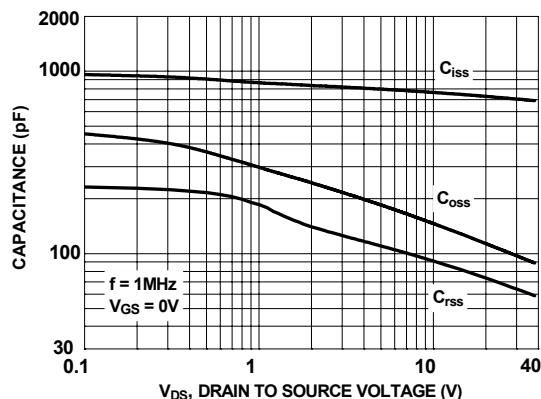


Figure 8. Capacitance vs Drain to Source Voltage

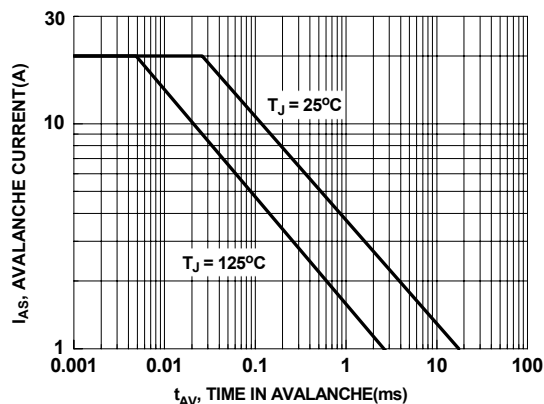


Figure 9. Unclamped Inductive Switching Capability

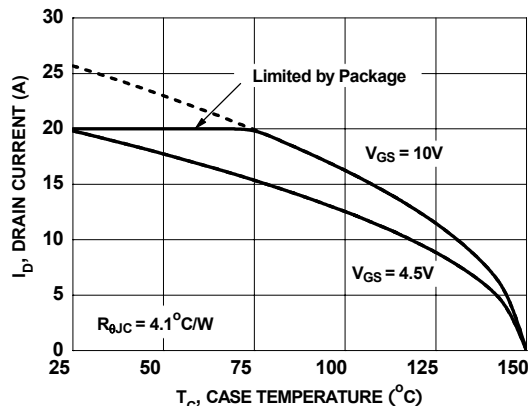


Figure 10. Maximum Continuous Drain Current vs Case Temperature

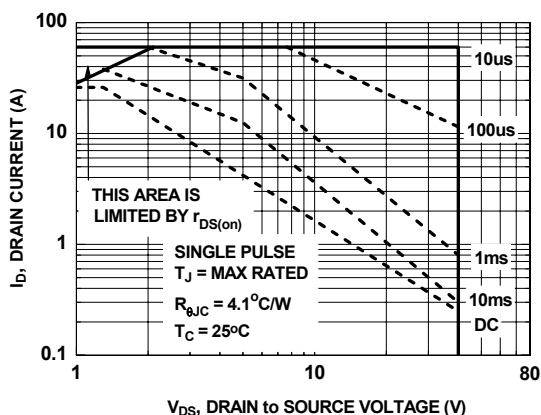


Figure 11. Forward Bias Safe Operating Area

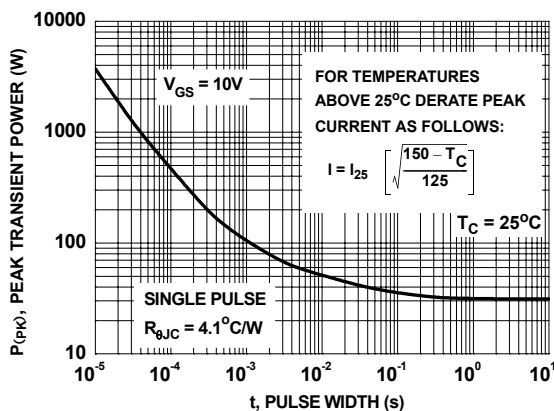


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

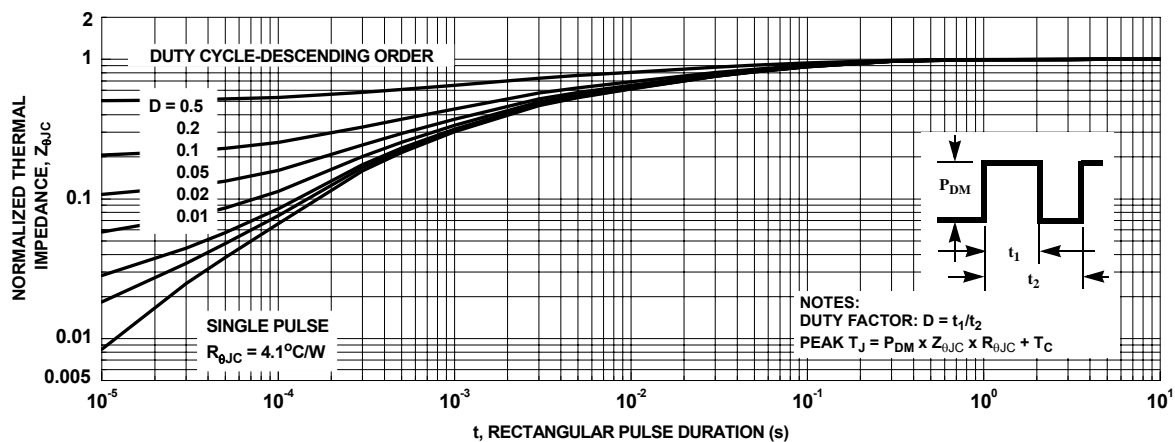


Figure 13. Transient Thermal Response Curve

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

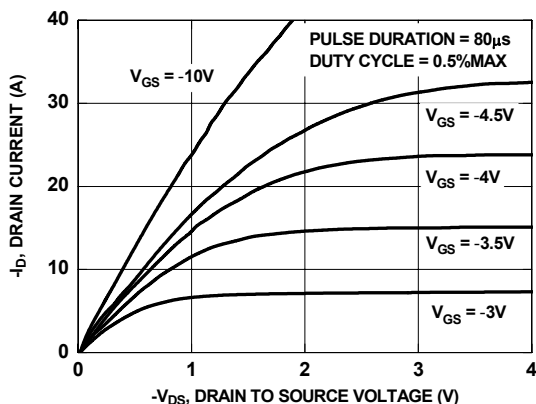


Figure 14. On-Region Characteristics

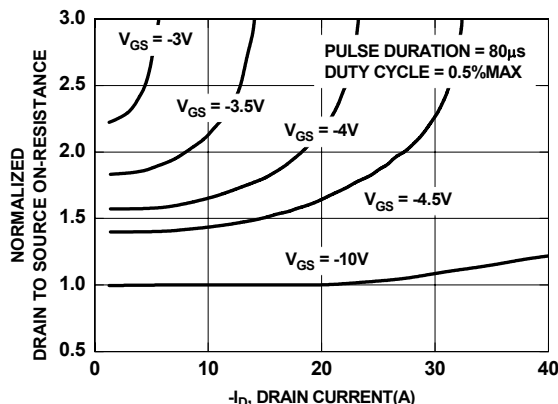


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

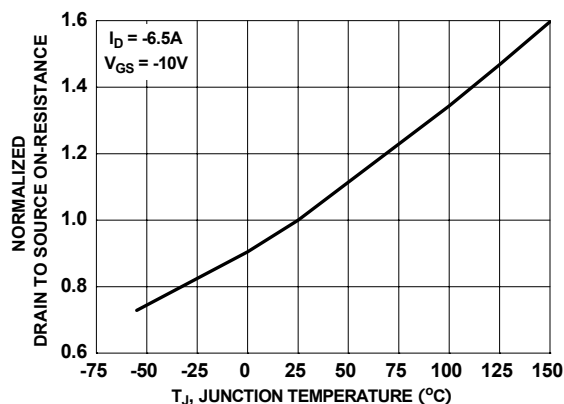


Figure 16. Normalized On-Resistance vs Junction Temperature

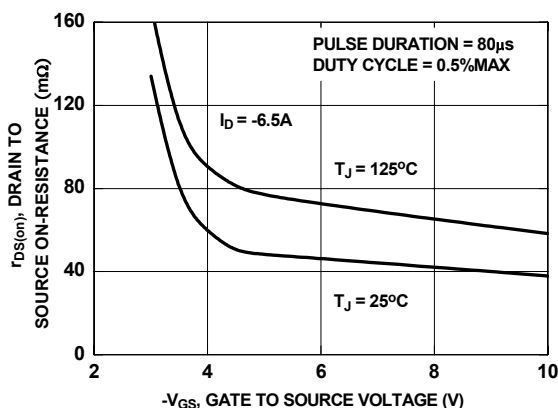


Figure 17. On-Resistance vs Gate to Source Voltage

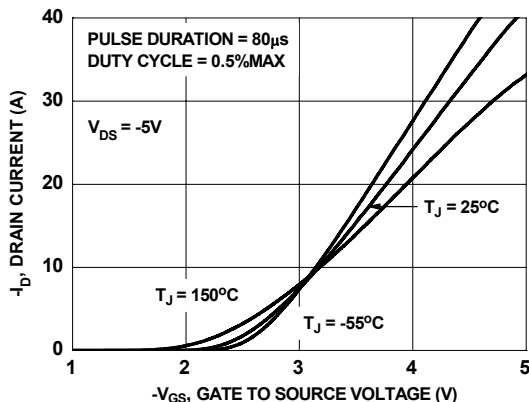


Figure 18. Transfer Characteristics

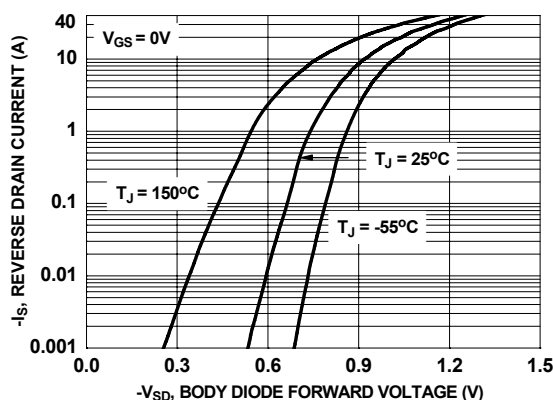


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

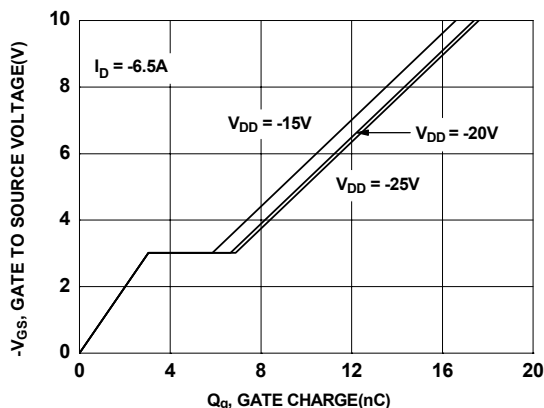


Figure 20. Gate Charge Characteristics

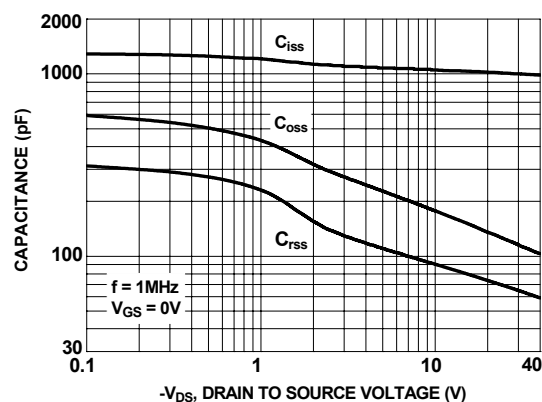


Figure 21. Capacitance vs Drain to Source Voltage

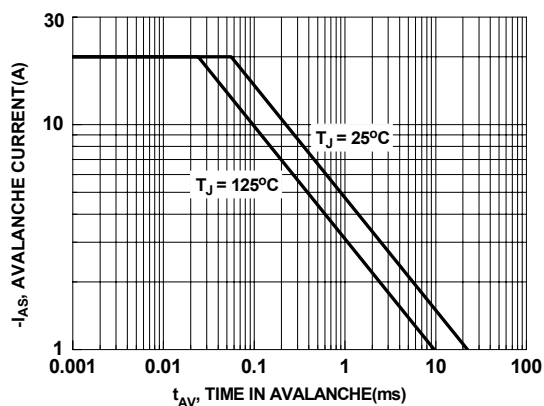


Figure 22. Unclamped Inductive Switching Capability

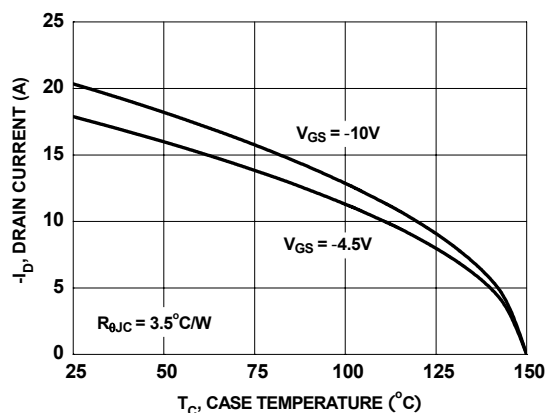


Figure 23. Maximum Continuous Drain Current vs Case Temperature

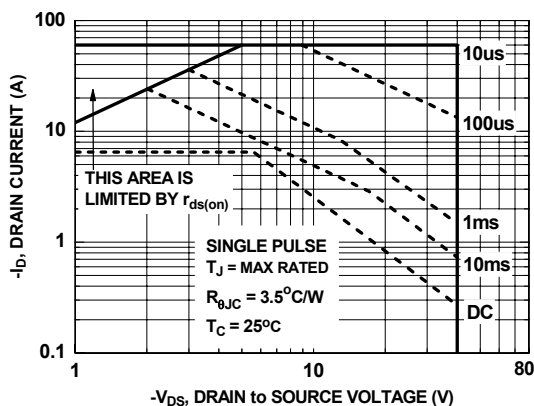


Figure 24. Forward Bias Safe Operating Area

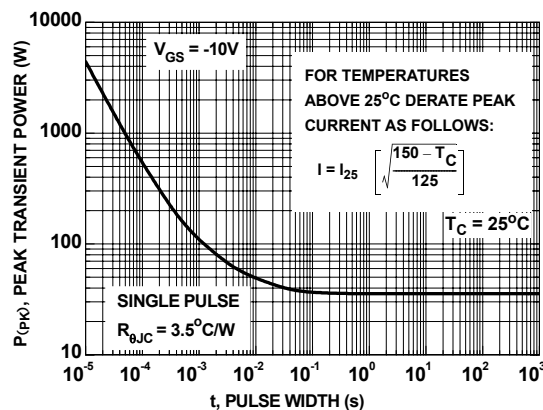
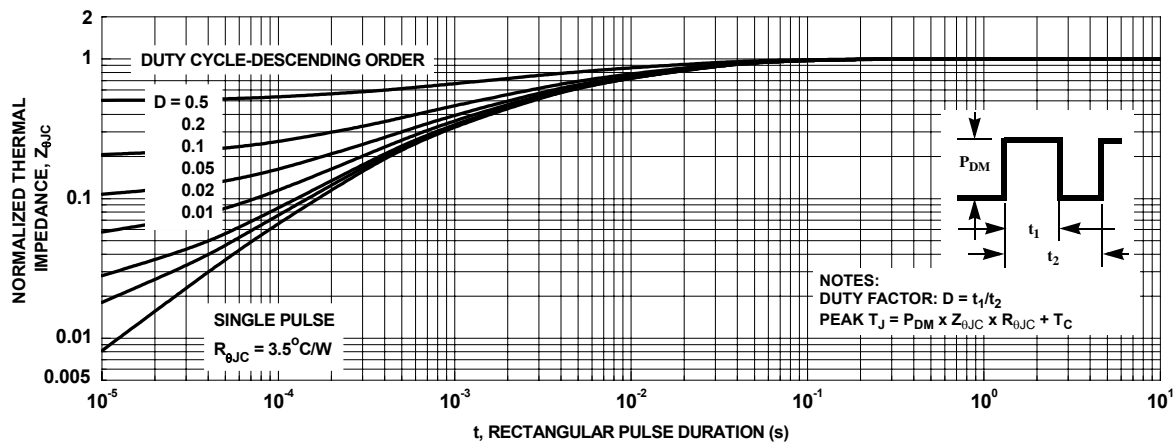
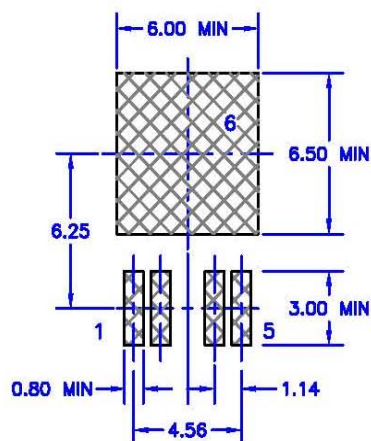


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted





SEE NOTE D

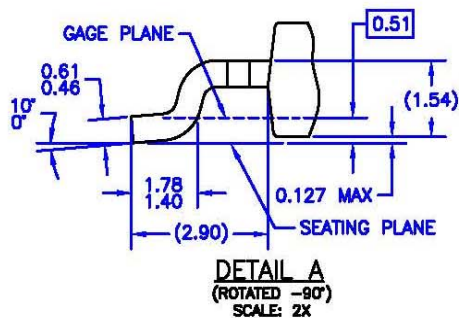
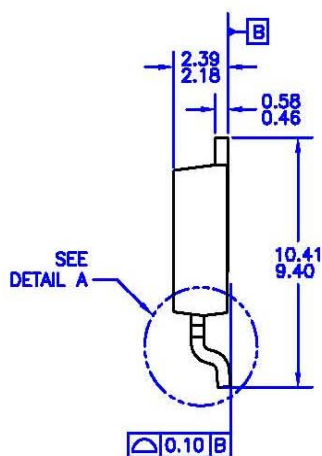
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MIN 5.21

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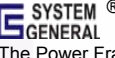
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PRODUCT STATUS DEFINITIONS

Definition of Terms

| Datasheet Identification | Product Status | Definition |
|--------------------------|-----------------------|---|
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