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June 2014

# FQP3N80C / FQPF3N80C

## N-Channel QFET<sup>®</sup> MOSFET

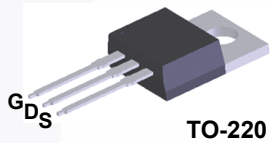
800 V, 3.0 A, 4.8 Ω

### Features

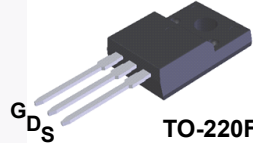
- 3.0 A, 800 V,  $R_{DS(on)} = 4.8 \Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 1.5 \text{ A}$
- Low Gate Charge (Typ. 13 nC)
- Low  $C_{rss}$  (Typ. 5.5 pF)
- 100% Avalanche Tested

### Description

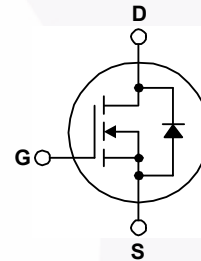
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.



TO-220



TO-220F



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQP3N80C	FQPF3N80C	Unit
$V_{DSS}$	Drain to Source Voltage	800		V
$I_D$	Drain Current	-Continuous ( $T_C = 25^\circ\text{C}$ )	3	3 *
		-Continuous ( $T_C = 100^\circ\text{C}$ )	1.9	1.9 *
$I_{DM}$	Drain Current - Pulsed (Note 1)	12	12 *	A
$V_{GSS}$	Gate to Source Voltage	$\pm 30$		V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	320		mJ
$I_{AR}$	Avalanche Current (Note 1)	3		A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	10.7		mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	4.5		V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	107	39	W
		0.85	0.31	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300		$^\circ\text{C}$

\*Drain current limited by maximum junction temperature.

### Thermal Characteristics

Symbol	Parameter	FQP3N80C	FQPF3N80C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	1.17	3.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	62.5	$^\circ\text{C/W}$

FQP3N80C / FQPF3N80C — N-Channel QFET<sup>®</sup> MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP3N80C	FQP3N80C	TO-220	Tube	Tube	N/A	50 units
FQPF3N80C	FQPF3N80C	TO-220F	Tube	Tube	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	800	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	1	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	$\mu\text{A}$
		$V_{DS} = 640\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}$	--	4.0	4.8	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 1.5\text{ A}$	--	3	--	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	543	705	pF
$C_{oss}$	Output Capacitance		--	54	70	pF
$C_{rss}$	Reverse Transfer Capacitance		--	5.5	7.5	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 400\text{ V}, I_D = 3\text{ A}, R_G = 25\ \Omega$	--	15	40	ns
$t_r$	Turn-On Rise Time		--	43.5	95	ns
$t_{d(off)}$	Turn-Off Delay Time		--	22.5	55	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	32	75
$Q_g$	Total Gate Charge	$V_{DS} = 640\text{ V}, I_D = 3\text{ A}, V_{GS} = 10\text{ V}$	--	13	16.5	nC
$Q_{gs}$	Gate-Source Charge		--	3.4	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	5.8	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		--	--	3.0	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	12	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 3.0\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 3.0\text{ A}, di_F / dt = 100\text{ A}/\mu\text{s}$	--	642	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	4.0	--	$\mu\text{C}$

### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2.  $L = 67\text{ mH}, I_{AS} = 3.0\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 3\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

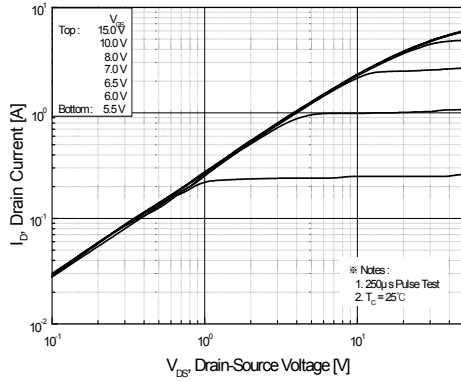


Figure 1. On-Region Characteristics

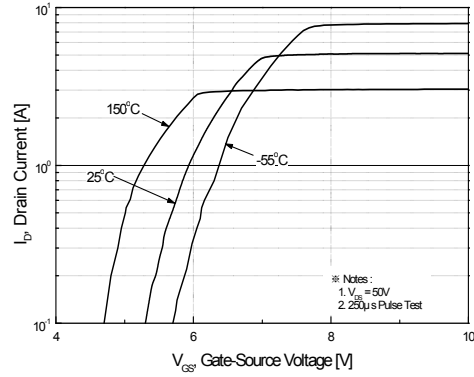


Figure 2. Transfer Characteristics

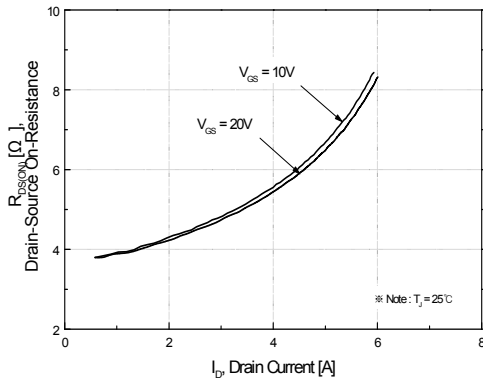


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

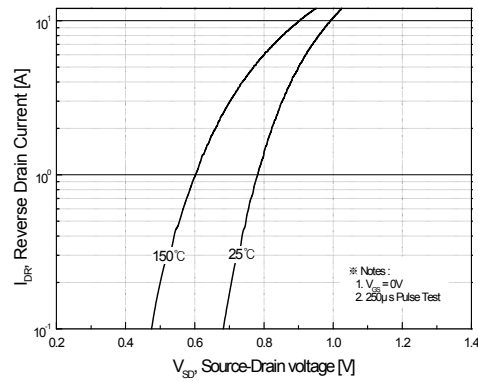


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

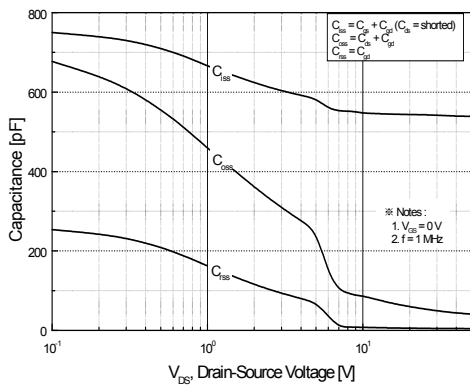


Figure 5. Capacitance Characteristics

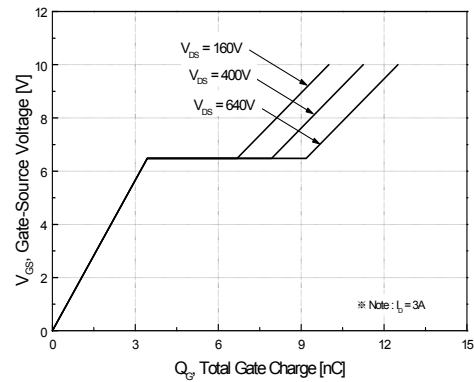


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

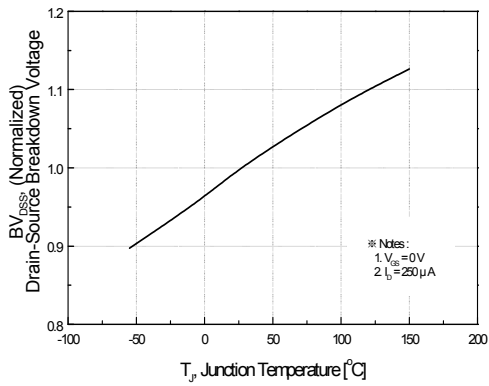


Figure 7. Breakdown Voltage Variation vs Temperature

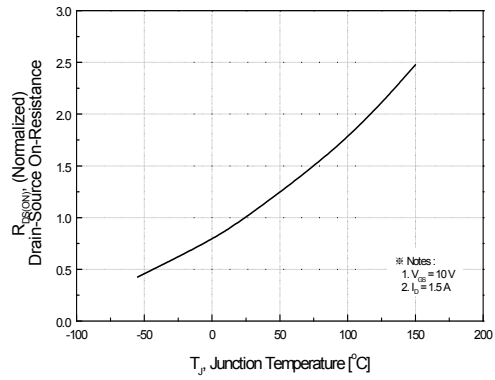


Figure 8. On-Resistance Variation vs Temperature

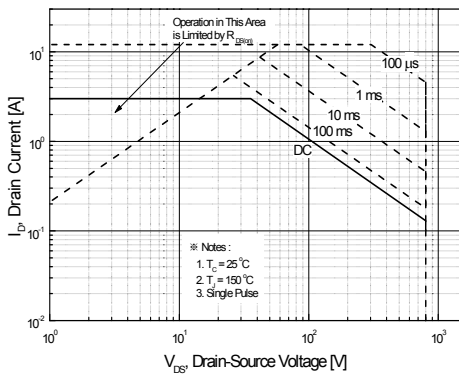


Figure 9-1. Maximum Safe Operating Area for FQP3N80C

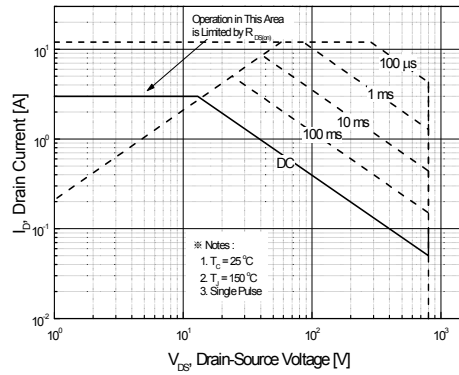


Figure 9-2. Maximum Safe Operating Area for FQPF3N80C

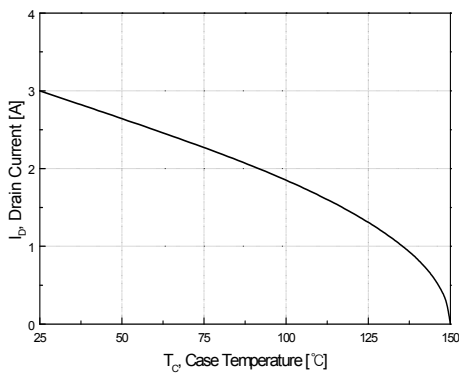


Figure 10. Maximum Drain Current vs Case Temperature

Typical Characteristics (Continued)

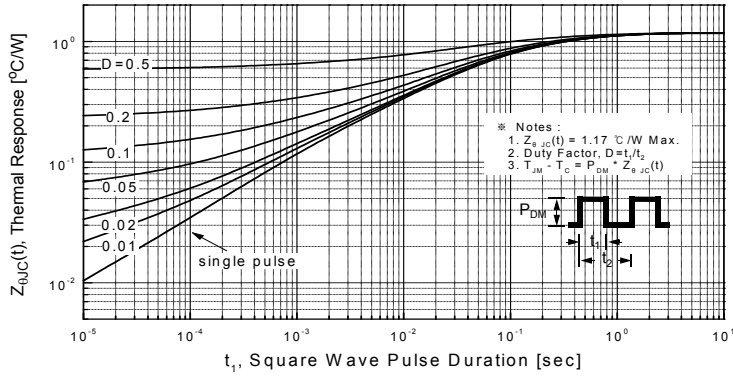


Figure 11-1. Transient Thermal Response Curve for FQP3N80C

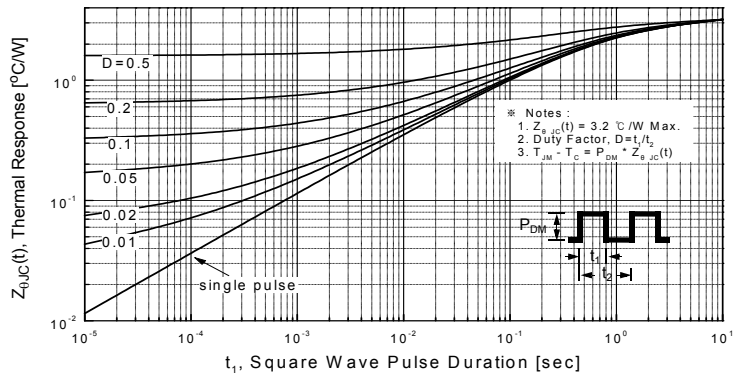
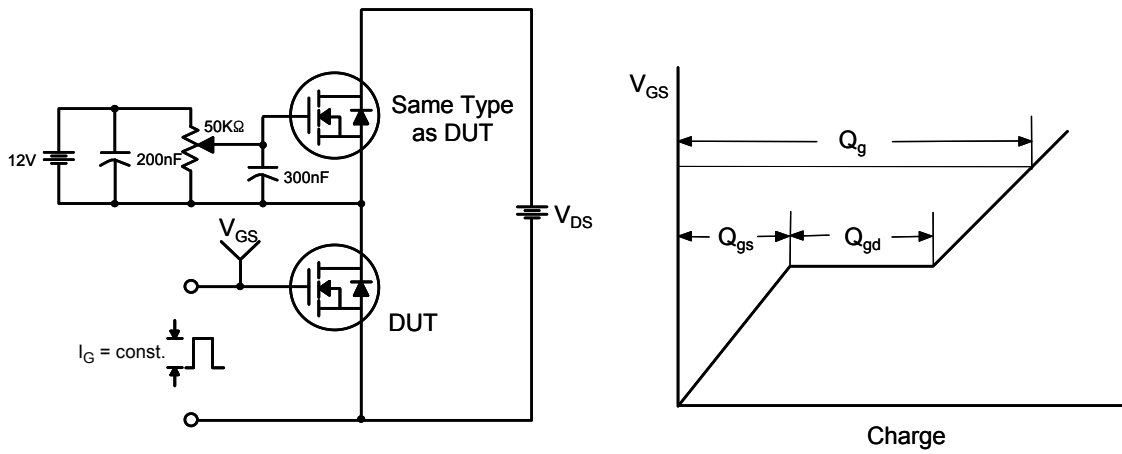
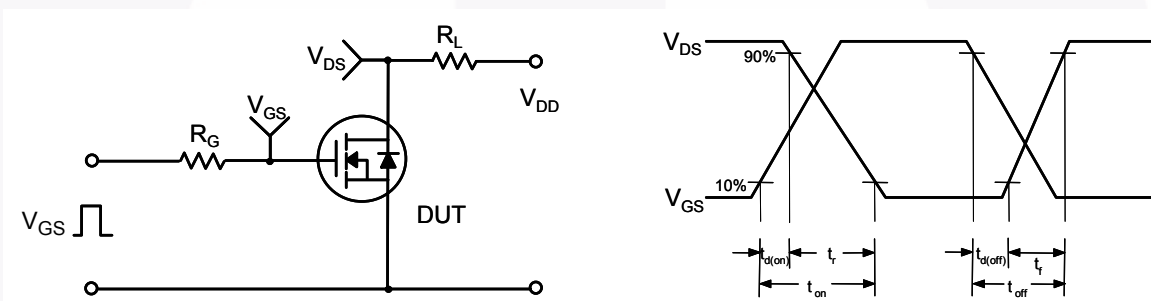


Figure 11-2. Transient Thermal Response Curve for FQPF3N80C

**Figure 12. Gate Charge Test Circuit & Waveform**



**Figure 13. Resistive Switching Test Circuit & Waveforms**



**Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms**

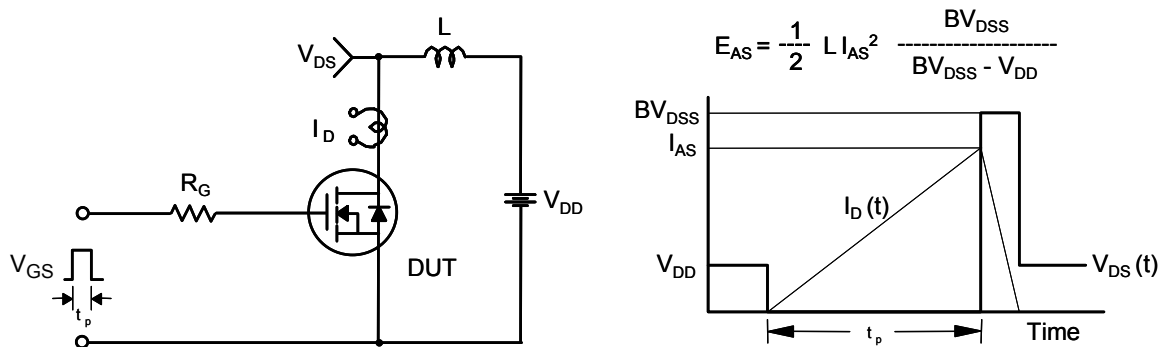
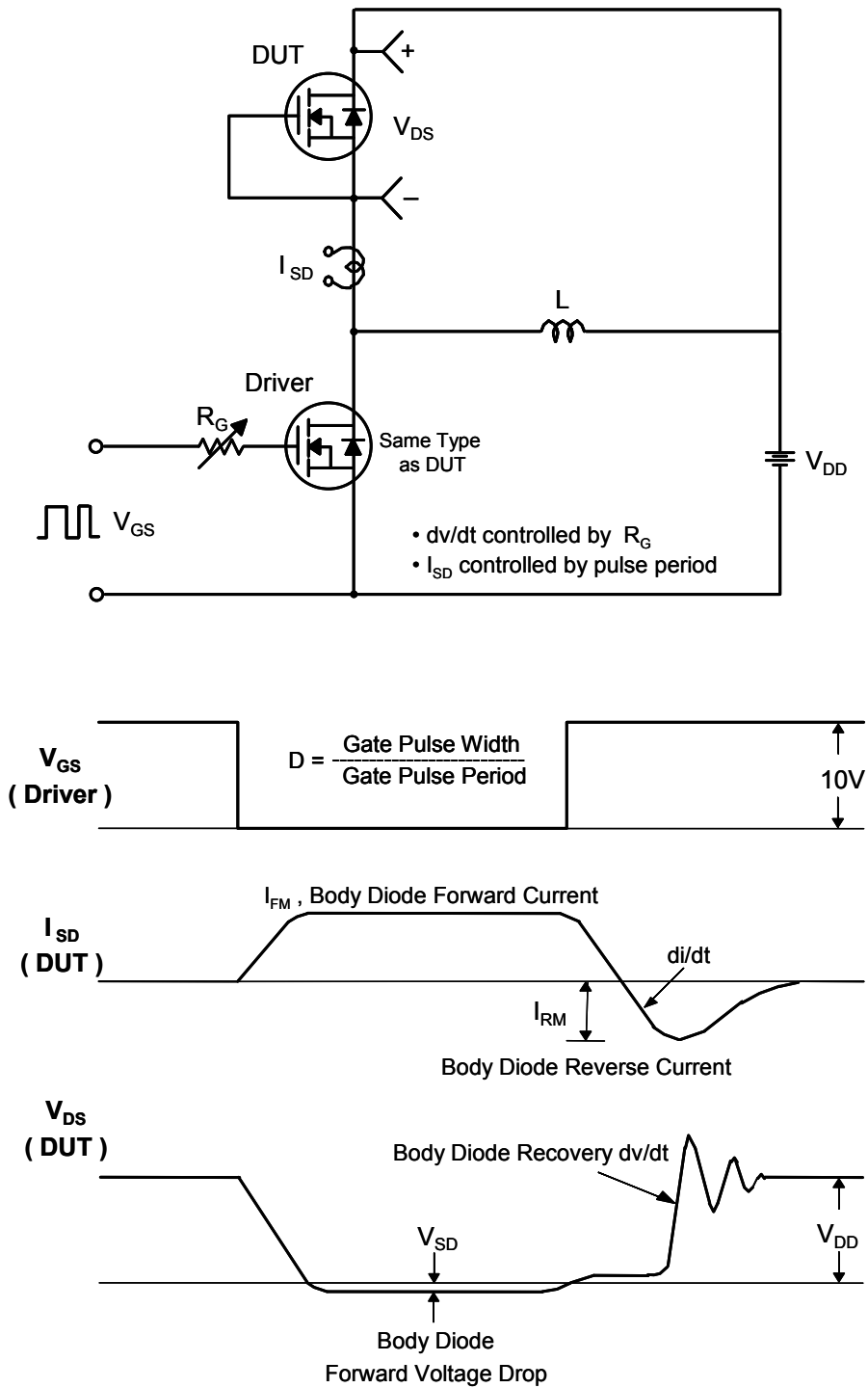
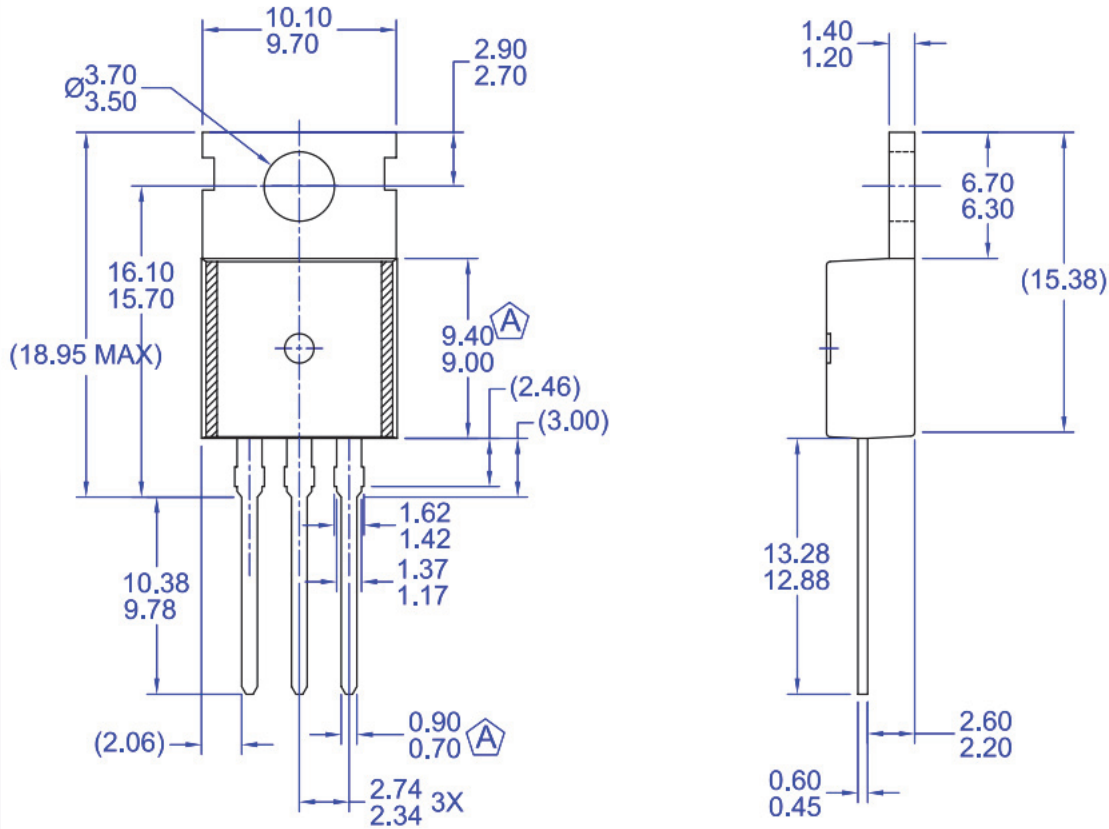


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





## Mechanical Dimensions



### NOTES:

- A) CONFORMS TO JEDEC TO-220 VARIATION AB EXCEPT WHERE NOTED
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

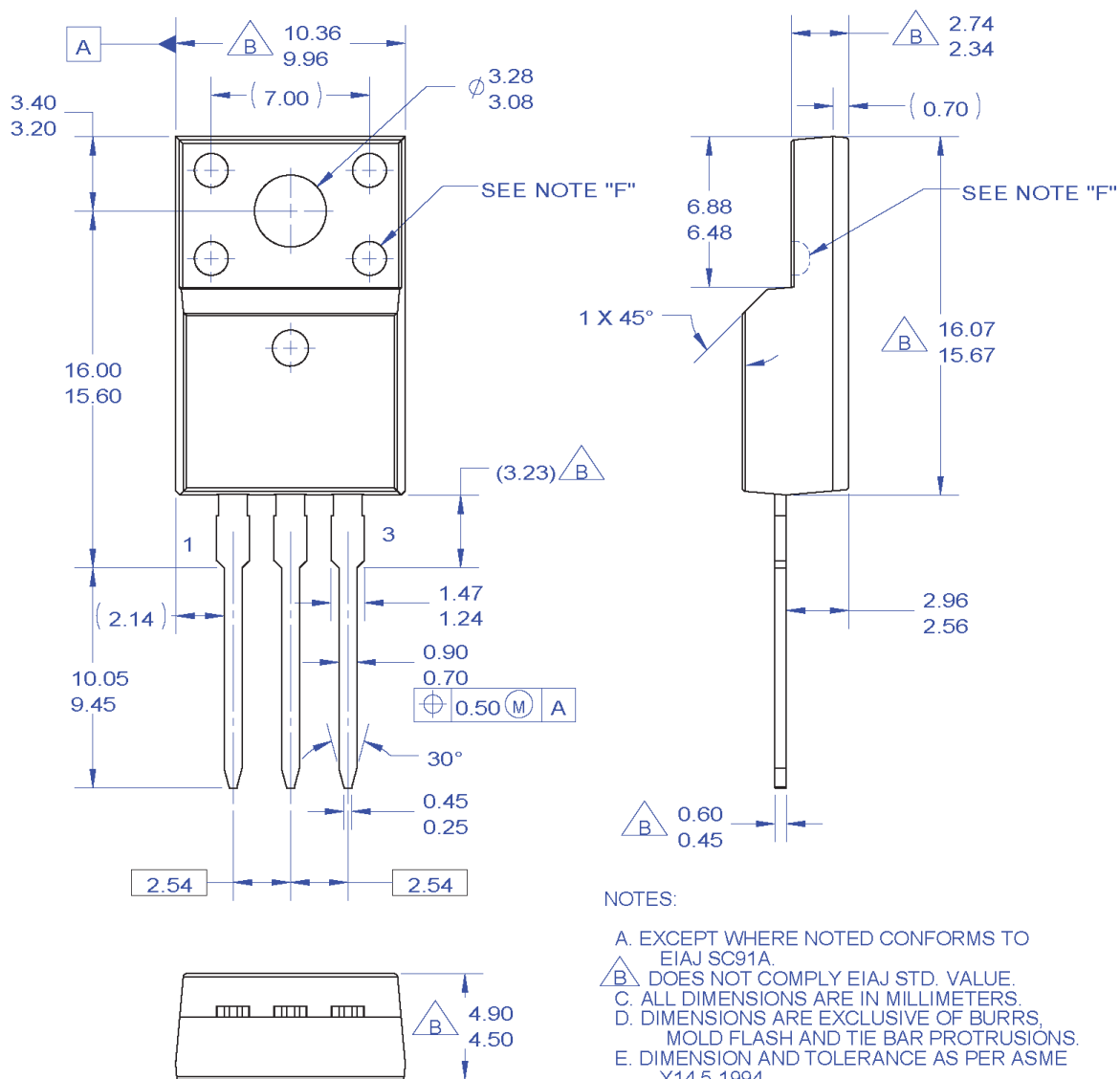
**Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB**

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### Mechanical Dimensions



#### NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
- B. DOES NOT COMPLY EIAJ STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
- F. OPTION 1 - WITH SUPPORT PIN HOLE.  
OPTION 2 - NO SUPPORT PIN HOLE.
- G. DRAWING FILE NAME: TO220M03REV3

**Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead**

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