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# FSB50450T

## Smart Power Module (SPM®)

### Features

- 500V 3.0A 3-phase FRFET inverter including high voltage integrated circuit (HVIC)
- 3 divided negative dc-link terminals for inverter current sensing applications
- HVIC for gate driving and undervoltage protection
- 3/5V CMOS/TTL compatible, active-high interface
- Optimized for low electromagnetic interference
- Isolation voltage rating of 1500Vrms for 1min.
- Extended VB pin for PCB isolation

### General Description

FSB50450T is a tiny smart power module (SPM®) based on FRFET technology as a compact inverter solution for small power motor drive applications such as fan motors and water suppliers. It is composed of 6 fast-recovery MOSFET (FRFET), and 3 half-bridge HVICs for FRFET gate driving. FSB50450T provides low electromagnetic interference (EMI) characteristics with optimized switching speed. Moreover, since it employs FRFET as a power switch, it has much better ruggedness and larger safe operation area (SOA) than that of an IGBT-based power module or one-chip solution. The package is optimized for the thermal performance and compactness for the use in the built-in motor application and any other application where the assembly space is concerned. FSB50450T is the most solution for the compact inverter providing the energy efficiency, compactness, and low electromagnetic interference.

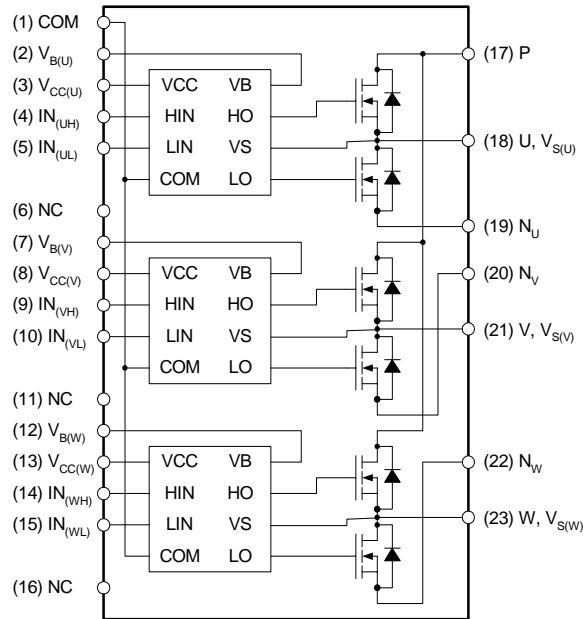


### Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Units
$V_{PN}$	DC Link Input Voltage, Drain-source Voltage of each FRFET		500	V
$I_{D25}$	Each FRFET Drain Current, Continuous	$T_C = 25^\circ\text{C}$	1.5	A
$I_{D80}$	Each FRFET Drain Current, Continuous	$T_C = 100^\circ\text{C}$	1.0	A
$I_{DP}$	Each FRFET Drain Current, Peak	$T_C = 25^\circ\text{C}$ , $PW < 100\mu\text{s}$	3.0	A
$P_D$	Maximum Power Dissipation	$T_C = 25^\circ\text{C}$ , Each FRFET	10	W
$V_{CC}$	Control Supply Voltage	Applied between $V_{CC}$ and COM	20	V
$V_{BS}$	High-side Bias Voltage	Applied between $V_{B(U)}-U$ , $V_{B(V)}-V$ , $V_{B(W)}-W$	20	V
$V_{IN}$	Input Signal Voltage	Applied between IN and COM	-0.3 ~ $V_{CC}+0.3$	V
$T_J$	Operating Junction Temperature		-20 ~ 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature		-50 ~ 150	$^\circ\text{C}$
$R_{\theta JC}$	Junction to Case Thermal Resistance	Each FRFET under inverter operating condition (Note 1)	8.9	$^\circ\text{C/W}$
$V_{ISO}$	Isolation Voltage	60Hz, Sinusoidal, 1 minute, Connection pins to heatsink	1500	$V_{rms}$

## Pin Descriptions

Pin Number	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U Phase High Side FRFET Driving
3	$V_{CC(U)}$	Bias Voltage for U Phase IC and Low Side FRFET Driving
4	$IN_{(UH)}$	Signal Input for U Phase High-side
5	$IN_{(UL)}$	Signal Input for U Phase Low-side
6	NC	No Connection
7	$V_{B(V)}$	Bias Voltage for V Phase High Side FRFET Driving
8	$V_{CC(V)}$	Bias Voltage for V Phase IC and Low Side FRFET Driving
9	$IN_{(VH)}$	Signal Input for V Phase High-side
10	$IN_{(VL)}$	Signal Input for V Phase Low-side
11	NC	No Connection
12	$V_{B(W)}$	Bias Voltage for W Phase High Side FRFET Driving
13	$V_{CC(W)}$	Bias Voltage for W Phase IC and Low Side FRFET Driving
14	$IN_{(WH)}$	Signal Input for W Phase High-side
15	$IN_{(WL)}$	Signal Input for W Phase Low-side
16	NC	No Connection
17	P	Positive DC-Link Input
18	U, $V_{S(U)}$	Output for U Phase & Bias Voltage Ground for High Side FRFET Driving
19	$N_U$	Negative DC-Link Input for U Phase
20	$N_V$	Negative DC-Link Input for V Phase
21	V, $V_{S(V)}$	Output for V Phase & Bias Voltage Ground for High Side FRFET Driving
22	$N_W$	Negative DC-Link Input for W Phase
23	W, $V_{S(W)}$	Output for W Phase & Bias Voltage Ground for High Side FRFET Driving



**Note:**

Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside SPM®. External connections should be made as indicated in Figure 2 and 5.

**Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)**

**Electrical Characteristics** ( $T_J = 25^\circ\text{C}$ ,  $V_{CC}=V_{BS}=15\text{V}$  Unless Otherwise Specified)**Inverter Part** (Each FRFET Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{IN}=0\text{V}$ , $I_D = 250\mu\text{A}$ (Note 2)	500	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.53	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{IN}=0\text{V}$ , $V_{DS} = 500\text{V}$	-	-	250	$\mu\text{A}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{CC} = V_{BS} = 15\text{V}$ , $V_{IN} = 5\text{V}$ , $I_D = 1.0\text{A}$	-	1.9	2.4	$\Omega$
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{CC} = V_{BS} = 15\text{V}$ , $V_{IN} = 0\text{V}$ , $I_D = -1.0\text{A}$	-	-	1.2	V
$t_{ON}$	Switching Times	$V_{PN} = 300\text{V}$ , $V_{CC} = V_{BS} = 15\text{V}$ , $I_D = 1.0\text{A}$ $V_{IN} = 0\text{V} \leftrightarrow 5\text{V}$ Inductive load $L=3\text{mH}$ High- and low-side FRFET switching  (Note 3)	-	1152	-	ns
$t_{OFF}$			-	600	-	ns
$t_{rr}$			-	185	-	ns
$E_{ON}$			-	85	-	$\mu\text{J}$
$E_{OFF}$			-	11	-	$\mu\text{J}$
RBSOA	Reverse-bias Safe Operating Area	$V_{PN} = 400\text{V}$ , $V_{CC} = V_{BS} = 15\text{V}$ , $I_D = I_{DP}$ , $R_{EH} = 0\Omega$ $V_{DS}=BV_{DSS}$ , $T_J = 150^\circ\text{C}$ High- and low-side FRFET switching (Note 4)	Full Square			

**Control Part** (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{QCC}$	Quiescent $V_{CC}$ Current	$V_{CC}=15\text{V}$ , $V_{IN}=0\text{V}$ Applied between $V_{CC}$ and COM	-	-	160	$\mu\text{A}$
$I_{QBS}$	Quiescent $V_{BS}$ Current	$V_{BS}=15\text{V}$ , $V_{IN}=0\text{V}$ Applied between $V_{B(U)}-U$ , $V_{B(V)}-V$ , $V_{B(W)}-W$	-	-	100	$\mu\text{A}$
$UV_{CCD}$	Low-side Undervoltage Protection (Figure 6)	$V_{CC}$ Undervoltage Protection Detection Level	7.4	8.0	9.4	V
$UV_{CCR}$		$V_{CC}$ Undervoltage Protection Reset Level	8.0	8.9	9.8	V
$UV_{BSD}$	High-side Undervoltage Protection (Figure 7)	$V_{BS}$ Undervoltage Protection Detection Level	7.4	8.0	9.4	V
$UV_{BSR}$		$V_{BS}$ Undervoltage Protection Reset Level	8.0	8.9	9.8	V
$V_{IH}$	ON Threshold Voltage	Logic High Level	3.0	-	-	V
$V_{IL}$	OFF Threshold Voltage	Logic Low Level				
$I_{IH}$	Input Bias Current	$V_{IN} = 5\text{V}$	-	10	20	$\mu\text{A}$
$I_{IL}$		$V_{IN} = 0\text{V}$	-	-	2	$\mu\text{A}$

**Note:**

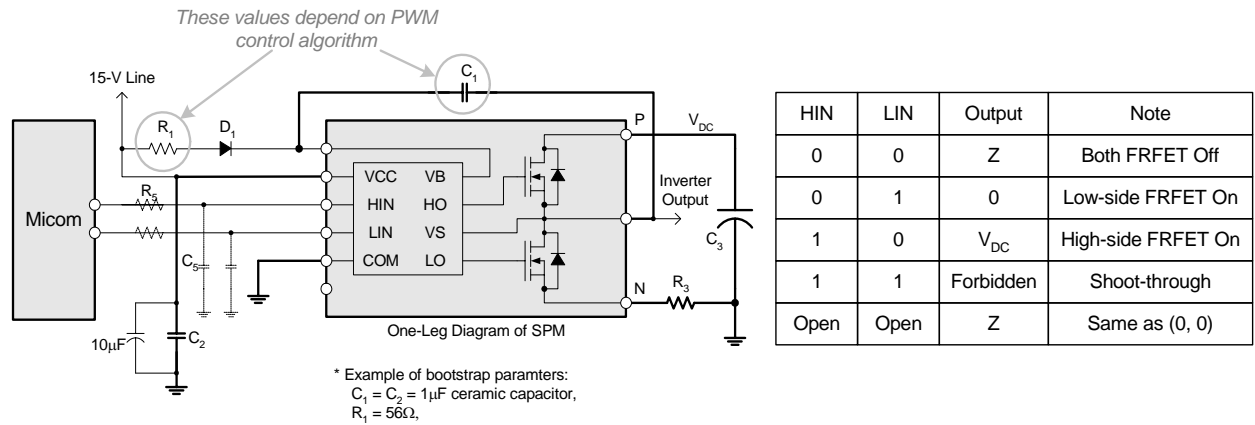
- For the measurement point of case temperature  $T_C$ , please refer to Figure 3 in page 4.
- $BV_{DSS}$  is the absolute maximum voltage rating between drain and source terminal of each FRFET inside SPM®.  $V_{PN}$  should be sufficiently less than this value considering the effect of the stray inductance so that  $V_{DS}$  should not exceed  $BV_{DSS}$  in any case.
- $t_{ON}$  and  $t_{OFF}$  include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 4 for the switching time definition with the switching test circuit of Figure 5.
- The peak current and voltage of each FRFET during the switching operation should be included in the safe operating area (SOA). Please see Figure 5 for the RBSOA test circuit that is same as the switching test circuit.

**Package Marking & Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FSB50450T	FSB50450T	SPM23AC	—	—	15

## Recommended Operating Conditions

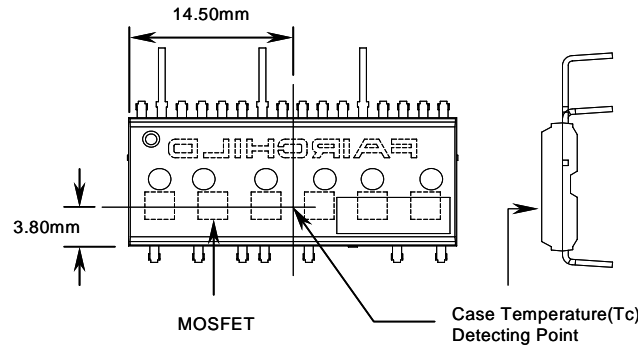
Symbol	Parameter	Conditions	Value			Units
			Min.	Typ.	Max.	
$V_{PN}$	Supply Voltage	Applied between P and N	-	300	400	V
$V_{CC}$	Control Supply Voltage	Applied between $V_{CC}$ and COM	12	15	16.5	V
$V_{BS}$	High-side Bias Voltage	Applied between $V_B$ and output(U, V, W)	12	15	16.5	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied between IN and COM	3.0	-	$V_{CC}$	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	-	0.6	V
$t_{dead}$	Blanking Time for Preventing Arm-short	$V_{CC}=V_{BS}=12 \sim 16.5V$ , $T_J \leq 150^\circ C$	1.0	-	-	$\mu s$
$f_{PWM}$	PWM Switching Frequency	$T_J \leq 150^\circ C$	-	15	-	kHz
$T_C$	Case Temperature	$T_J \leq 150^\circ C$	-20	-	125	$^\circ C$



### Note:

- (1) It is recommended the bootstrap diode  $D_1$  to have soft and fast recovery characteristics with 600-V rating
- (2) Parameters for bootstrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
- (3) RC coupling ( $R_5$  and  $C_5$ ) at each input (indicated as dotted lines) may be used to prevent improper input signal due to surge noise. Signal input of SPM® is compatible with standard CMOS or LSTTL outputs.
- (4) Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge voltage. Bypass capacitors such as  $C_1$ ,  $C_2$  and  $C_3$  should have good high-frequency characteristics to absorb high-frequency ripple current.

**Figure 2. Recommended CPU Interface and Bootstrap Circuit with Parameters**



### Note:

Attach the thermocouple on top of the heatsink-side of SPM® (between SPM® and heatsink if applied) to get the correct temperature measurement.

**Figure 3. Case Temperature Measurement**

The diagram illustrates a one-leg power MOSFET driver circuit for a Switched Power Module (SPM). The SPM block contains two MOSFETs (top and bottom) and two diodes (anti-parallel). The top MOSFET's gate is driven by a pulse-width modulated (PWM) signal through a resistor  $R_{BS}$  and a diode connected to  $V_{CC}$ . The bottom MOSFET's gate is driven by an inverted PWM signal through a resistor  $R_{BS}$  and a diode connected to ground. The drain of the top MOSFET is connected to a load inductor  $L$  and a capacitor  $C_{BS}$  in parallel, which is then connected to the positive DC rail  $V_{DC}$ . The source of the top MOSFET is connected to the negative DC rail  $V_{DC}$ . The drain of the bottom MOSFET is connected to the negative DC rail  $V_{DC}$ . The source of the bottom MOSFET is connected to the positive DC rail  $V_{DC}$ . The output current  $I_b$  flows from the positive DC rail  $V_{DC}$  through the load inductor  $L$  and the capacitor  $C_{BS}$  to the negative DC rail  $V_{DC}$ . The drain-source voltage  $V_{DS}$  is shown across the load inductor  $L$  and the capacitor  $C_{BS}$ . The gate-source voltage  $V_{GS}$  is shown across the gates of the MOSFETs. The gate-drain voltage  $V_{GD}$  is shown across the gates and drains of the MOSFETs. The drain current  $I_D$  is shown flowing into the drain of the top MOSFET. The source current  $I_S$  is shown flowing out of the source of the bottom MOSFET. The output current  $I_b$  is shown flowing out of the positive DC rail  $V_{DC}$  and into the negative DC rail  $V_{DC}$ .

The diagram illustrates the UV Protection Status and its relationship to the Input Signal, Low-side Supply ( $V_{CC}$ ), and MOSFET Current.

- Input Signal:** A square wave signal that is high during the initial and final periods and low during the middle period.
- UV Protection Status:** A signal that transitions from **RESET** to **DETECTION** when the Low-side Supply drops below the  $UV_{CCD}$  threshold. It returns to **RESET** when the Low-side Supply rises above the  $UV_{CCR}$  threshold.
- Low-side Supply,  $V_{CC}$ :** A signal that drops from a high level to a low level during the middle period. The  $UV_{CCD}$  threshold is indicated by a dashed line, and the  $UV_{CCR}$  threshold is indicated by a dashed line.
- MOSFET Current:** A signal showing the current drawn by the MOSFET. It is high during the initial and final periods and drops to zero during the middle period when the UV Protection Status is in the **DETECTION** state.

The diagram illustrates the UV Protection Status logic. The **Input Signal** is a periodic square wave. The **UV Protection Status** is initially in the **RESET** state. When the **High-side Supply,  $V_{BS}$**  begins to fall, the status transitions to **DETECTION** once it reaches the  $UV_{BSD}$  threshold. During the **DETECTION** phase, the **MOSFET Current** is shown as a series of pulses. When  $V_{BS}$  rises above the  $UV_{BSR}$  threshold, the status returns to **RESET**, and the MOSFET current ceases.

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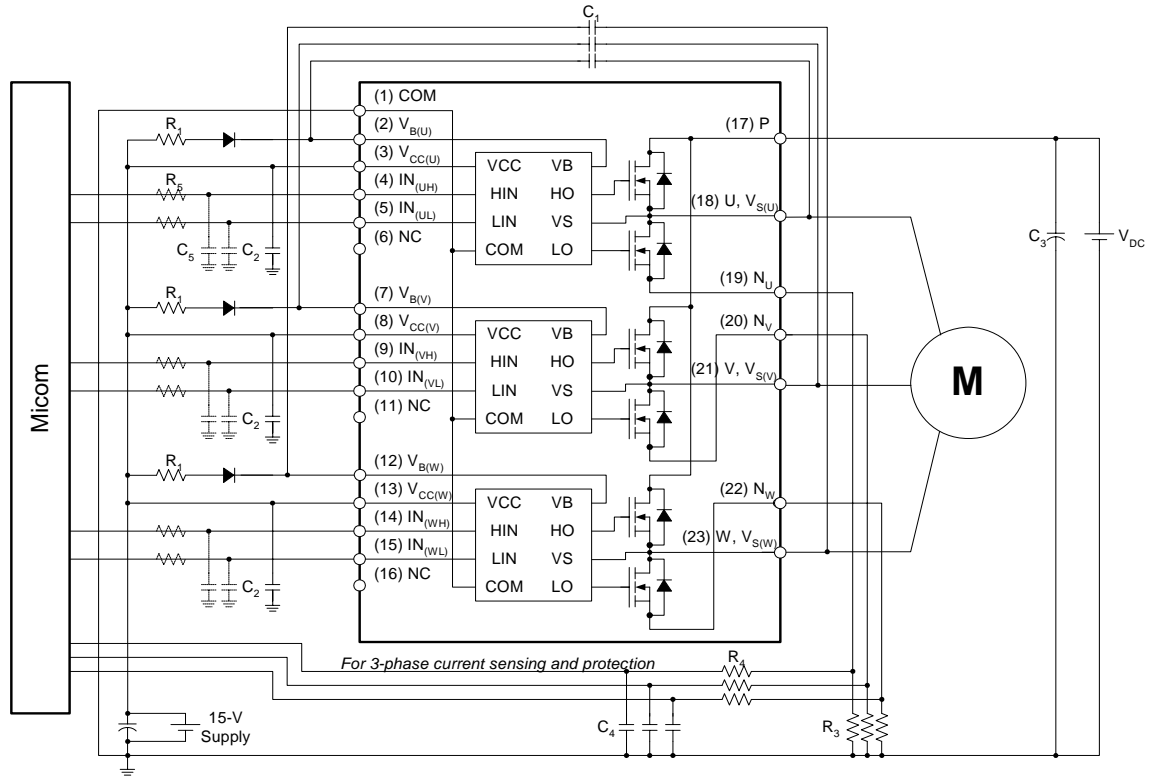
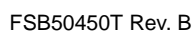


Figure 8. Example of Application Circuit








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