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April 2009

KA7500C SMPS Controller

Features

- Internal Regulator Provides a Stable 5V Reference Supply Trimmed to ±1% Accuracy
- Uncommitted Output TR for 200mA Sink or Source Current
- Output Control for Push-Pull or Single-Ended Operation
- Variable Duty Cycle by Dead-Time Control (Pin 4)
 Complete PWM Control Circuit
- On-Chip Oscillator with Master or Slave Operation
- Internal Circuit Prohibits Double Pulse at Either Output

Description

The KA7500C is used for the control circuit of the pulsewidth modulation switching regulator. The KA7500C consists of 5V reference voltage circuit, two error amplifiers, flip flop, an output control circuit, a PWM comparator, a dead-time comparator, and an oscillator.

This device can be operated in the switching frequency of 1kHz to 300kHz. The precision of voltage reference (V_{REF}) is improved up to ±1% with trimming. This provides a better output voltage regulation. The operating temperature range is -25°C ~ +85°C.



Ordering Information

Part Number	Operating Temperature Range	© Eco Status	Package	Packing Method	
KA7500C			16-Lead Dual Inline Package (DIP)	Tube	
KA7500CD	7500CD -25 to +85°C F		16-Lead Small Outline Package (SOP)	Tube	
KA7500CDTF			10-Lead Small Oddille Package (SOP)	Tape and Reel	

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Block Diagram

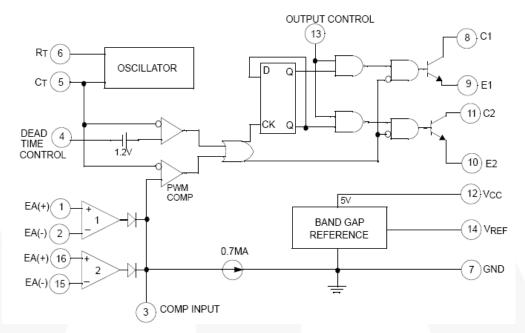
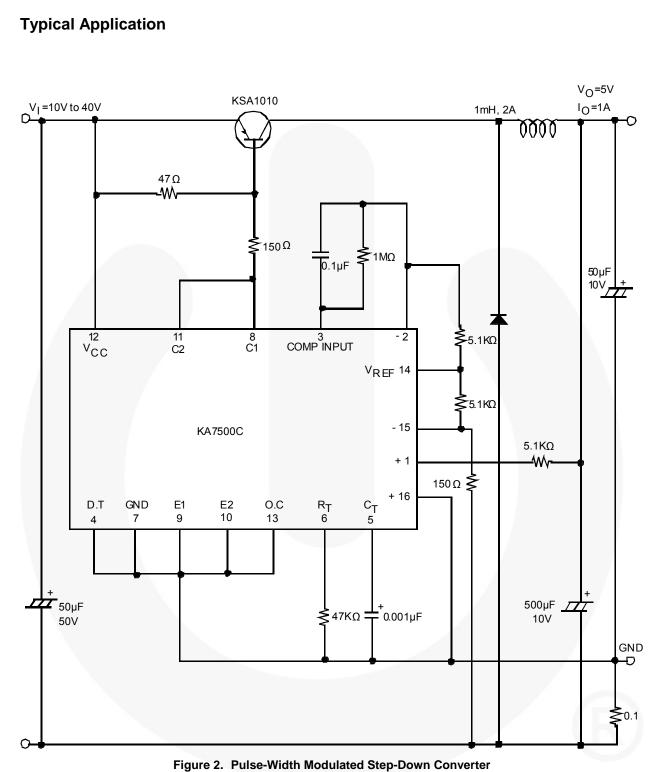


Figure 1. Block Diagram



Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit	
V _{CC}	Supply Voltage			42	V	
V _C	Collector Supply Voltage			42	V	
Io	Output Current			250	mA	
V _{IN}	Amplifier Input Voltage			V _{CC} + 0.3	V	
D	Power Dissipation	KA7500C		1	W	
P_D		KA7500CD		0.9] vv	
T _{OPR}	Operation Temperature Range		-25	+85	°C	
T _{STG}	Storage Temperature Rang		-65	+150	°C	
TJ	Junction Temperature			+125	°C	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Тур.	Max.	Unit
V _{CC}	Power Supply Voltage	7	15	40	V
V_{C1}, V_{C2}	Collector Supply Voltage		30	40	V
I _{C1} , I _{C2}	Collector Output Current (Each Transition)			200	mA
V _{IN}	Amplifier Input Voltage	0.3		V _{CC} - 2.0	V
I _{FB}	Current Into Feedback Terminal			0.3	mA
I _{REF}	Reference Output Terminal			10	mA
R_T	Timing Resistor	1.8	30.0	500.0	KΩ
C _T	Timing Capacitor	0.0047	0.0010	10.0000	μA
fosc	Oscillator Frequency	1	40	200	kHz
V _{IN_PWM}	PWM Input Voltage (Pins 3, 4, and 13)	0.3		5.3	V

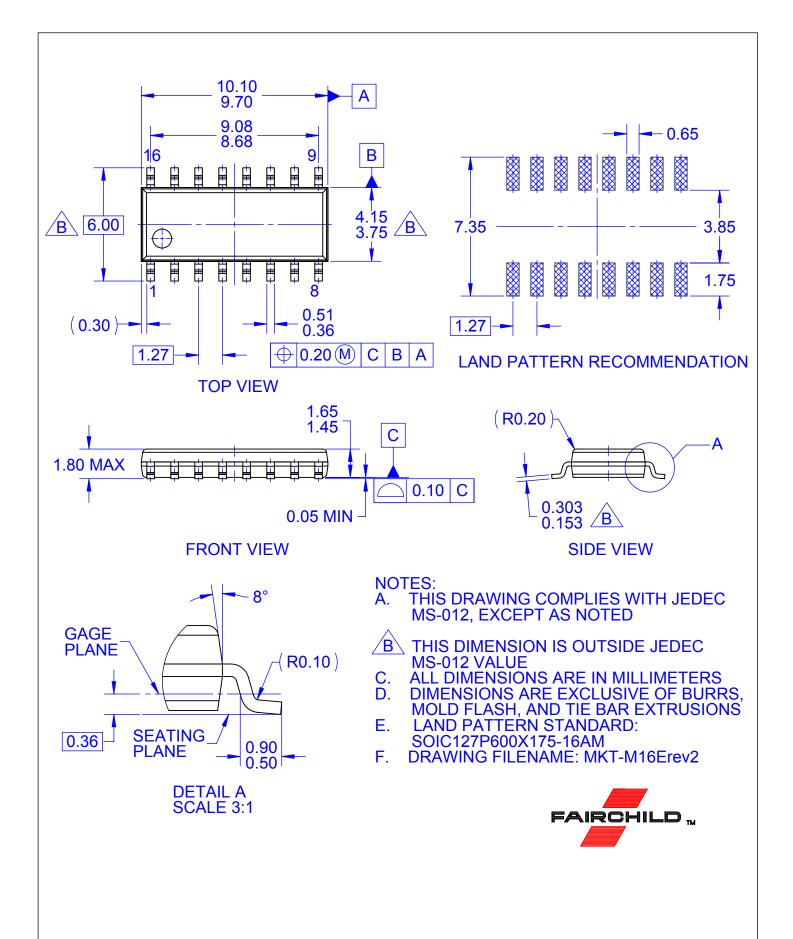
Electrical Characteristics

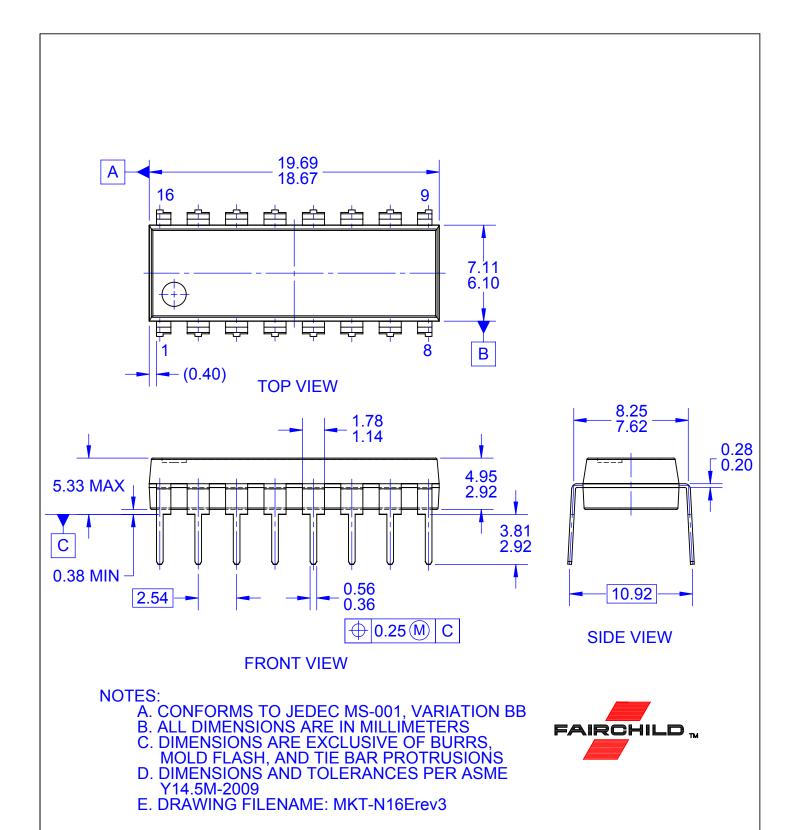
 V_{CC} = 20V, f = 10kHz, T_A = -25°C to +85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Units	
Reference	Section						
V_{REF}	Reference Output Voltage	I _{REF} =1mA, T _A =25°C ⁽¹⁾	4.95	5.00	5.05	V	
		I _{REF} =1mA	4.90	5.00	5.10		
R _{LINE}	Line Regulation	V _{CC} =7V to 40V		2	25	mV	
R _{LOAD}	Load Regulation	I _{REF} =1mA to 10mA		1	15	mV	
I _{SC}	Short-Circuit Output Current	V _{REF} =0V	10	35	50	mA	
Oscillation	Frequency		•	•	•		
	Oscillation Frequency	C_T =0.001 μ F, R_T =30 $K\Omega$		40.0		kHz	
		C_T =0.01 μ F, R_T =12 $K\Omega$, T_A =25° C	9.2	10.0	10.8		
		C_T =0.01 μ F, R_T =12 $K\Omega$, T_A = T_{LOW} to T_{HIGH}	9.0		12.0		
Δf/Δt	Frequency Change with Temperature	$C_T = 0.01 \mu F, R_T = 12 K\Omega$			2	%	
Dead-Tim	e Control Section			I			
I _{BIAS}	Input Bias Current	V _{CC} =15V, 0V≤ V ₄ ≤ 5.25V		-2	-10	μA	
D _(MAX)	Maximum Duty Cycle	V _{CC} =15V, V ₄ =0V, OC Pin=V _{REF}	45	_		%	
		Zero Duty Cycle		3.0	3.3	V	
V_{ITH}	Input Threshold Voltage	Maximum Duty Cycle	0				
Error Amp	lifier Section	, ,	1		l		
V _{IO}	Input Offset Voltage	V ₃ =2.5V		2	10	mV	
I _{IO}	Input Offset Current	V ₃ =2.5V		25	250	mA	
I _{BIAS}	Input Bias Current	V ₃ =2.5V		0.2	1.0	μΑ	
V _{CIM}	Common Mode Input Voltage	7V≤ V _{CC} ≤ 40V	-0.3		V _{CC}	V	
G _{VO}	Open-Loop Voltage Gain	0.5V≤ V ₃ ≤ 3.5V	70	95		dB	
Bw	Unit-Gain Bandwidth			650		kHz	
	parator Section		_		<u> </u>		
V _{ITH}	Input Threshold Voltage	Zero Duty Cycle		4.0	4.5	V	
I _{SINK}	Input Sink Current	V ₃ =0.7V	-0.3	-0.7	- //	mA	
Output Sec				I			
V _{CE(SAT)}	Output Saturation Voltage Common Emitter	V _E =0V, I _C =200mA		1.0	1.3	V	
V _{CC(SAT)}	Emitter-Follower	V _C =15V, I _E =-200mA		1.5	2.5	v	
I _{C(OFF)}	Collector Off-State Current	V _{CC} =40V, V _{CE} =40V		2	100	μА	
I _{E(OFF)}	Emitter Off-State Current	V _{CC} =V _C =40V, V _E =40V			-100		
Total Device	ce .					\leq	
Icc	Supply Current	Pin6=V _{REF} , V _{CC} =15V		6	10	mA	
Output Sw	itching Characteristics						
t _R	Rise Time, Common Emitter, Common Collector			100	200		
t _F	Fall Time, Common Emitter, Common Collector			25	100	ns	

Note:

1. This is guaranteed where the marking code of the package surface is over 027.





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