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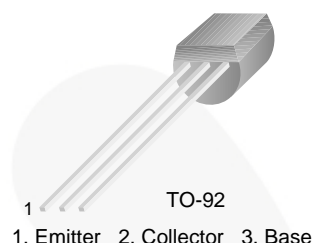
February 2015

KSD1616A

NPN Epitaxial Silicon Transistor

Features

- Audio Frequency Power Amplifier and Medium Speed Switching
- Complement to KSB1116 / KSB1116A



Ordering Information

Part Number	Top Mark	Package	Packing Method
KSD1616AYTA	D1616A	TO-92 3L	Ammo
KSD1616AGBU	D1616A	TO-92 3L	Bulk
KSD1616AGTA	D1616A	TO-92 3L	Ammo
KSD1616ALTA	D1616A	TO-92 3L	Ammo

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage	120	V
V_{CEO}	Collector-Emitter Voltage	60	V
V_{EBO}	Emitter-Base Voltage	6	V
I_C	Collector Current (DC)	1	A
I_{CP}	Collector Current (Pulse) ⁽¹⁾	2	A
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-55 to 150	$^\circ\text{C}$

Note:

1. Pulse width ≤ 10 ms, duty cycle $< 50\%$

Thermal Characteristics⁽²⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Max.	Unit
P_D	Total Device Dissipation	0.75	W
	Derate Above 25°C	6	mW/ $^\circ\text{C}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	160	$^\circ\text{C/W}$

Note:

2. PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{CBO}	Collector-Base Breakdown Voltage	$I_C = 100\ \mu\text{A}$, $I_E = 0$	120			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	$I_C = 1\ \text{mA}$, $I_B = 0$	60			V
BV_{EBO}	Emitter-Base Breakdown Voltage	$I_E = 100\ \mu\text{A}$, $I_C = 0$	6			V
I_{CBO}	Collector Cut-Off Current	$V_{CB} = 60\ \text{V}$, $I_E = 0$			100	nA
I_{EBO}	Emitter Cut-Off Current	$V_{EB} = 6\ \text{V}$, $I_C = 0$			100	nA
h_{FE1}	DC Current Gain	$V_{CE} = 2\ \text{V}$, $I_C = 100\ \text{mA}$	135		400	
h_{FE2}	DC Current Gain	$V_{CE} = 2\ \text{V}$, $I_C = 1\ \text{A}$	81			
$V_{BE(on)}$	Base-Emitter On Voltage ⁽³⁾	$V_{CE} = 2\ \text{V}$, $I_C = 50\ \text{mA}$	600	640	700	mV
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage ⁽³⁾	$I_C = 1\ \text{A}$, $I_B = 50\ \text{mA}$		0.15	0.30	V
$V_{BE(sat)}$	Base-Emitter Saturation Voltage ⁽³⁾	$I_C = 1\ \text{A}$, $I_B = 50\ \text{mA}$		0.9	1.2	V
C_{ob}	Output Capacitance	$V_{CE} = 10\ \text{V}$, $I_E = 0$, $f = 1\ \text{MHz}$		19		pF
f_T	Current Gain Bandwidth Product	$V_{CE} = 2\ \text{V}$, $I_C = 100\ \text{mA}$	100	160		MHz
t_{ON}	Turn-On Time	$V_{CC} = 10\ \text{V}$, $I_C = 100\ \text{mA}$,		0.07		μs
t_{STG}	Storage Time	$I_{B1} = -I_{B2} = 10\ \text{mA}$,		0.95		μs
t_F	Fall Time	$V_{BE(off)} = -2\ \text{V} \sim -3\ \text{V}$		0.07		μs

Note:

3. Pulse test: pulse width $< 350\ \mu\text{s}$, duty cycle $\leq 2\%$ pulsed.

 h_{FE} Classification

Classification	Y	G	L
h_{FE1}	135 ~ 270	200 ~ 400	300 ~ 600

Typical Performance Characteristics

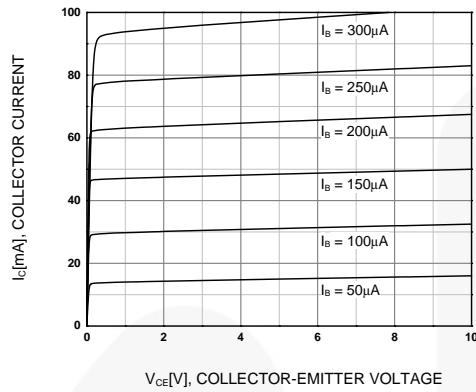


Figure 1. Static Characteristic

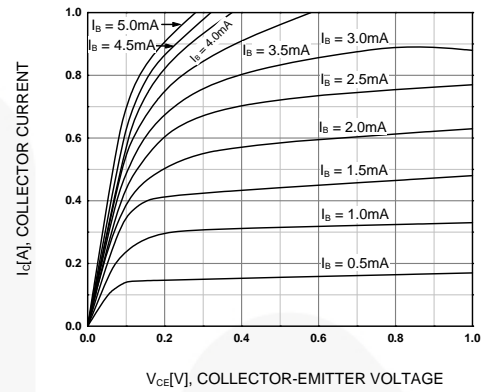


Figure 2. Static Characteristic

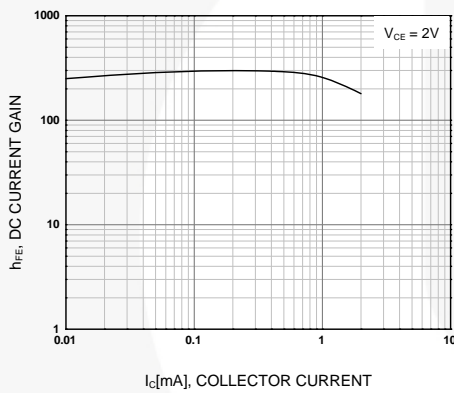


Figure 3. DC Current Gain

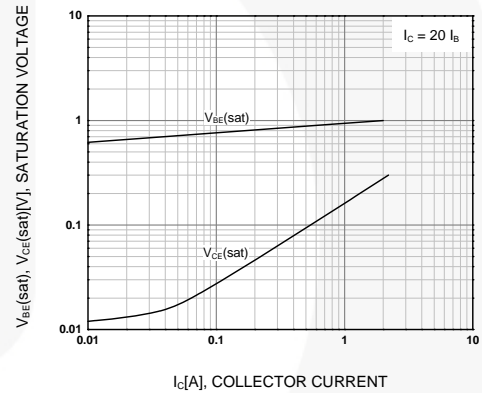


Figure 4. Base-Emitter Saturation Voltage and Collector-Emitter Saturation Voltage

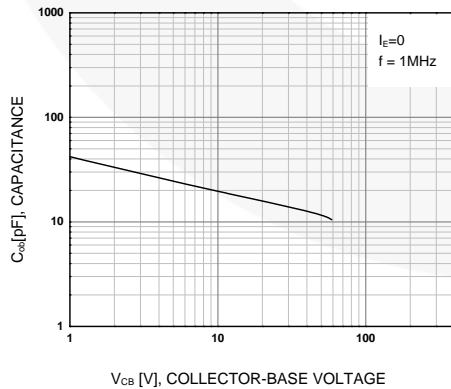


Figure 5. Collector Output Capacitance

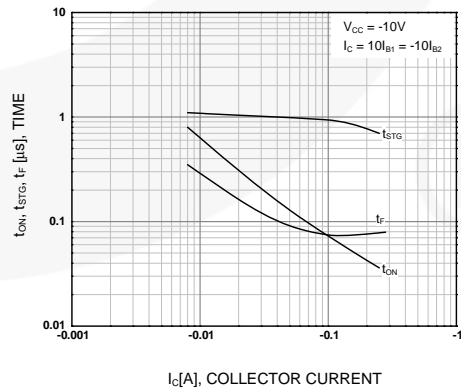


Figure 6. Switching Time

Typical Performance Characteristics (Continued)

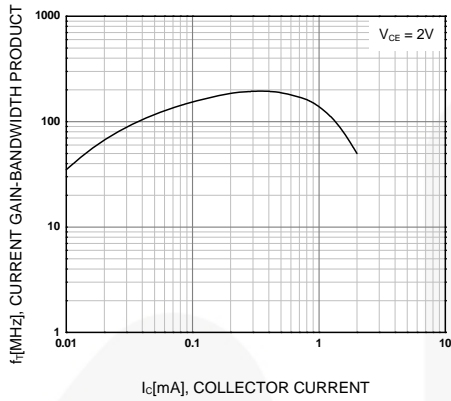


Figure 7. Current Gain Bandwidth Product

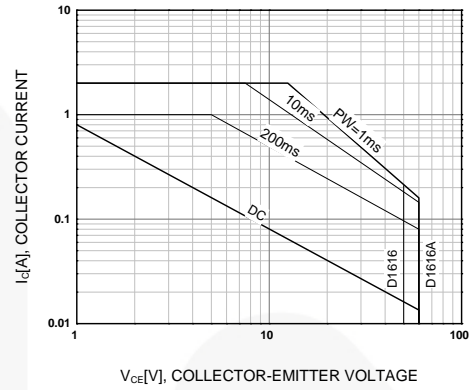


Figure 8. Safe Operating Area

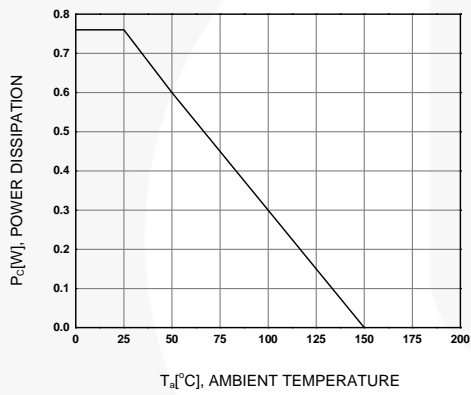
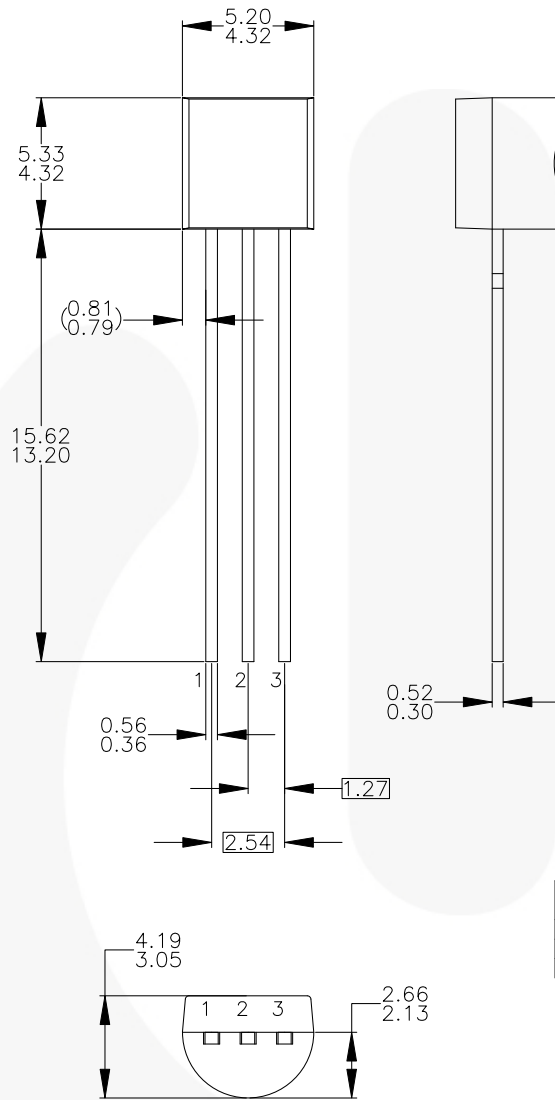


Figure 9. Power Derating

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	P	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

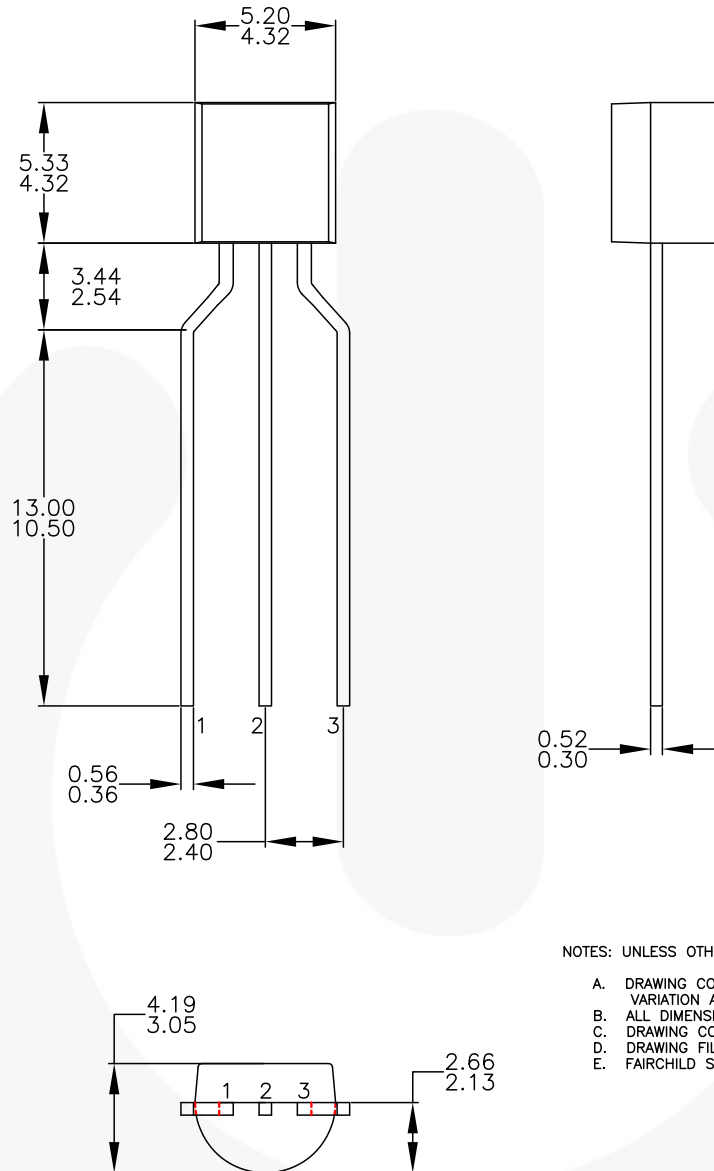
LEGEND:

P - BIPOLAR E - EMITTER D - DRAIN
F - JFET B - BASE S - SOURCE
M - DMOS C - COLLECTOR G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98:
PIN CONFIGURATION DRAIN "D" AND SOURCE "S"
ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

Figure 10. 3-Lead, TO-92, JEDEC TO-92 Compliant Straight Lead Configuration, Bulk Type

Physical Dimensions (Continued)



NOTES: UNLESS OTHERWISE SPECIFIED

- A. DRAWING CONFORMS TO JEDEC MS-013, VARIATION AC.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5M-2009.
- D. DRAWING FILENAME: MKT-ZA03FREVS3.
- E. FAIRCHILD SEMICONDUCTOR.

Figure 11. 3-Lead, TO-92, Molded, 0.2 In Line Spacing Lead Form, Ammo, Tape and Reel Type





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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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