



HIGH SPEED 36K (4K X 9) SYNCHRONOUS DUAL-PORT RAM

IDT70914S

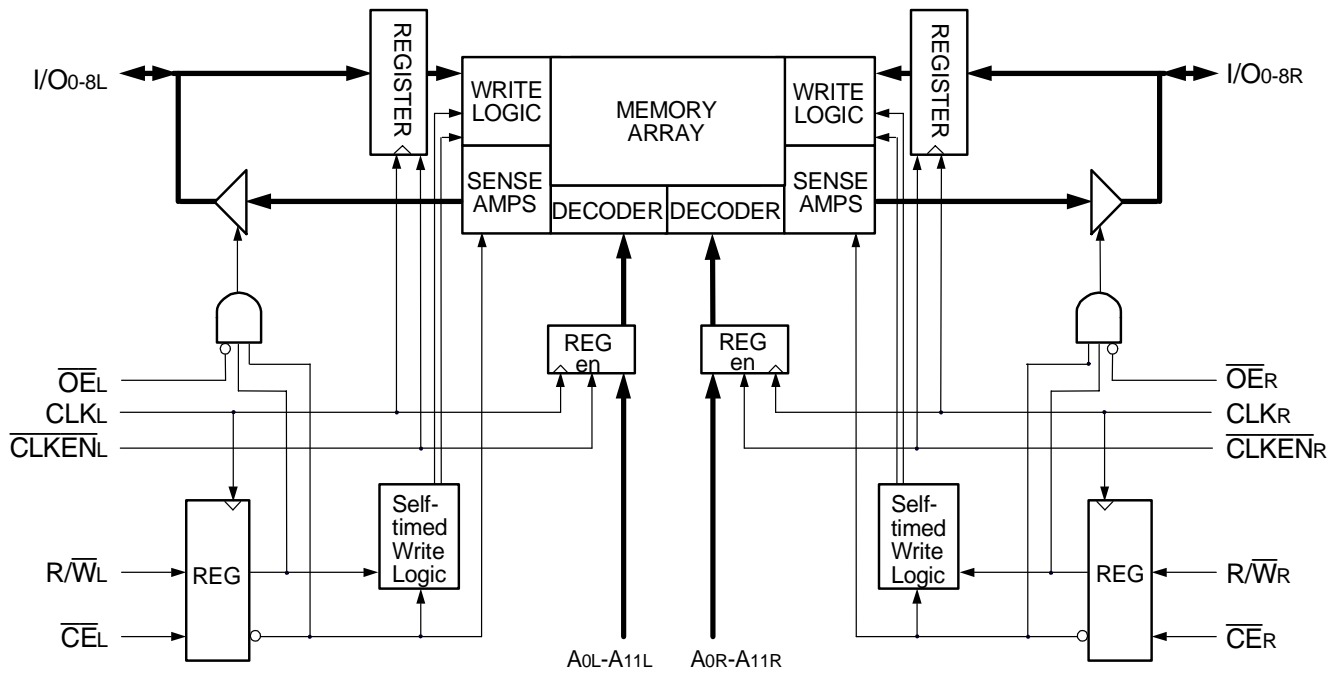
LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features

- ◆ High-speed clock-to-data output times
 - Commercial: 12/15/20ns (max.)
- ◆ Low-power operation
 - IDT70914S
 - Active: 850 mW (typ.)
 - Standby: 50 mW (typ.)
- ◆ Architecture based on Dual-Port RAM cells
 - Allows full simultaneous access from both ports
- ◆ Synchronous operation
 - 4ns setup to clock, 1ns hold on all control, data, and address inputs

- Data input, address, and control registers
- Fast 12ns clock to data out
- Self-timed write allows fast cycle times
- 16ns cycle times, 60MHz operation
- ◆ Clock Enable feature
- ◆ TTL-compatible, single 5V ($\pm 10\%$) power supply
- ◆ Guaranteed data output hold times
- ◆ Available in 68-pin PLCC, and 80-pin TQFP
- ◆ Industrial temperature range (-40°C to +85°C) is available for selected speeds
- ◆ Green parts available, see ordering information

Functional Block Diagram



3490 drw 01

FEBRUARY 2018

Description

The IDT70914 is a high-speed 4K x 9 bit synchronous Dual-Port RAM. The memory array is based on Dual-Port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low set-up and hold times. The timing latitude provided by this approach allow systems to be designed with very short cycle times. With an input data register, this device has been optimized for applications having unidirectional data flow or bidirectional data flow in bursts.

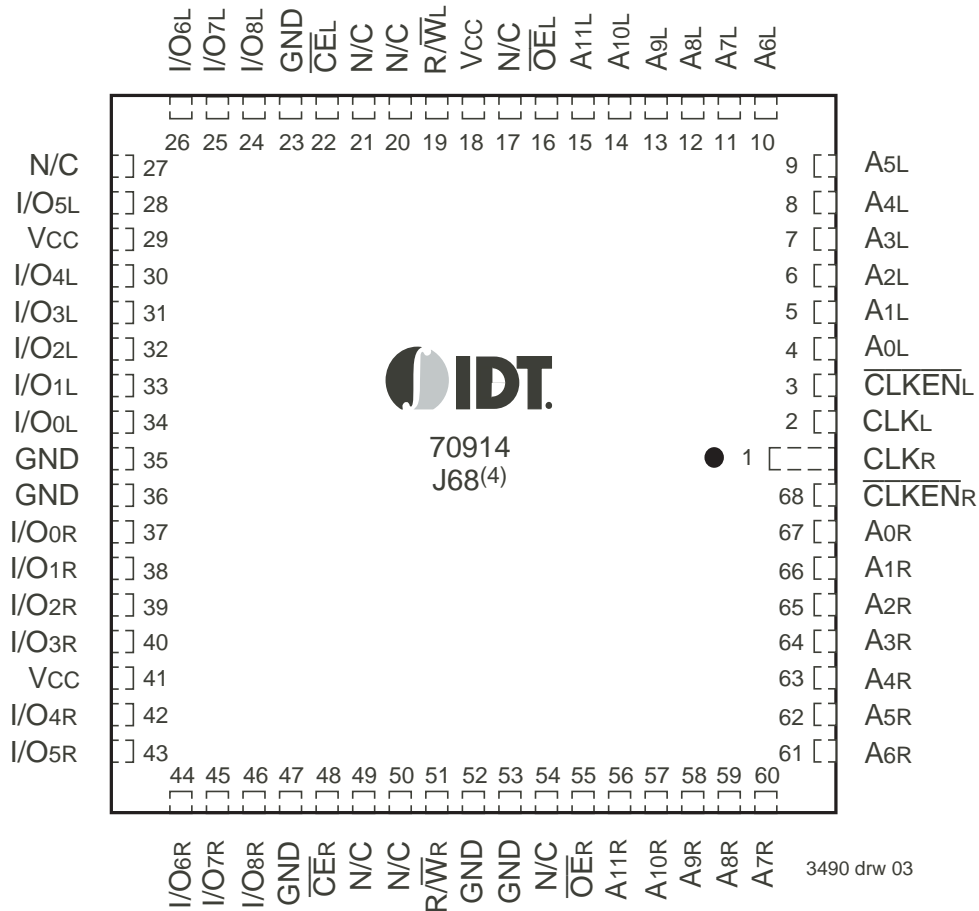
The IDT70914 utilizes a 9-bit wide data path to allow for parity at the

user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/reception error checking.

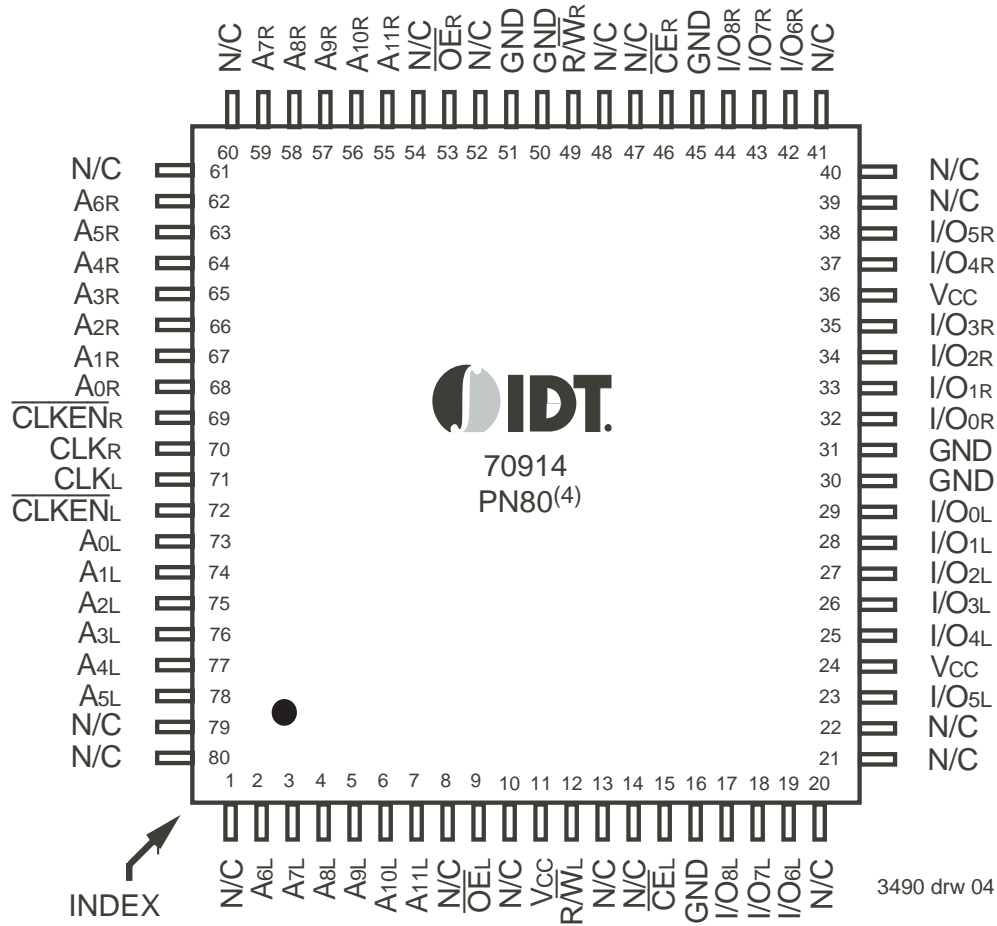
Fabricated using CMOS high-performance technology, these Dual-Ports typically operate on only 850mW of power at maximum high-speed clock-to-data output times as fast as 12ns. An automatic power down feature, controlled by \overline{CE} , permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70914 is packaged in a 68-pin PLCC, and an 80-pin TQFP.

Pin Configurations^(1,2,3)



Pin Configuration^(1,2,3) (con't.)



NOTES:

1. All V_{CC} pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. PN80-1 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Com'l Only	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
V _{TERM} ⁽²⁾	Terminal Voltage	-0.5 to V _{CC}	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	50	mA

3490 tbl 01

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ V_{CC} + 10%.

Capacitance

(T_A = +25°C, f = 1.0MHz) TQFP Only

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	8	pF
C _{OUT}	Output Capacitance	V _{OUT} = 3dV	9	pF

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NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage^(1,2)

Grade	Ambient Temperature	GND	V _{CC}
Commercial	0°C to +70°C	0V	5.0V ± 10%

3490 tbl 02

NOTES:

- This is the parameter T_A. This is the "instant on" case temperature
- Industrial temperature: for specific speeds, packages and powers contact your

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0 ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

3490 tbl 03

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10ns.
- V_{TERM} must not exceed V_{CC} + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	70914S		Unit
			Min.	Max.	
I _{LI}	Input Leakage Current ⁽¹⁾	V _{CC} = 5.5V, V _{IN} = 0V to V _{CC}	—	10	μA
I _{LO}	Output Leakage Current	\overline{CE} = V _{IH} , V _{OUT} = 0V to V _{CC}	—	10	μA
V _{OL}	Output Low Voltage	I _{OL} = +4mA	—	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4mA	2.4	—	V

3490 tbl 05

NOTE:

- At V_{CC} ≤ 2.0V, input leakages are undefined

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽⁴⁾ ($V_{CC} = 5V \pm 10\%$)

Symbol	Parameter	Test Condition	Version	70914S12 Com'l Only		70914S15 Com'l Only		Unit
				Typ. ⁽²⁾	Max.	Typ. ⁽²⁾	Max.	
I _{CC}	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled $f = f_{MAX}^{(1)}$	COM'L	190	310	180	300	mA
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	\overline{CE}_L and $\overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	95	150	90	140	mA
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^{*A} = V_{IL}$ and $\overline{CE}^{*B} = V_{IH}^{(3)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	170	220	160	210	mA
I _{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports \overline{CE}_R and $\overline{CE}_L \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L	10	15	10	15	mA
I _{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}^{*A} \leq 0.2V$ and $\overline{CE}^{*B} \geq V_{CC} - 0.2V^{(3)}$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Disabled $f = f_{MAX}^{(1)}$	COM'L	165	210	155	200	mA

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Symbol	Parameter	Test Condition	Version	70914S20 Com'l Only		Unit
				Typ. ⁽²⁾	Max.	
I _{CC}	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled $f = f_{MAX}^{(1)}$	COM'L	170	290	mA
I _{SB1}	Standby Current (Both Ports - TTL Level Inputs)	\overline{CE}_L and $\overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	85	130	mA
I _{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^{*A} = V_{IL}$ and $\overline{CE}^{*B} = V_{IH}^{(3)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	150	200	mA
I _{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports \overline{CE}_R and $\overline{CE}_L \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L	10	15	mA
I _{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}^{*A} \leq 0.2V$ and $\overline{CE}^{*B} \geq V_{CC} - 0.2V^{(3)}$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Disabled $f = f_{MAX}^{(1)}$	COM'L	145	190	mA

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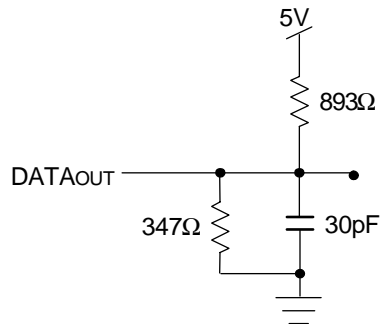
NOTES:

- At f_{MAX} , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cvc}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{CC} = 5V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{CCDC} = 150mA$ (Typ)
- Industrial temperature: for specific speeds, packages and powers contact your sales office.

AC Test Conditions

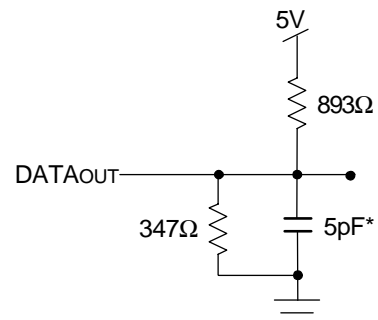
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

3490 tbl 07



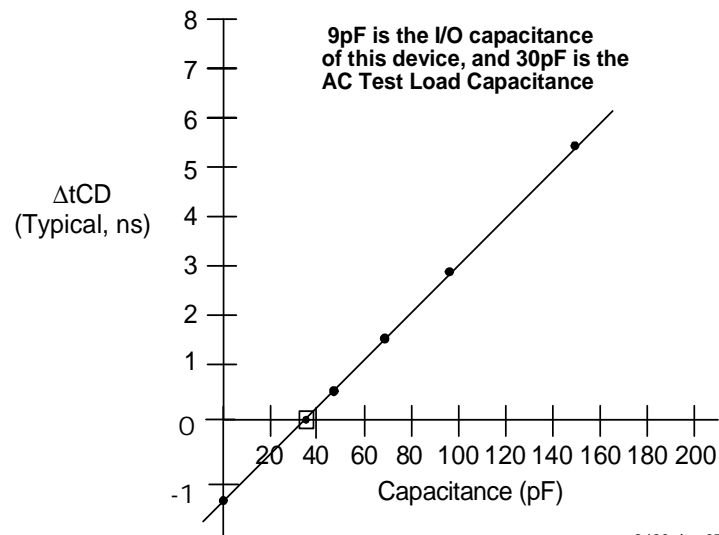
3490 drw 05

Figure 1. AC Output Test load.



3490 drw 06

Figure 2. Output Test Load
(For tCKLZ, tCKHZ, tOLZ, and tOHZ).
*Including scope and jig.



3490 drw 07

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)⁽³⁾ (Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	70914S12 Com'l Only		70914S15 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	16	—	20	—	ns
t _{CH}	Clock High Time	6	—	6	—	ns
t _{CL}	Clock Low Time	6	—	6	—	ns
t _{CD}	Clock High to Output Valid	—	12	—	15	ns
t _S	Registered Signal Set-up Time	4	—	4	—	ns
t _H	Registered Signal Hold Time	1	—	1	—	ns
t _{DC}	Data Output Hold After Clock High	3	—	3	—	ns
t _{CKLZ}	Clock High to Output Low-Z ^(1,2)	2	—	2	—	ns
t _{CKHZ}	Clock High to Output High-Z ^(1,2)	—	7	—	7	ns
t _{OE}	Output Enable to Output Valid	—	7	—	8	ns
t _{OLZ}	Output Enable to Output Low-Z ^(1,2)	0	—	0	—	ns
t _{OHZ}	Output Disable to Output High-Z ^(1,2)	—	7	—	7	ns
t _{SCK}	Clock Enable, Disable Set-up Time	4	—	4	—	ns
t _{HCK}	Clock Enable, Disable Hold Time	2	—	2	—	ns
Port-to-Port Delay						
t _{WDD}	Write Port Clock High to Read Data Delay	—	25	—	30	ns
t _{CSS}	Clock-to-Clock Setup Time	—	13	—	15	ns

3490 tbl 08a

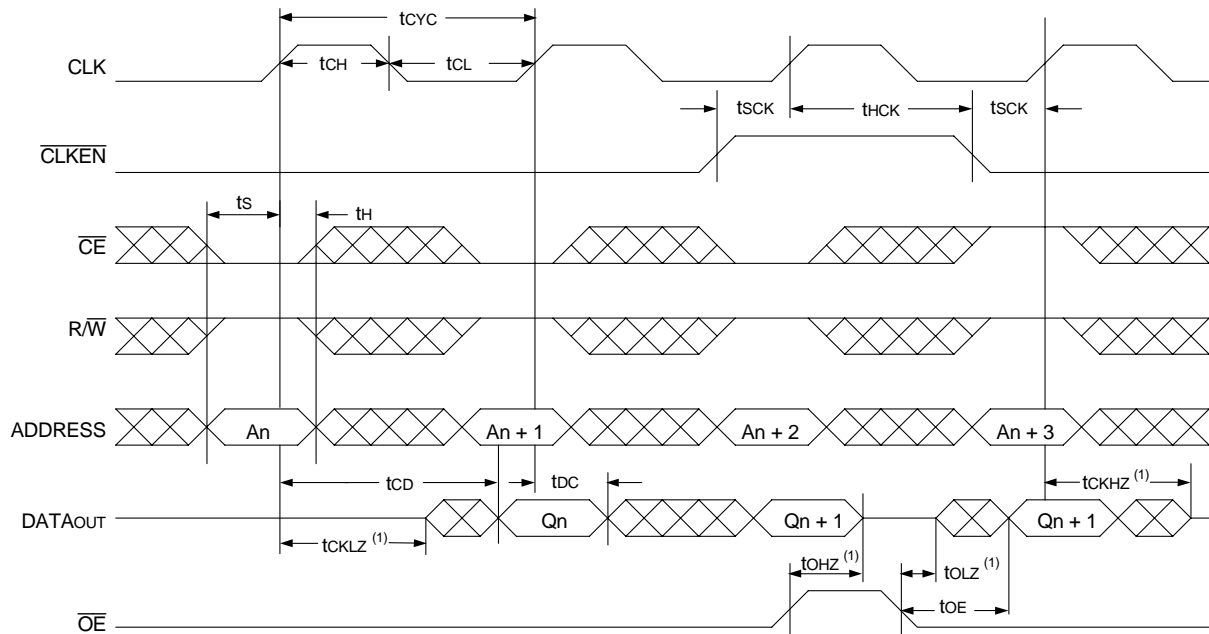
Symbol	Parameter	70914S20 Com'l Only		Unit
		Min.	Max.	
t _{CYC}	Clock Cycle Time	20	—	ns
t _{CH}	Clock High Time	8	—	ns
t _{CL}	Clock Low Time	8	—	ns
t _{CD}	Clock High to Output Valid	—	20	ns
t _S	Registered Signal Set-up Time	5	—	ns
t _H	Registered Signal Hold Time	1	—	ns
t _{DC}	Data Output Hold After Clock High	3	—	ns
t _{CKLZ}	Clock High to Output Low-Z ^(1,2)	2	—	ns
t _{CKHZ}	Clock High to Output High-Z ^(1,2)	—	9	ns
t _{OE}	Output Enable to Output Valid	—	10	ns
t _{OLZ}	Output Enable to Output Low-Z ^(1,2)	0	—	ns
t _{OHZ}	Output Disable to Output High-Z ^(1,2)	—	9	ns
t _{SCK}	Clock Enable, Disable Set-up Time	5	—	ns
t _{HCK}	Clock Enable, Disable Hold Time	2	—	ns
Port-to-Port Delay				
t _{WDD}	Write Port Clock High to Read Data Delay	—	35	ns
t _{CSS}	Clock-to-Clock Setup Time	—	15	ns

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NOTES:

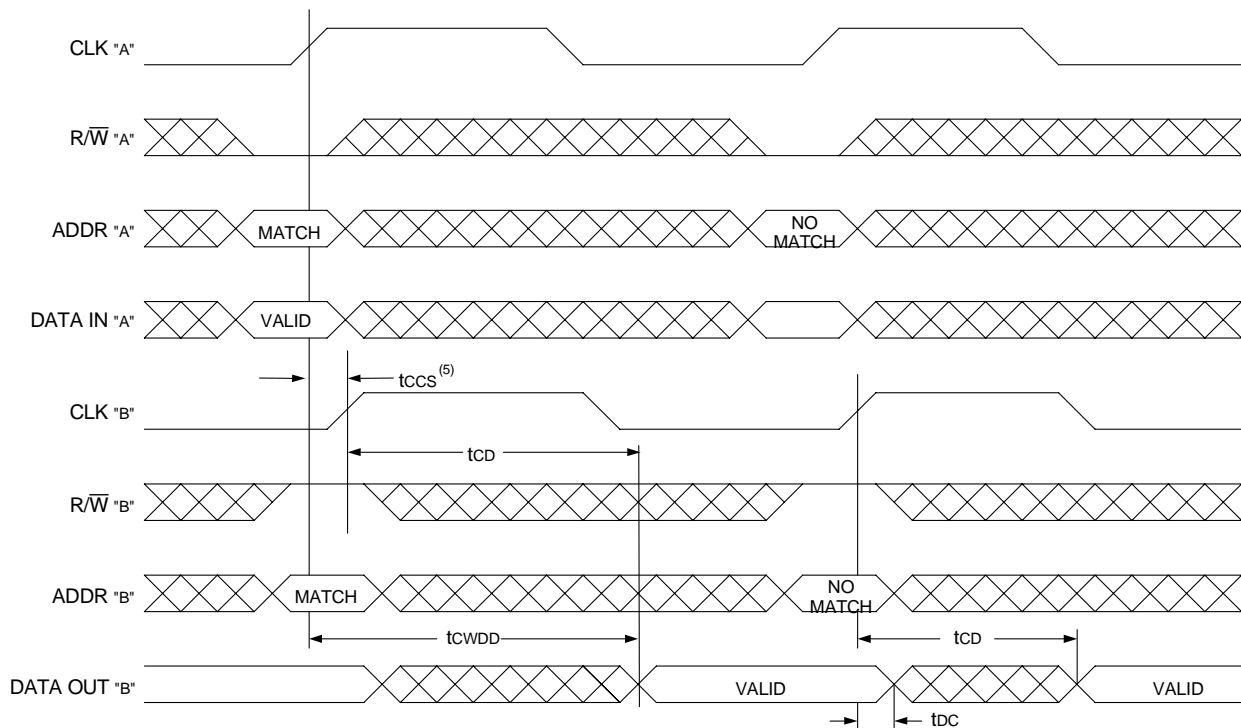
1. Transition is measured 0mV from Low or High impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Timing Waveform of Read Cycle, Either Side



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Timing Waveform of Write with Port-to-Port Read^(2,3,4)

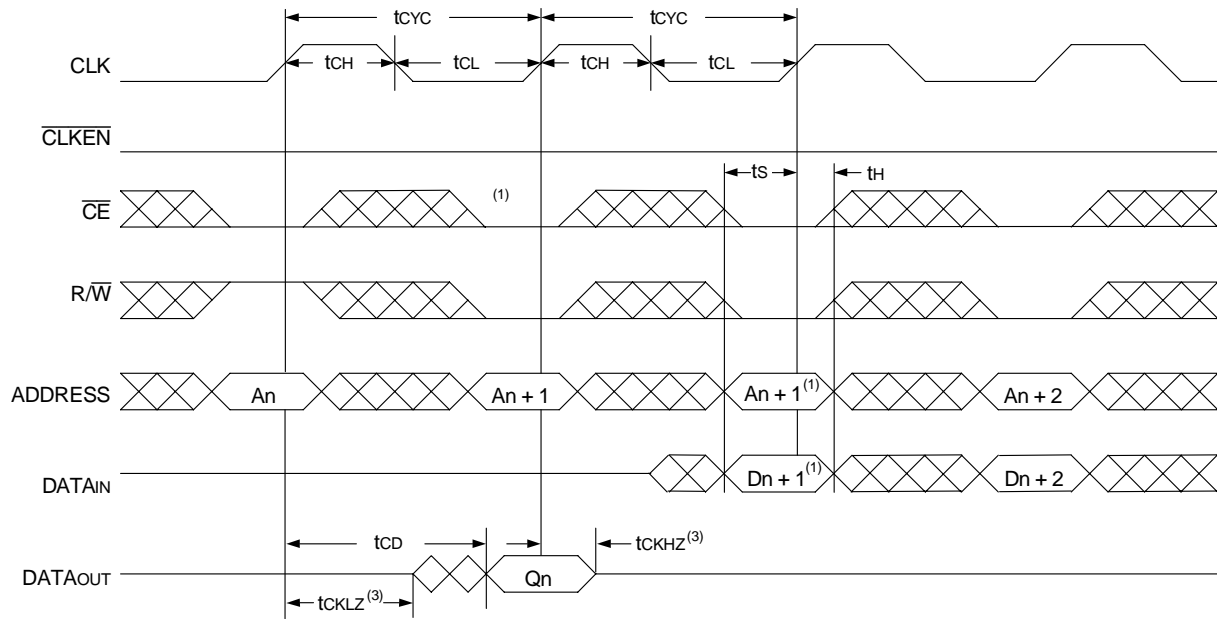


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NOTES:

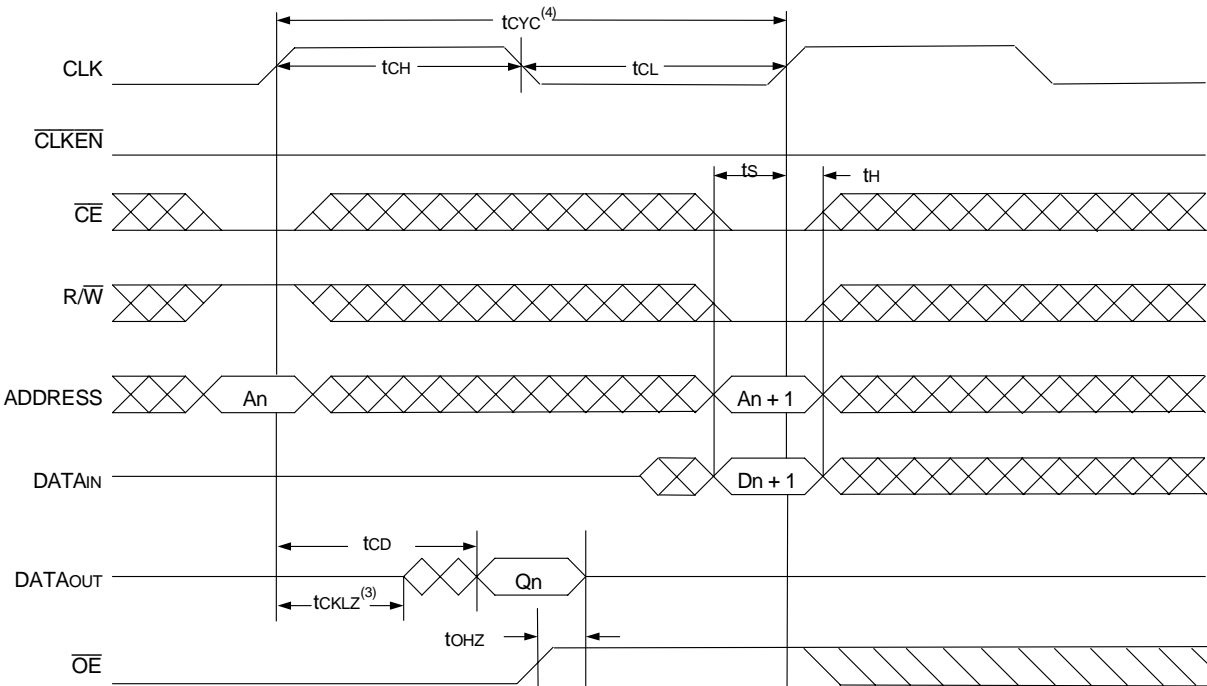
1. Transition is measured $\pm 200\text{mV}$ from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$, $\overline{CLKEN}_L = \overline{CLKEN}_R = V_{IL}$.
3. $\overline{OE} = V_{IL}$ for the reading port, port 'B'.
4. All timing is the same for left and right ports. Ports "A" may be either the left or right port. Port "B" is opposite from port "A".
5. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD} .
If $t_{CCS} >$ maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD}$. t_{CWDD} does not apply in this case.

Timing Waveform of Read-to-Write Cycle No. 1^(1,2) ($t_{CYC} = \text{min.}$)



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Timing Waveform of Read-to-Write Cycle No. 2⁽⁴⁾ ($t_{CYC} > \text{min.}$)



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NOTES:

1. For $t_{CYC} = \text{min.}$; data out coincident with the rising edge of the subsequent write clock can occur. To ensure writing to the correct address location, the write must be repeated on the second write clock rising edge. If $\overline{CE} = V_{IL}$, invalid data will be written into array. The $An+1$ must be rewritten on the following cycle.
2. \overline{OE} LOW throughout.
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. For $t_{CYC} > \text{min.}$; \overline{OE} may be used to avoid data out coincident with the rising edge of the subsequent write clock. Use of \overline{OE} will eliminate the need for the write to be repeated.

Functional Description

The IDT70914 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is dependent on the LOW to HIGH

transitions of the clock signal allowing the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

A HIGH on the \overline{CE} input for one clock cycle will power down the internal circuitry to reduce static power consumption.

Truth Table I: Read/Write Control⁽¹⁾

Inputs			Asynchronous	Outputs	Mode
Synchronous ⁽³⁾		\overline{OE}			
CLK	\overline{CE}		R/W	I/O ₀₋₈	
↑	H	X	X	High-Z	Deselected, Power-Down
↑	L	L	X	DATA _{IN}	Selected and Write Enabled
↑	L	H	L	DATA _{OUT}	Read Selected and Data Output Enable Read
↑	X	X	H	High-Z	Outputs Disabled

3490 tbl 09

Truth Table II: Clock Enable Function Table⁽¹⁾

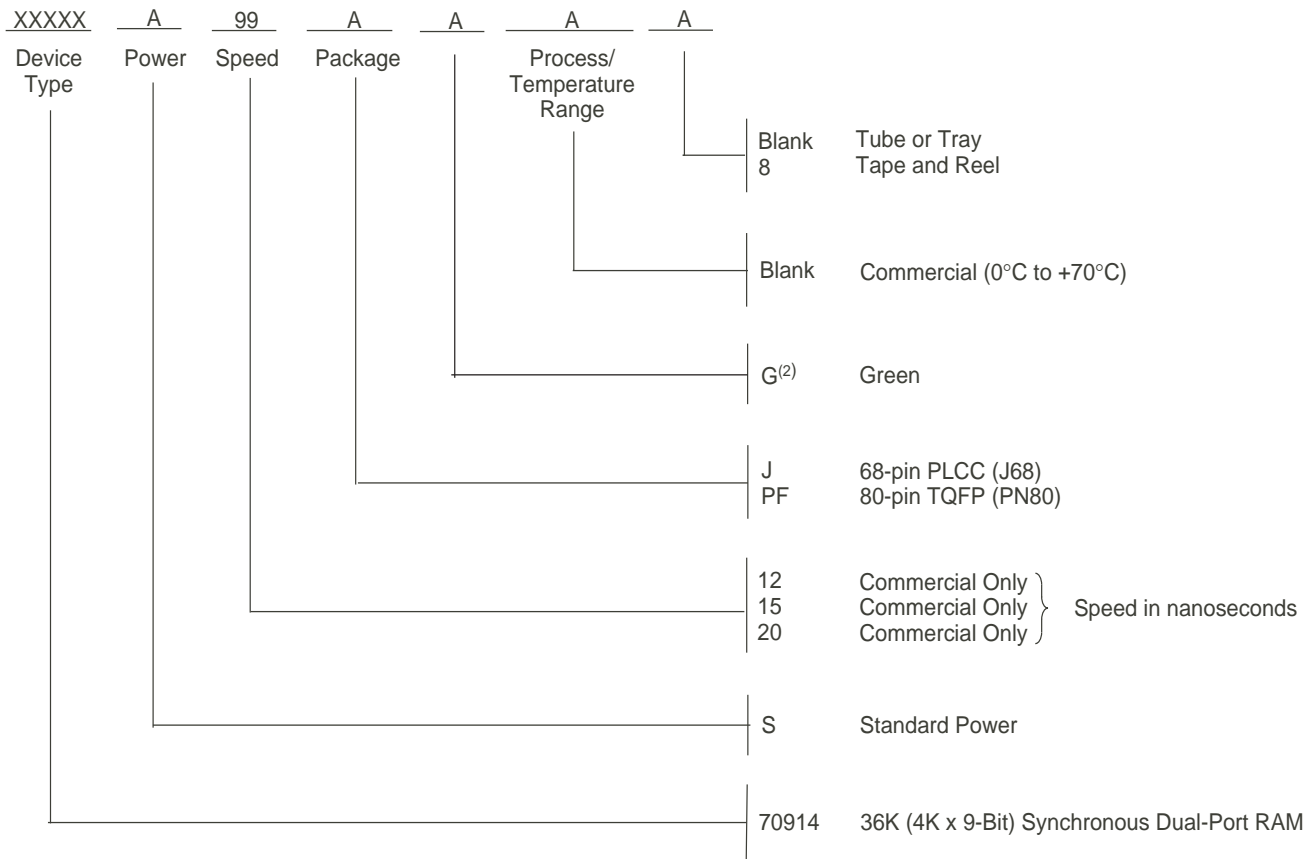
Mode	Inputs		Register Inputs		Register Outputs ⁽⁴⁾	
	CLK ⁽³⁾	\overline{CLKEN} ⁽²⁾	ADDR	DATA _{IN}	ADDR	DATA _{OUT}
Load "1"	↑	L	H	H	H	H
Load "0"	↑	L	L	L	L	L
Hold (do nothing)	↑	H	X	X	NC	NC
	X	H	X	X	NC	NC

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NOTES:

- 'H' = HIGH voltage level steady state, 'h' = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'L' = LOW voltage level steady state 'l' = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'X' = Don't care, 'NC' = No change
- \overline{CLKEN} = V_{IL} must be clocked in during Power-Up.
- Control signals are initiated and terminated on the rising edge of the CLK, depending on their input level. When $\overline{R/W}$ and \overline{CE} are LOW, a write cycle is initiated on the LOW-to-HIGH transition of the CLK. Termination of a write cycle is done on the next LOW-to-HIGH transition of the CLK.
- The register outputs are internal signals from the register inputs being clocked in or disabled by \overline{CLKEN} .

Ordering Information



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NOTES:

- Industrial temperature range is available on selected TQFP packages in standard power. For specific speeds, packages and powers contact your sales office.
- Green parts available. For specific speeds, packages and powers contact your sales office.

LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

- 3/10/99: Initiated datasheet document history
Converted to new format
Cosmetic and typographical corrections
Page 2 and 3 Added additional notes to pin configurations
- 6/7/99: Changed drawing format
- 11/10/99: Replaced IDT logo
- 5/24/00: Page 4 Increased storage temperature parameter
Clarified TA parameter
Page 5 DC Electrical parameters—changed wording from "open" to "disabled"
Changed ±200mV to 0mV in notes
- 1/12/01: Removed PGA pinout (obsolete package)
Changed cycle time of 12ns part from 17ns (58MHz) to 16ns (60MHz)
- 10/21/08: Page 11 Removed "IDT" from orderable part number
- 05/24/10: Page 1 Added green parts availability to features
Page 11 Added green indicator to ordering information

Datasheet Document History (con't.)

- 06/05/15: Pages 1-12 Removed Military and Industrial Temperature Ranges from datasheet header
Page 1 Removed Military speed offerings from the Features
Page 2 Removed MIL-PRF 38535 QML support information
Pages 2, 3 & 11 The package codes J68-1 and PN80-1 changed to J68 and PN80 respectively to match the standard package codes
Page 4 Removed the military and industrial offerings in the Absolute Max Ratings & the Max Operating Temp tables
Page 5 Removed the military and industrial offerings in the DC Elec Chars tables
Page 6 Corrected typo in the Typical Output Derating drawing
Page 7 Removed military offering for the 20 & 25 speed grades in the AC Elec Chars table
Removed the military temp range information from the AC Elec Chars table title
Page 11 Added Tape and Reel to and removed military offering & 25ns speed grade from the Ordering Information
- 04/28/16: Page 2 Changed diagram for the J68 pin configuration by rotating package pin labels and pin numbers 90 degrees clockwise to reflect pin1 orientation and added pin 1 dot at pin 1
Removed all four chamfers from J68 and aligned the top and bottom pin labels in the standard direction
Page 3 Changed diagram for the PN80 pin configuration by rotating package pin labels and pin numbers 90 degrees counter clockwise to reflect pin 1 orientation and added pin 1 dot at pin 1
Added the IDT logo, changed the text to be in alignment with new diagram marking specs for all pin configurations and updated footnote references for the J68 & the PN80 pin configurations
- Page 11 Removed Industrial temp range information from the Ordering Information
- 02/02/18: Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018



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