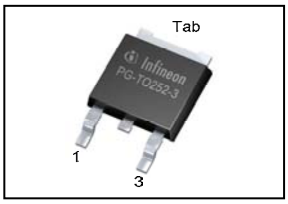
OptiMOS®-T2 Power-Transistor

Product Summary

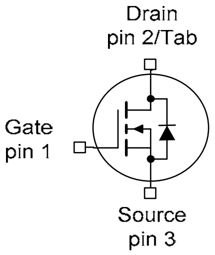
V_{DS}	60	V
$R_{DS(on),max}$	7.8	mΩ
I_D	50	A

PG-TO252-3-11



Features

- N-channel - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested



Type	Package	Marking
IPD50N06S4L-08	PG-TO252-3-11	4N06L08

Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current[1)]	I_D	T_C=25°C, V_{GS}=10V	50	A
		T_C=100°C, V_{GS}=10V[2)]	47	
Pulsed drain current[2)]	$I_{D,pulse}$	T_C=25°C	200	
Avalanche energy, single pulse[2)]	E_{AS}	I_D=25A	87	mJ
Avalanche current, single pulse	I_{AS}	-	50	A
Gate source voltage	V_{GS}	-	±16	V
Power dissipation	P_{tot}	T_C=25°C	71	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	–

Parameter	**Symbol**	**Conditions**	**Values**			**Unit**
			min.	**typ.**	**max.**	
Thermal characteristics2)						
Thermal resistance, junction - case	R_{thJC}	-	-	-	2.1	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area3)	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{\mathrm{(BR)DSS}}$	V_{GS}=0V, I_{D}= 1mA	60	-	-	V
Gate threshold voltage	$V_{\mathrm{GS(th)}}$	V_{DS}=V_{GS}, I_{D}=35µA	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	V_{DS}=60V, V_{GS}=0V, T_j=25°C	-	0.01	1	µA
		V_{DS}=60V, V_{GS}=0V, T_j=125°C2)	-	5	100	
Gate-source leakage current	I_{GSS}	V_{GS}=16V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{\mathrm{DS(on)}}$	V_{GS}=4.5V, I_{D}=25A	-	9.0	13.5	mΩ
		V_{GS}=10V, I_{D}=50A	-	6.3	7.8	

Parameter	**Symbol**	**Conditions**	**Values**			**Unit**
			min.	**typ.**	**max.**	
Dynamic characteristics[2]						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	3680	4780	pF
Output capacitance	C_{oss}		-	840	1090	
Reverse transfer capacitance	C_{rss}		-	40	80	
Turn-on delay time	$t_{d(on)}$	V_{DD}=30V, V_{GS}=10V, I_D=50A, R_G=3.5Ω	-	9	-	ns
Rise time	t_r		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	45	-	
Fall time	t_f		-	8	-	
Gate Charge Characteristics[2]						
Gate to source charge	Q_{gs}	V_{DD}=48V, I_D=50A, V_{GS}=0 to 10V	-	13	19	nC
Gate to drain charge	Q_{gd}		-	5	10	
Gate charge total	Q_g		-	49	64	
Gate plateau voltage	$V_{plateau}$		-	3.6	-	V
Reverse Diode						
Diode continous forward current[2]	I_S	T_C=25°C	-	-	50	A
Diode pulse current[2]	$I_{S,pulse}$		-	-	200	
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=50A, T_j=25°C	0.6	0.95	1.3	V
Reverse recovery time[2]	t_{rr}	V_R=30V, I_F=I_S, di_F/dt=100A/µs	-	33	-	ns
Reverse recovery charge[2]	Q_{rr}		-	32	-	nC

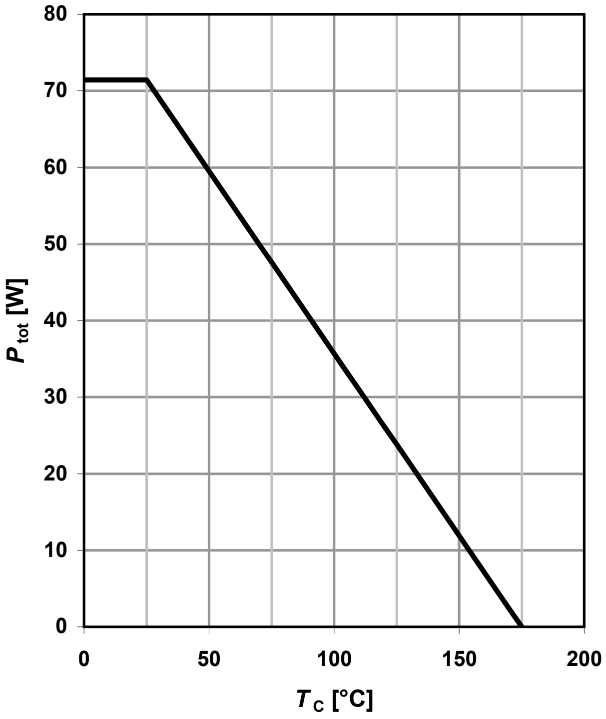
[1] Current is limited by bondwire; with an R_{thJC} = 2.1K/W the chip is able to carry 65A at 25°C.

[2] Specified by design. Not subject to production test.

[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

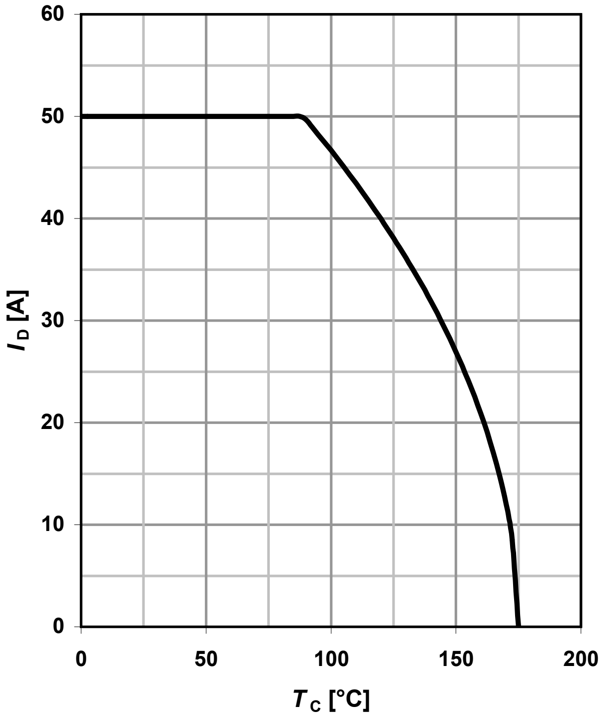
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6$ V



2 Drain current

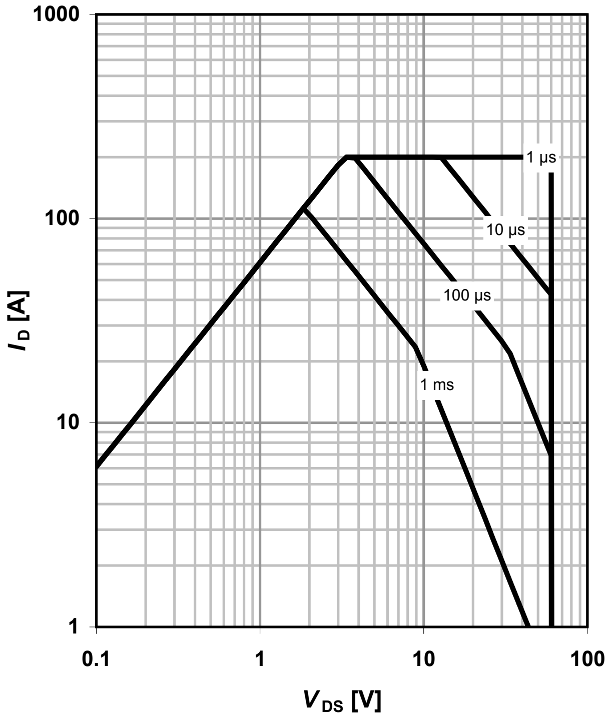
$I_D = f(T_C)$; $V_{GS} \geq 6$ V



3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25$ °C; $D = 0$

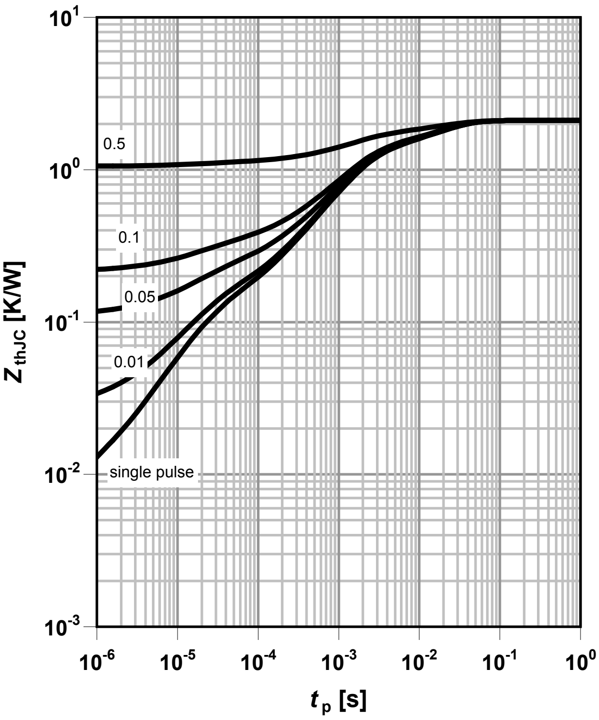
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

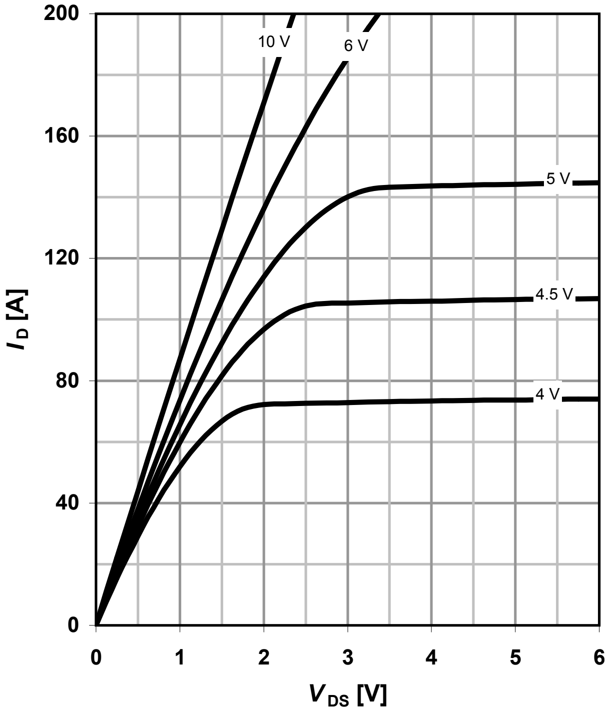
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS})$; $T_j = 25$ °C

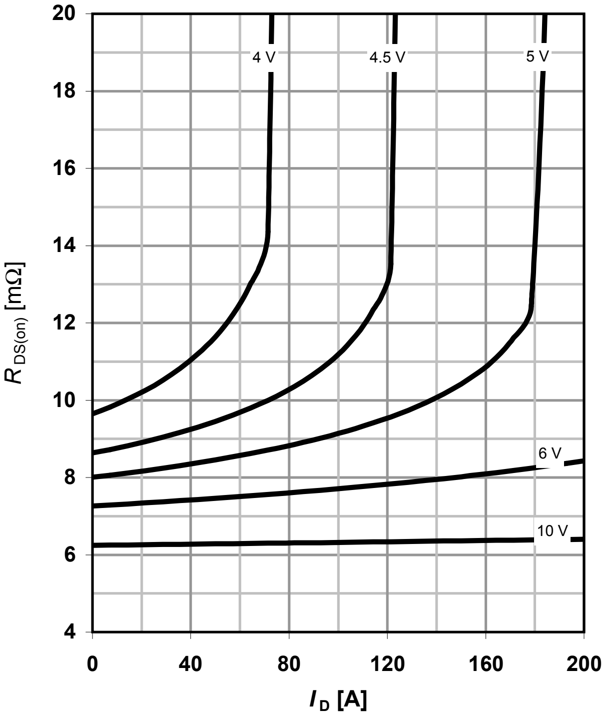
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D)$; $T_j = 25$ °C

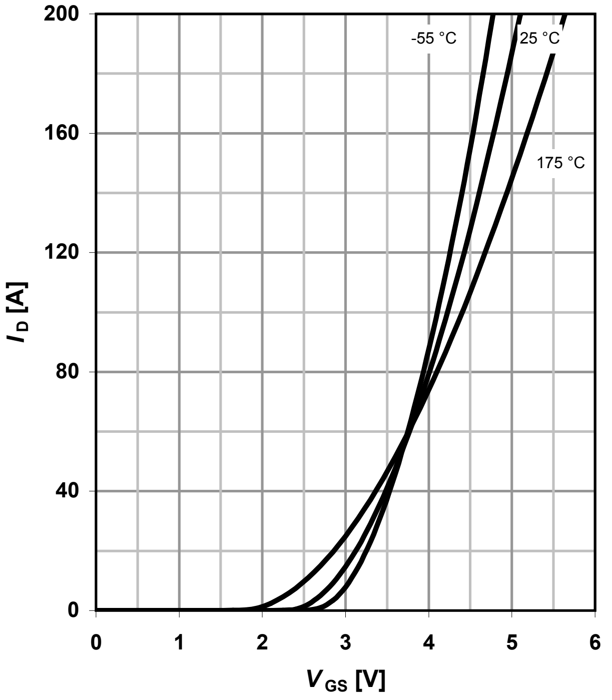
parameter: V_{GS}



7 Typ. transfer characteristics

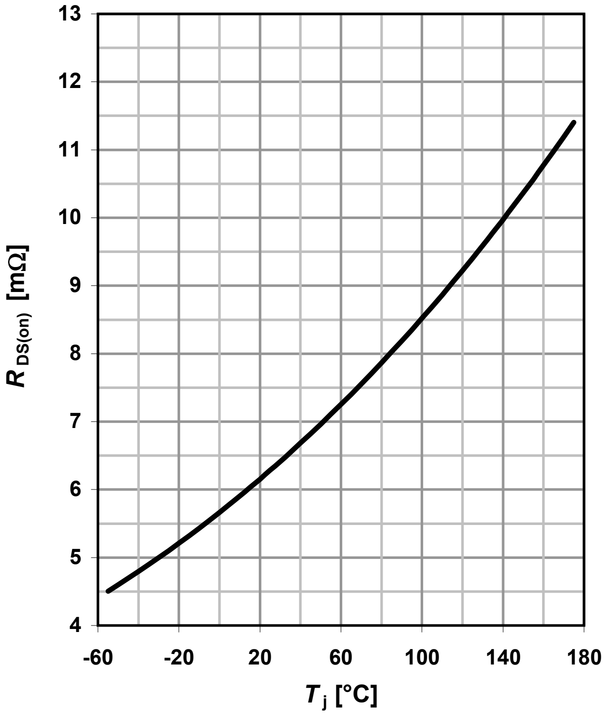
$I_D = f(V_{GS})$; $V_{DS} = 6$V

parameter: T_j



8 Typ. drain-source on-state resistance

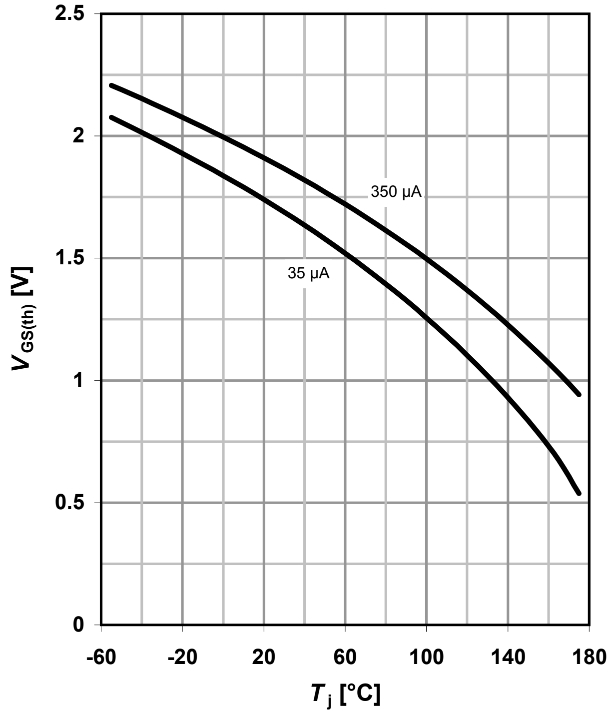
$R_{DS(on)} = f(T_j)$; $I_D = 50$ A; $V_{GS} = 10$ V



9 Typ. gate threshold voltage

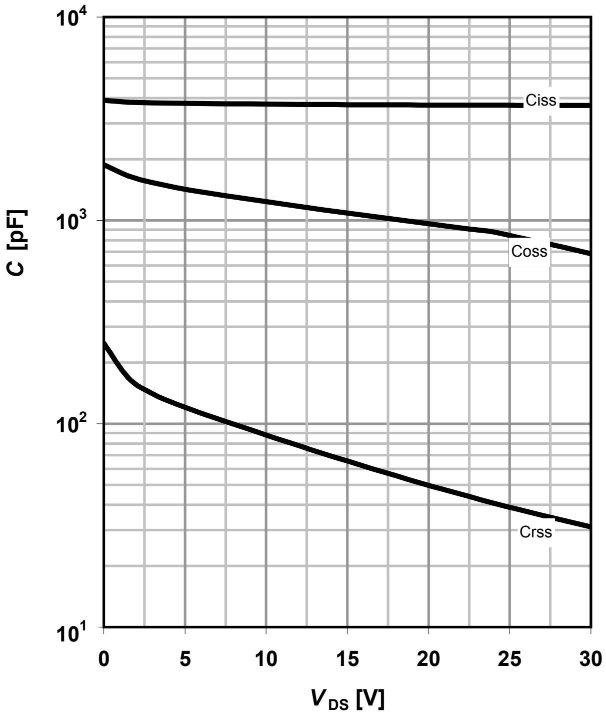
$V_{GS(th)} = f(T_j)$; $V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

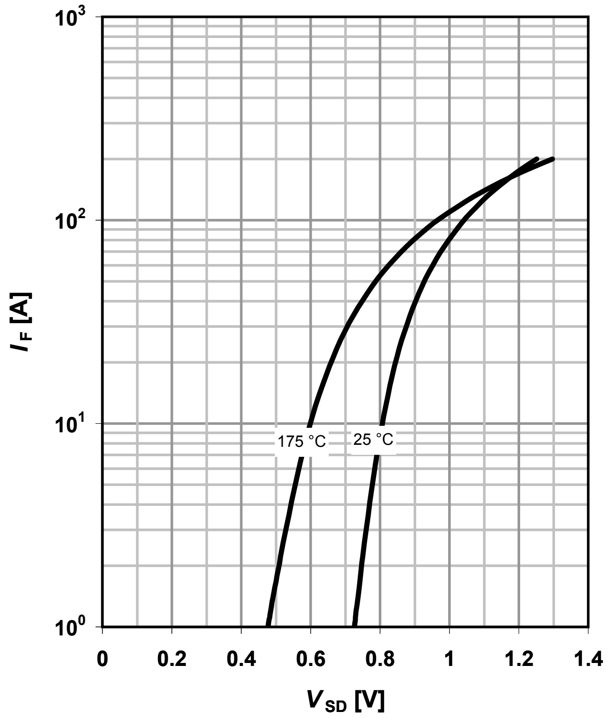
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz



11 Typical forward diode characteristicis

IF = $f(V_{SD})$

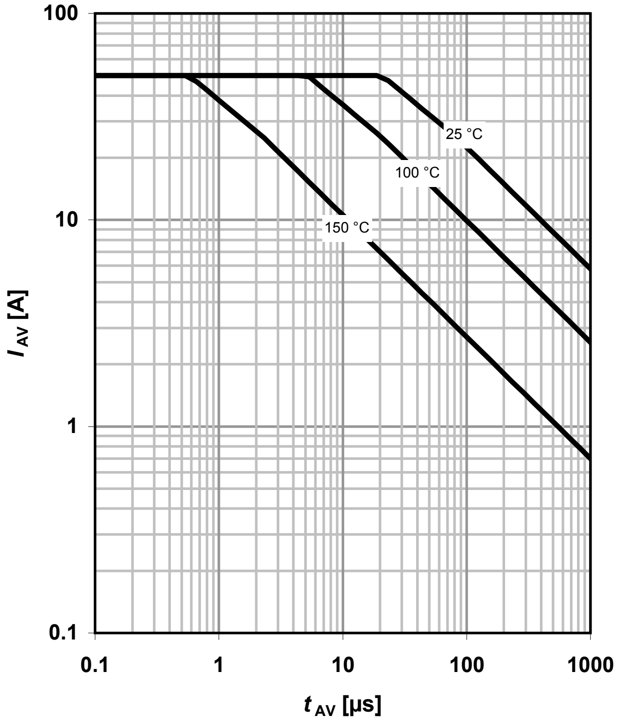
parameter: T_j



12 Avalanche characteristics

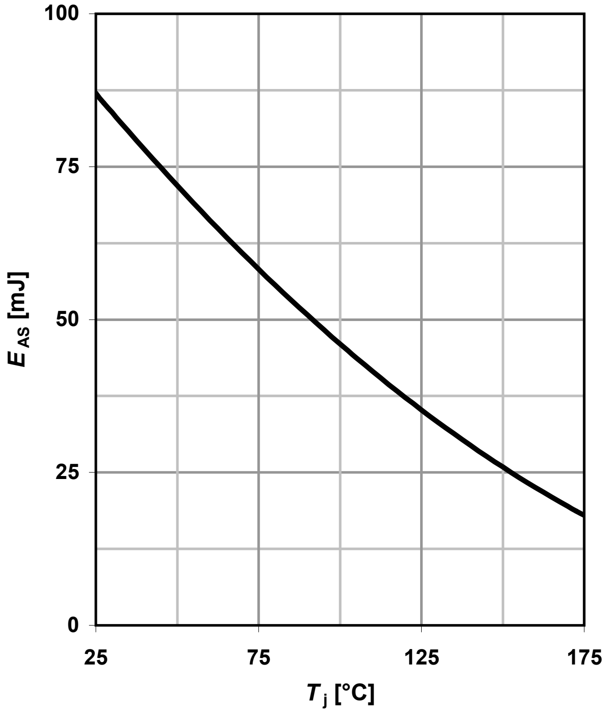
$I_{AS} = f(t_{AV})$

parameter: $T_{j(start)}$



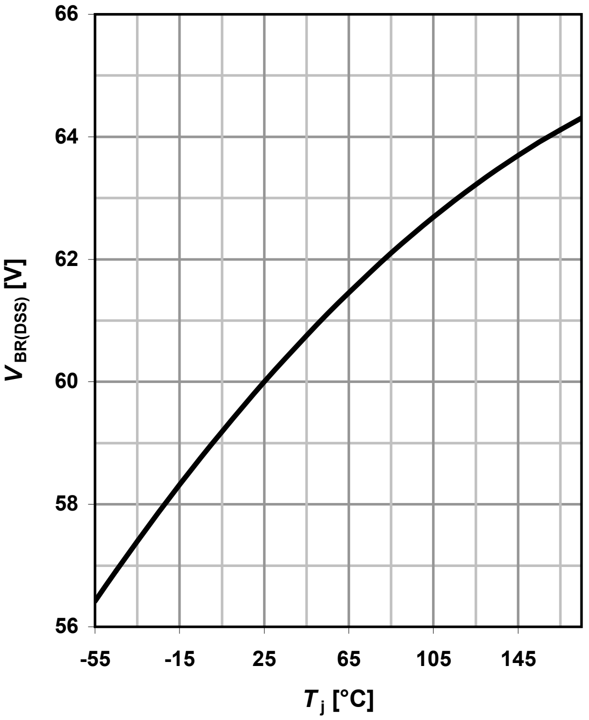
13 Avalanche energy

$E_{AS} = f(T_j)$; $I_D = 25$ A



14 Drain-source breakdown voltage

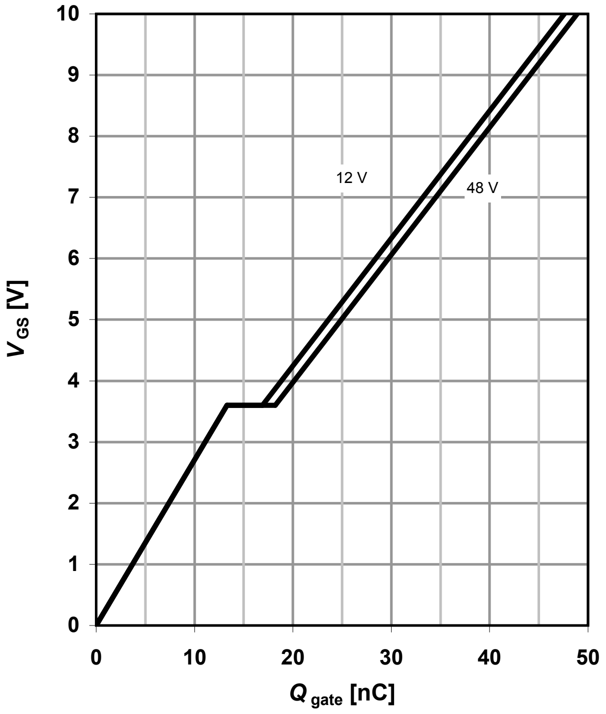
$V_{BR(DSS)} = f(T_j)$; $I_D = 1$ mA



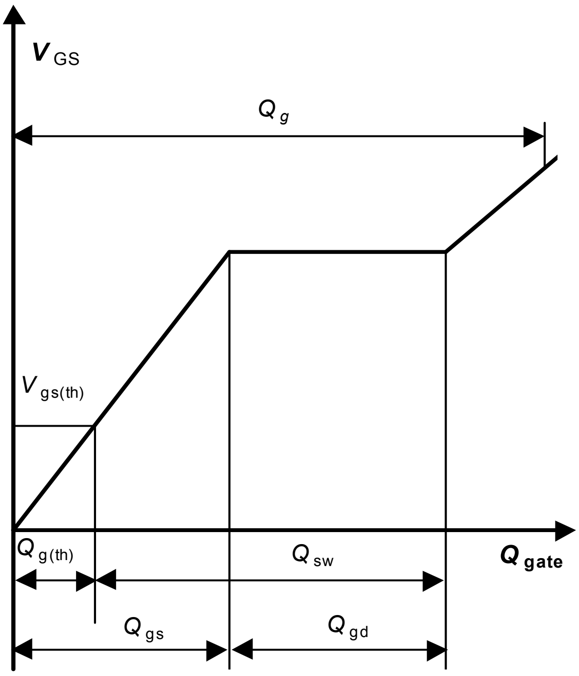
15 Typ. gate charge

$V_{GS} = f(Q_{gate})$; $I_D = 50$ A pulsed

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

Version	Date	Changes
Revision 1.0	24.03.2009	Final data sheet