Never stop thinking

32-Bit

Microcontroller

TC1798

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.1 2014-05

Microcontrollers

Edition 2014-05

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Table of Contents

1 Summary of Features

The **SAK-TC1798F-512F300EL / SAK-TC1798F-512F300EP** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - 300 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
  - 4 Mbyte Program Flash Memory (PFLASH) with ECC
  - 192 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 2 x 8 Kbyte Key Flash
  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)
  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication

  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture / Compare 6 modules
  - Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 64 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, ADC2, and ADC3)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 8 digital input lines for SENT
  - communication according to the SENT specification J2716 FEB2008
- 238 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1798ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL and PLL_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)

The **SAK-TC1798N-512F300EP** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - 300 MHz operation at full temperature range

- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
  - 4 Mbyte Program Flash Memory (PFLASH) with ECC
  - 192 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 2 x 8 Kbyte Key Flash
  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)
  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication
  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture / Compare 6 modules

  - Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 64 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, ADC2, and ADC3)
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  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 8 digital input lines for SENT
  - communication according to the SENT specification J2716 FEB2008
- 238 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1798ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL and PLL_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)

The **SAK-TC1798S-512F300EP** has the following features:

- High-performance 32-bit super-scalar TriCore V1.6 CPU with 6-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
  - Fully pipelined Floating point unit (FPU)
  - 300 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 200 MHz operation at full temperature range
- Multiple on-chip memories
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  - 16 Kbyte Instruction Cache (ICACHE)
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Data Cache (DACHE)

  - 128 Kbyte Memory (SRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- 8-Channel Safe DMA (SDMA) Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Cross Bar Interconnect between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (SFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Four High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - Four SSC Guardian (SSCG) modules, one for each SSC
  - Two serial Micro Second Bus interfaces (MSC) for serial port expansion to external power devices
  - Two High-Speed Micro Link interfaces (MLI) for serial inter-processor communication
  - One External Bus Interface (EBU) supporting different memories: asynchronous memories e.g. SRAM, peripheral devices; synchronous devices e.g. burst NOR flash, PSRAM; and DDR NOR flash e.g. LPDDR-NVM (Jedec 42.2), ONFI 2.0 (limited frequency at 1.8 V I/O supply)
  - One MultiCAN Module with 4 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).
  - Two General Purpose Timer Array Modules (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
  - Two Capture / Compare 6 modules
  - Two General Purpose 12 Timer Units (GPT120 and GPT121)
- 64 analog input lines for ADC
  - 4 independent kernels (ADC0, ADC1, ADC2, and ADC3)
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- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 8 digital input lines for SENT
  - communication according to the SENT specification J2716 FEB2008

- 238 digital general purpose I/O lines (GPIO)
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Buses)
- Dedicated Emulation Device chip available (TC1798ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL and PLL_ERAY
- Flexible CRC Engine (FCE)
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)
- Secure Hardware Extension (SHE)
  - For further information please contact your Infineon representative

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1798 please refer to the **"Product Catalog Microcontrollers"**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

Table 1 TC1798 Derivative Synopsis

Derivative	Ambient Temperature Range
SAK-TC1798F-512F300EL	T_A = -40°C to +125°C
SAK-TC1798F-512F300EP	T_A = -40°C to +125°C
SAK-TC1798N-512F300EP	T_A = -40°C to +125°C
SAK-TC1798S-512F300EP	T_A = -40°C to +125°C

2 System Overview of the TC1798

The TC1798 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1798 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1798 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1798 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1798 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1798, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Cross Bar Interconnect (SRI). Several I/O lines on the TC1798 ports are reserved for these peripheral units to communicate with the external world.

2.1 Block Diagram

Figure 1 shows the block diagram of the **SAK-TC1798S-512F300EP**.

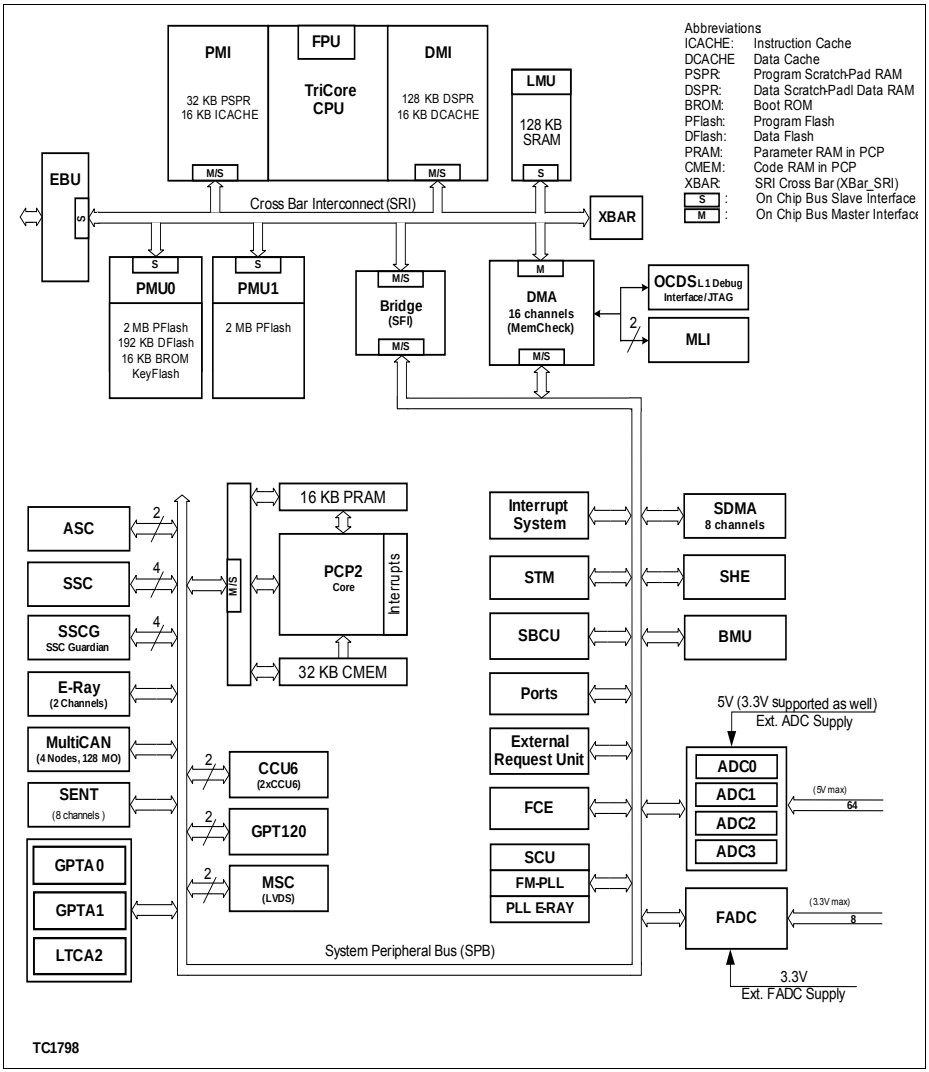


Figure 1 Block Diagram

Figure 1 shows the block diagram of the **SAK-TC1798F-512F300EL / SAK-TC1798F-512F300EP**.

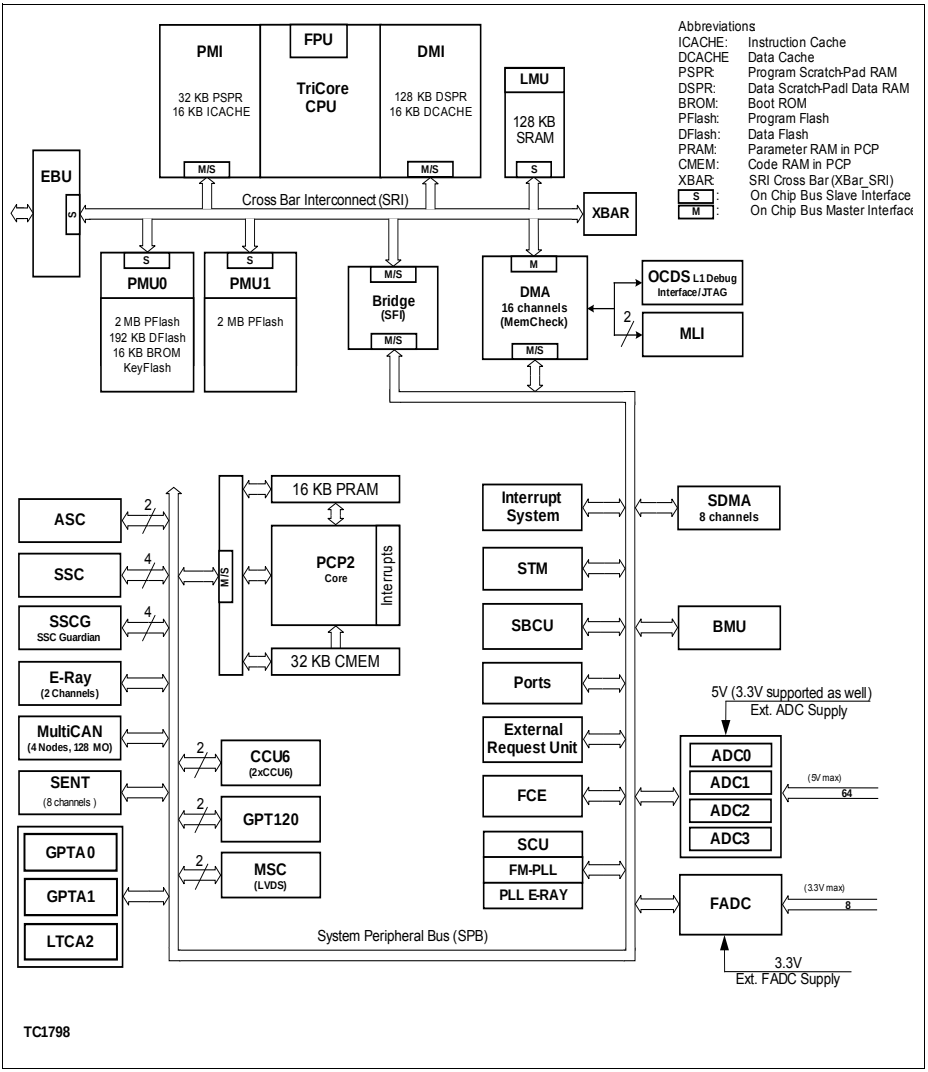


Figure 2 Block Diagram

Figure 1 shows the block diagram of the **SAK-TC1798N-512F300EP**.

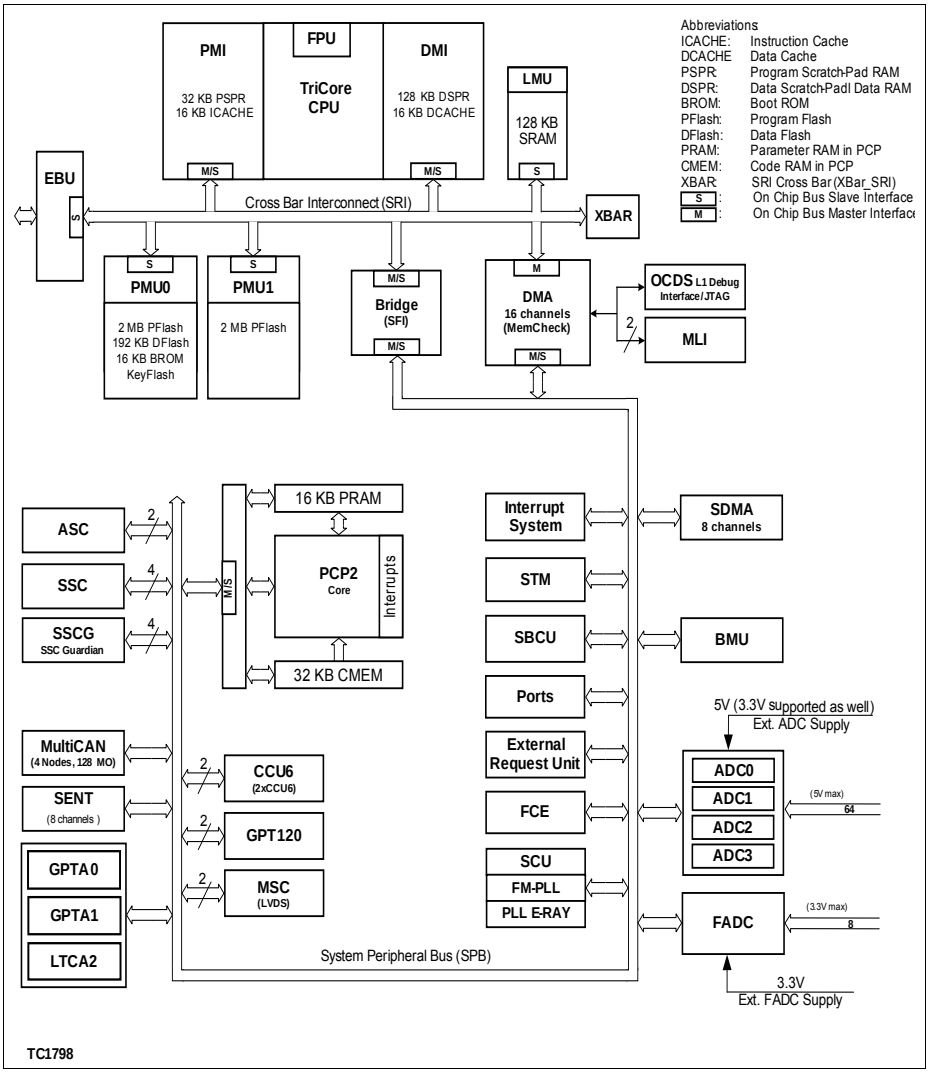


Figure 3 Block Diagram

3 Pinning

Figure 4 is showing the TC1798 Logic Symbol.

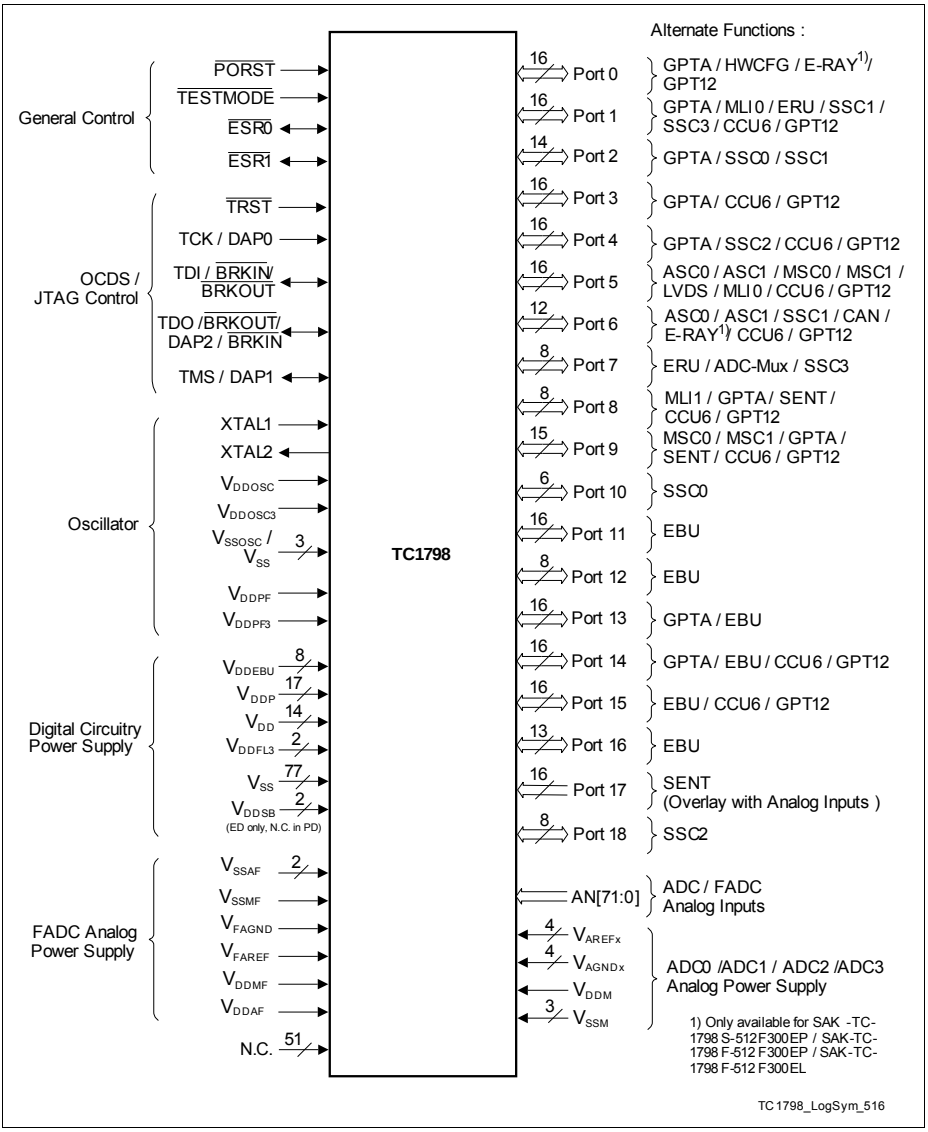


Figure 4 TC1798 Logic Symbol

3.1 TC1798 Pin Configuration

This chapter shows the pin configuration of the TC1798 package PG-LFBGA- 516.

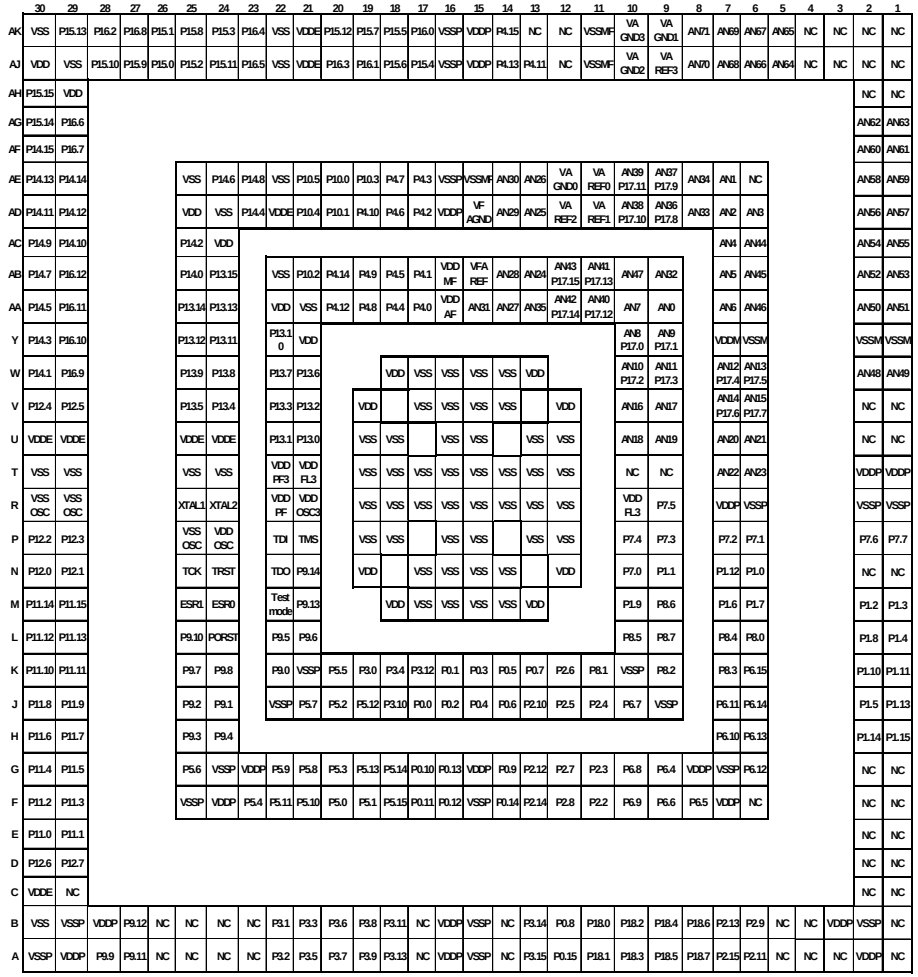


Figure 5 TC1798 Pinning for PG-LFBGA- 516 Package

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package)

Pin	Symbol	Ctrl.	Type	Function
Port 0				
J17	P0.0	I/O	A1+/ PU	**Port 0 General Purpose I/O Line 0**
	HWCFG0	I		**Hardware Configuration Input 0**
	OUT56	O1		**OUT56 Line of GPTA0**
	OUT56	O2		**OUT56 Line of GPTA1**
	OUT80	O3		**OUT80 Line of LTCA2**
K16	P0.1	I/O	A1/ PU	**Port 0 General Purpose I/O Line 1**
	HWCFG1	I		**Hardware Configuration Input 1**
	OUT57	O1		**OUT57 Line of GPTA0**
	OUT57	O2		**OUT57 Line of GPTA1**
	OUT81	O3		**OUT81 Line of LTCA2**
J16	P0.2	I/O	A2/ PU	**Port 0 General Purpose I/O Line 2**
	HWCFG2	I		**Hardware Configuration Input 2**
	OUT58	O1		**OUT58 Line of GPTA0**
	OUT58	O2		**OUT58 Line of GPTA1**
	OUT82	O3		**OUT82 Line of LTCA2**
K15	P0.3	I/O	A1/ PU	**Port 0 General Purpose I/O Line 3**
	HWCFG3	I		**Hardware Configuration Input 3**
	OUT59	O1		**OUT59 Line of GPTA0**
	OUT59	O2		**OUT59 Line of GPTA1**
	OUT83	O3		**OUT83 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
J15	P0.4	I/O	A1/ PU	**Port 0 General Purpose I/O Line 4**
	HWCFG4	I		**Hardware Configuration Input 4**
	OUT60	O1		**OUT60 Line of GPTA0**
	OUT60	O2		**OUT60 Line of GPTA1**
	EVTO0	O3		**MCDS Output Event 0**[1)]
K14	P0.5	I/O	A1/ PU	**Port 0 General Purpose I/O Line 5**
	HWCFG5	I		**Hardware Configuration Input 5**
	OUT61	O1		**OUT61 Line of GPTA0**
	OUT61	O2		**OUT61 Line of GPTA1**
	EVTO1	O3		**MCDS Output Event 1**[1)]
J14	P0.6	I/O	A2/ PU	**Port 0 General Purpose I/O Line 6**
	HWCFG6	I		**Hardware Configuration Input 6**
	OUT62	O1		**OUT62 Line of GPTA0**
	OUT62	O2		**OUT62 Line of GPTA1**
	EVTO2	O3		**MCDS Output Event 2**[1)]
K13	P0.7	I/O	A1/ PU	**Port 0 General Purpose I/O Line 7**
	HWCFG7	I		**Hardware Configuration Input 7**
	OUT63	O1		**OUT63 Line of GPTA0**
	OUT63	O2		**OUT63 Line of GPTA1**
	EVTO3	O3		**MCDS Output Event 3**[1)]
B12	P0.8	I/O	A1/ PU	**Port 0 General Purpose I/O Line 8**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
G14	P0.9	I/O	A1/ PU	**Port 0 General Purpose I/O Line 9**
	RXDA0	I		**E-Ray Channel A Receive Data Input 0** [2]
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
G17	P0.10	I/O	A2/ PU	**Port 0 General Purpose I/O Line 10**
	TXENA	O1		**E-Ray Channel A transmit Data Output enable** [2]
	Reserved	O2		-
	Reserved	O3		-
F17	P0.11	I/O	A2/ PU	**Port 0 General Purpose I/O Line 11**
	T5INB	I		**GPT120**
	T5INA	I		**GPT121**
	TXENB	O1		**E-Ray Channel B transmit Data Output enable** [2]
	Reserved	O2		-
	Reserved	O3		-
F16	P0.12	I/O	A2/ PU	**Port 0 General Purpose I/O Line 12**
	T5EUDA	I		**GPT120**
	T5EUDB	I		**GPT121**
	TXDB	O1		**E-Ray Channel B transmit Data Output** [2]
	Reserved	O2		-
	Reserved	O3		-

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
G16	P0.13	I/O	A1/ PU	**Port 0 General Purpose I/O Line 13**
	RXDB0	I		**E-Ray Channel B Receive Data Input 0** [2]
	T5EUDB	I		**GPT120**
	T5EUDA	I		**GPT121**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
F14	P0.14	I/O	A2/ PU	**Port 0 General Purpose I/O Line 14**
	T6INA	I		**GPT120**
	T6INB	I		**GPT121**
	TXDA	O1		**E-Ray Channel A transmit Data Output** [2]
	Reserved	O2		-
	Reserved	O3		-
A12	P0.15	I/O	A1/ PU	**Port 0 General Purpose I/O Line 15**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
Port 1				
N6	P1.0	I/O	A2/ PU	**Port 1 General Purpose I/O Line 0**
	REQ0	I		**External trigger Input 0**
	EXTCLK1	O1		**External Clock Output 1**
	Reserved	O2		-
	Reserved	O3		-

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
N9	P1.1	I/O	A1/ PU	**Port 1 General Purpose I/O Line 1**
	REQ1	I		**External trigger Input 1**
	CC60INA	I		**CCU60**
	CC60INB	I		**CCU61**
	CC60	O1		**CCU60**
	Reserved	O2		**-**
	Reserved	O3		**-**
M2	P1.2	I/O	A1/ PU	**Port 1 General Purpose I/O Line 2**
	REQ2	I		**External trigger Input 2**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
M1	P1.3	I/O	A1/ PU	**Port 1 General Purpose I/O Line 3**
	REQ3	I		**External trigger Input 3**
	TREADY0B	I		**MLI0 transmit Channel ready Input B**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
L1	P1.4	I/O	A2/ PU	**Port 1 General Purpose I/O Line 4**
	TCLK0	O1		**MLI0 transmit Channel Clock Output**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
J2	P1.5	I/O	A1/ PU	**Port 1 General Purpose I/O Line 35**
	TREADY0A	I		**MLI0 transmit Channel ready Input A**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
M7	P1.6	I/O	A2/ PU	**Port 1 General Purpose I/O Line 6**
	TVALID0A	O1		**MLI0 transmit Channel valid Output A**
	SLSO10	O2		**SSC1 Slave Select Output Line 10**
	COUT60	O3		**CCU60**
M6	P1.7	I/O	A2/ PU	**Port 1 General Purpose I/O Line 7**
	CC61INB	I		**CCU60**
	CC61INA	I		**CCU61**
	TData0	O1		**MLI0 transmit Channel Data Output**
	CC61	O2		**CCU61**
	T3OUT	O3		**GPT120**
L2	P1.8	I/O	A1/ PU	**Port 1 General Purpose I/O Line 8**
	RCLK0A	I		**MLI0 Receive Channel Clock Input A**
	OUT64	O1		**OUT64 Line of GPTA0**
	OUT64	O2		**OUT64 Line of GPTA1**
	OUT88	O3		**OUT88 Line of LTCA2**
M10	P1.9	I/O	A2/ PU	**Port 1 General Purpose I/O Line 9**
	RREADY0A	O1		**MLI0 Receive Channel ready Output A**
	SLSO11	O2		**SSC 1Slave Select Output Line 11**
	OUT65	O3		**OUT65 Line of GPTA0**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K2	P1.10	I/O	A1/ PU	**Port 1 General Purpose I/O Line 10**
	RVALID0A	I		**MLI0 Receive Channel valid Input A**
	OUT66	O1		**OUT66 Line of GPTA0**
	OUT66	O2		**OUT66 Line of GPTA1**
	OUT90	O3		**OUT90 Line of LTCA2**
K1	P1.11	I/O	A1/ PU	**Port 1 General Purpose I/O Line 11**
	RDATA0A	I		**MLI0 Receive Channel Data Input A**
	$\overline{\text{SLSI3}}$	I		**SSC3 Input**
	OUT67	O1		**OUT67 Line of GPTA0**
	OUT67	O2		**OUT67 Line of GPTA1**
	OUT91	O3		**OUT91 Line of LTCA2**
N7	P1.12	I/O	A2/ PU	**Port 1 General Purpose I/O Line 12**
	EXTCLK0	O1		**External Clock Output 0**
	OUT68	O2		**OUT68 Line of GPTA0**
	OUT68	O3		**OUT68 Line of GPTA1**
J1	P1.13	I/O	A1/ PU	**Port 1 General Purpose I/O Line 13**
	RCLK0B	I		**MLI0 Receive Channel Clock Input B**
	OUT69	O1		**OUT69 Line of GPTA0**
	OUT69	O2		**OUT69 Line of GPTA1**
	OUT93	O3		**OUT93 Line of LTCA2**
H2	P1.14	I/O	A1/ PU	**Port 1 General Purpose I/O Line 14**
	RVALID0B	I		**MLI0 Receive Channel valid Input B**
	OUT70	O1		**OUT70 Line of GPTA0**
	OUT70	O2		**OUT70 Line of GPTA1**
	OUT94	O3		**OUT94 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
H1	P1.15	I/O	A1/ PU	**Port 1 General Purpose I/O Line 15**
	RDATA0B	I		**MLI0 Receive Channel Data Input B**
	OUT71	O1		**OUT71 Line of GPTA0**
	OUT71	O2		**OUT71 Line of GPTA1**
	OUT95	O3		**OUT95 Line of LTCA2**
Port 2				
F11	P2.2	I/O	A1+/ PU	**Port 2 General Purpose I/O Line 2**
	SLSO02	O1		**SSC0 Slave Select Output Line 2**
	SLSO12	O2		**SSC1 Slave Select Output Line 12**
	SLSO02 AND SLSO12	O3		**SSC0 & SSC1 Slave Select Output Line 2 AND Slave Select Output Line 12**
G11	P2.3	I/O	A1+/ PU	**Port 2 General Purpose I/O Line 3**
	SLSO03	O1		**SSC0 Slave Select Output Line 3**
	SLSO13	O2		**SSC1 Slave Select Output Line 13**
	SLSO03 AND SLSO13	O3		**SSC0 & SSC1 Slave Select Output Line 3 AND Slave Select Output Line 13**
J11	P2.4	I/O	A1+/ PU	**Port 2 General Purpose I/O Line 4**
	SLSO04	O1		**SSC0 Slave Select Output Line 4**
	SLSO14	O2		**SSC1 Slave Select Output Line 14**
	SLSO04 AND SLSO14	O3		**SSC0 & SSC1 Slave Select Output Line 4 AND Slave Select Output Line 14**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
J12	P2.5	I/O	A1+/ PU	**Port 2 General Purpose I/O Line 5**
	SLSO05	O1		**SSC0 Slave Select Output Line 5**
	SLSO15	O2		**SSC1 Slave Select Output Line 15**
	SLSO05 AND SLSO15	O3		**SSC0 & SSC1 Slave Select Output Line 5 AND Slave Select Output Line 15**
K12	P2.6	I/O	A1+/ PU	**Port 2 General Purpose I/O Line 6**
	SLSO06	O1		**SSC0 Slave Select Output Line 6**
	SLSO16	O2		**SSC1 Slave Select Output Line 16**
	SLSO06 AND SLSO16	O3		**SSC0 & SSC1 Slave Select Output Line 6 AND Slave Select Output Line 16**
G12	P2.7	I/O	A1+/ PU	**Port 2 General Purpose I/O Line 7**
	SLSO07	O1		**SSC0 Slave Select Output Line 7**
	SLSO17	O2		**SSC0 Slave Select Output Line 17**
	SLSO07 AND SLSO17	O3		**SSC0 & SSC1 Slave Select Output Line 7AND Slave Select Output Line 17**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
F12	P2.8	I/O	A1/ PU	**Port 2 General Purpose I/O Line 8**
	IN0	I		**IN0 Line of GPTA0**
	IN0	I		**IN0 Line of GPTA1**
	IN0	I		**IN0 Line of LTCA2**
	CCPOS0A	I		**CCU62**
	T12HRB	I		**CCU63**
	T3INB	I		**GPT120**
	T3INA	I		**GPT121**
	OUT0	O1		**OUT0 Line of GPTA0**
	OUT0	O2		**OUT0 Line of GPTA1**
	OUT0	O3		**OUT0 Line of LTCA2**
B6	P2.9	I/O	A1/ PU	**Port 2 General Purpose I/O Line 9**
	IN1	I		**IN1 Line of GPTA0**
	IN1	I		**IN1 Line of GPTA1**
	IN1	I		**IN1 Line of LTCA2**
	OUT1	O1		**OUT1 Line of GPTA0**
	OUT1	O2		**OUT1 Line of GPTA1**
	OUT1	O3		**OUT1 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
J13	P2.10	I/O	A1/ PU	**Port 2 General Purpose I/O Line 10**
	IN2	I		**IN2 Line of GPTA0**
	IN2	I		**IN2 Line of GPTA1**
	IN2	I		**IN2 Line of LTCA2**
	T12HRE	I		**CCU60**
	CC61INC	I		**CCU60**
	CTRAPA	I		**CCU61**
	CC60INC	I		**CCU61**
	CTRAPB	I		**CCU63**
	OUT2	O1		**OUT2 Line of GPTA0**
	OUT2	O2		**OUT2 Line of GPTA1**
	OUT2	O3		**OUT2 Line of LTCA2**
A6	P2.11	I/O	A1/ PU	**Port 2 General Purpose I/O Line 11**
	IN3	I		**IN3 Line of GPTA0**
	IN3	I		**IN3 Line of GPTA1**
	IN3	I		**IN3 Line of LTCA2**
	OUT3	O1		**OUT3 Line of GPTA0**
	OUT3	O2		**OUT3 Line of GPTA1**
	OUT3	O3		**OUT3 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
G13	P2.12	I/O	A1/ PU	**Port 2 General Purpose I/O Line 12**
	IN4	I		**IN4 Line of GPTA0**
	IN4	I		**IN4 Line of GPTA1**
	IN4	I		**IN4 Line of LTCA2**
	T12HRB	I		**CCU62**
	CCPOS0A	I		**CCU63**
	T2INB	I		**GPT120**
	T2INA	I		**GPT121**
	OUT4	O1		**OUT4 Line of GPTA0**
	OUT4	O2		**OUT4 Line of GPTA1**
	OUT4	O3		**OUT4 Line of LTCA2**
B7	P2.13	I/O	A1/ PU	**Port 2 General Purpose I/O Line 13**
	IN5	I		**IN5 Line of GPTA0**
	IN5	I		**IN5 Line of GPTA1**
	IN5	I		**IN5 Line of LTCA2**
	OUT5	O1		**OUT5 Line of GPTA0**
	OUT5	O2		**OUT5 Line of GPTA1**
	OUT5	O3		**OUT5 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
F13	P2.14	I/O	A1/ PU	**Port 2 General Purpose I/O Line 14**
	IN6	I		**IN6 Line of GPTA0**
	IN6	I		**IN6 Line of GPTA1**
	IN6	I		**IN6 Line of LTCA2**
	CCPOS0A	I		**CCU60**
	T12HRB	I		**CCU61**
	T3INA	I		**GPT120**
	T3INB	I		**GPT121**
	OUT6	O1		**OUT6 Line of GPTA0**
	OUT6	O2		**OUT6 Line of GPTA1**
	OUT6	O3		**OUT6 Line of LTCA2**
A7	P2.15	I/O	A1/ PU	**Port 2 General Purpose I/O Line 15**
	IN7	I		**IN7 Line of GPTA0**
	IN7	I		**IN7 Line of GPTA1**
	IN7	I		**IN7 Line of LTCA2**
	OUT7	O1		**OUT7 Line of GPTA0**
	OUT7	O2		**OUT7 Line of GPTA1**
	OUT7	O3		**OUT7 Line of LTCA2**
Port 3				

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K19	P3.0	I/O	A1/ PU	**Port 3 General Purpose I/O Line 0**
	IN8	I		**IN8 Line of GPTA0**
	IN8	I		**IN8 Line of GPTA1**
	IN8	I		**IN8 Line of LTCA2**
	CTRAPA	I		**CCU62**
	CTRPAB	I		**CCU61**
	CC60INC	I		**CCU61**
	T12HRE	I		**CCU63**
	CC61INC	I		**CCU63**
	T5INA	I		**GPT120**
	T5INB	I		**GPT121**
	OUT8	O1		**OUT8 Line of GPTA0**
	OUT8	O2		**OUT8 Line of GPTA1**
	OUT8	O3		**OUT8 Line of LTCA2**
B22	P3.1	I/O	A1/ PU	**Port 3 General Purpose I/O Line 1**
	IN9	I		**IN9 Line of GPTA0**
	IN9	I		**IN9 Line of GPTA1**
	IN9	I		**IN9 Line of LTCA2**
	OUT9	O1		**OUT9 Line of GPTA0**
	OUT9	O2		**OUT9 Line of GPTA1**
	OUT9	O3		**OUT9 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A22	P3.2	I/O	A1/ PU	**Port 3 General Purpose I/O Line 2**
	IN10	I		**IN10 Line of GPTA0**
	IN10	I		**IN10 Line of GPTA1**
	IN10	I		**IN10 Line of LTCA2**
	T13HRE	I		**CCU63**
	OUT10	O1		**OUT10 Line of GPTA0**
	OUT10	O2		**OUT10 Line of GPTA1**
	OUT10	O3		**OUT10 Line of LTCA2**
B21	P3.3	I/O	A1/ PU	**Port 3 General Purpose I/O Line 3**
	IN11	I		**IN11 Line of GPTA0**
	IN11	I		**IN11 Line of GPTA1**
	IN11	I		**IN11 Line of LTCA2**
	OUT11	O1		**OUT11 Line of GPTA0**
	OUT11	O2		**OUT11 Line of GPTA1**
	OUT11	O3		**OUT11 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K18	P3.4	I/O	A1/ PU	**Port 3 General Purpose I/O Line 4**
	IN12	I		**IN12 Line of GPTA0**
	IN12	I		**IN12 Line of GPTA1**
	IN12	I		**IN12 Line of LTCA2**
	T12HRE	I		**CCU62**
	CC61INC	I		**CCU62**
	CTRAPA	I		**CCU63**
	CTRAPB	I		**CCU60**
	CC60INC	I		**CCU63**
	OUT12	O1		**OUT12 Line of GPTA0**
	OUT12	O2		**OUT12 Line of GPTA1**
	OUT12	O3		**OUT12 Line of LTCA2**
A21	P3.5	I/O	A1/ PU	**Port 3 General Purpose I/O Line 5**
	IN13	I		**IN13 Line of GPTA0**
	IN13	I		**IN13 Line of GPTA1**
	IN13	I		**IN13 Line of LTCA2**
	OUT13	O1		**OUT13 Line of GPTA0**
	OUT13	O2		**OUT13 Line of GPTA1**
	OUT13	O3		**OUT13 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B20	P3.6	I/O	A1/ PU	**Port 3 General Purpose I/O Line 6**
	IN14	I		**IN14 Line of GPTA0**
	IN14	I		**IN14 Line of GPTA1**
	IN14	I		**IN14 Line of LTCA2**
	T13HRE	I		**CCU62**
	T6EUDB	I		**GPT120**
	T6EUDA	I		**GPT121**
	OUT14	O1		**OUT14 Line of GPTA0**
	OUT14	O2		**OUT14 Line of GPTA1**
	OUT14	O3		**OUT14 Line of LTCA2**
A20	P3.7	I/O	A1/ PU	**Port 3 General Purpose I/O Line 7**
	IN15	I		**IN15 Line of GPTA0**
	IN15	I		**IN15 Line of GPTA1**
	IN15	I		**IN15 Line of LTCA2**
	OUT15	O1		**OUT15 Line of GPTA0**
	OUT15	O2		**OUT15 Line of GPTA1**
	OUT15	O3		**OUT15 Line of LTCA2**
B19	P3.8	I/O	A1/ PU	**Port 3 General Purpose I/O Line 8**
	IN16	I		**IN16 Line of GPTA0**
	IN16	I		**IN16 Line of GPTA1**
	IN16	I		**IN16 Line of LTCA2**
	T13HRE	I		**CCU61**
	OUT16	O1		**OUT16 Line of GPTA0**
	OUT16	O2		**OUT16 Line of GPTA1**
	OUT16	O3		**OUT16 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A19	P3.9	I/O	A1/ PU	**Port 3 General Purpose I/O Line 9**
	IN17	I		**IN17 Line of GPTA0**
	IN17	I		**IN17 Line of GPTA1**
	IN17	I		**IN17 Line of LTCA2**
	OUT17	O1		**OUT17 Line of GPTA0**
	OUT17	O2		**OUT17 Line of GPTA1**
	OUT17	O3		**OUT17 Line of LTCA2**
J18	P3.10	I/O	A1+/ PU	**Port 3 General Purpose I/O Line 10**
	IN18	I		**IN18 Line of GPTA0**
	IN18	I		**IN18 Line of GPTA1**
	IN18	I		**IN18 Line of LTCA2**
	CCPOS1A	I		**CCU62**
	T13HRB	I		**CCU63**
	T3EUDB	I		**GPT120**
	T3EUDA	I		**GPT121**
	OUT18	O1		**OUT18 Line of GPTA0**
	OUT18	O2		**OUT18 Line of GPTA1**
	OUT18	O3		**OUT18 Line of LTCA2**
B18	P3.11	I/O	A1/ PU	**Port 3 General Purpose I/O Line 11**
	IN19	I		**IN19 Line of GPTA0**
	IN19	I		**IN19 Line of GPTA1**
	IN19	I		**IN19 Line of LTCA2**
	OUT19	O1		**OUT19 Line of GPTA0**
	OUT19	O2		**OUT19 Line of GPTA1**
	OUT19	O3		**OUT19 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K17	P3.12	I/O	A1/ PU	**Port 3 General Purpose I/O Line 12**
	IN20	I		**IN20 Line of GPTA0**
	IN20	I		**IN20 Line of GPTA1**
	IN20	I		**IN20 Line of LTCA2**
	CCPOS2A	I		**CCU62**
	T12HRC	I		**CCU63**
	T13HRC	I		**CCU63**
	T4INB	I		**GPT120**
	T4INA	I		**GPT121**
	OUT20	O1		**OUT20 Line of GPTA0**
	OUT20	O2		**OUT20 Line of GPTA1**
	OUT20	O3		**OUT20 Line of LTCA2**
A18	P3.13	I/O	A1/ PU	**Port 3 General Purpose I/O Line 13**
	IN21	I		**IN21 Line of GPTA0**
	IN21	I		**IN21 Line of GPTA1**
	IN21	I		**IN21 Line of LTCA2**
	OUT21	O1		**OUT21 Line of GPTA0**
	OUT21	O2		**OUT21 Line of GPTA1**
	OUT21	O3		**OUT21 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B13	P3.14	I/O	A1/ PU	**Port 3 General Purpose I/O Line 14**
	IN22	I		**IN22 Line of GPTA0**
	IN22	I		**IN22 Line of GPTA1**
	IN22	I		**IN22 Line of LTCA2**
	T13HRE	I		**CCU63**
	OUT22	O1		**OUT22 Line of GPTA0**
	OUT22	O2		**OUT22 Line of GPTA1**
	OUT22	O3		**OUT22 Line of LTCA2**
A13	P3.15	I/O	A1/ PU	**Port 3 General Purpose I/O Line 15**
	IN23	I		**IN23 Line of GPTA0**
	IN23	I		**IN23 Line of GPTA1**
	IN23	I		**IN23 Line of LTCA2**
	OUT23	O1		**OUT23 Line of GPTA0**
	OUT23	O2		**OUT23 Line of GPTA1**
	OUT23	O3		**OUT23 Line of LTCA2**
Port 4				
AA17	P4.0	I/O	A1+/ PU	**Port 4 General Purpose I/O Line 0**
	IN24	I		**IN24 Line of GPTA0**
	IN24	I		**IN24 Line of GPTA1**
	IN24	I		**IN24 Line of LTCA2**
	MRST2A	I		**SSC2 Master Receive Input A (Master Mode)**
	OUT24	O1		**OUT24 Line of GPTA0**
	OUT24	O2		**OUT24 Line of GPTA1**
	MRST2	O3		**SSC2 Slave Transmit Output (Slave Mode)**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AB17	P4.1	I/O	A1+/ PU	**Port 4 General Purpose I/O Line 1**
	IN25	I		**IN25 Line of GPTA0**
	IN25	I		**IN25 Line of GPTA1**
	IN25	I		**IN25 Line of LTCA2**
	MTSR2A	I		**SSC2 Slave Receive Input A (Slave Mode)**
	MRSTG2A	I		**SSC Guardian 2 Master Receive Input A (Master Mode)**
	OUT25	O1		**OUT25 Line of GPTA0**
	OUT25	O2		**OUT25 Line of GPTA1**
	MTSR2	O3		**SSC2 Master Transmit Output (Master Mode)[3)]**
AD17	P4.2	I/O	A1+/ PU	**Port 4 General Purpose I/O Line 2**
	IN26	I		**IN26 Line of GPTA0**
	IN26	I		**IN26 Line of GPTA1**
	IN26	I		**IN26 Line of LTCA2**
	SCLK2	I		**SSC2 Input**
	OUT26	O1		**OUT26 Line of GPTA0**
	OUT26	O2		**OUT26 Line of GPTA1**
	SCLK2	O3		**SSC2 Output**
AE17	P4.3	I/O	A1+/ PU	**Port 4 General Purpose I/O Line 3**
	IN27	I		**IN27 Line of GPTA0**
	IN27	I		**IN27 Line of GPTA1**
	IN27	I		**IN27 Line of LTCA2**
	OUT27	O1		**OUT27 Line of GPTA0**
	OUT27	O2		**OUT27 Line of GPTA1**
	SLSO20	O3		**SSC2 Output**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AA18	P4.4	I/O	A1+/ PU	**Port 4 General Purpose I/O Line 4**
	IN28	I		**IN28 Line of GPTA0**
	IN28	I		**IN28 Line of GPTA1**
	IN28	I		**IN28 Line of LTCA2**
	OUT28	O1		**OUT28 Line of GPTA0**
	OUT28	O2		**OUT28 Line of GPTA1**
	SLSO21	O3		**SSC2 Output**
AB18	P4.5	I/O	A1+/ PU	**Port 4 General Purpose I/O Line 5**
	IN29	I		**IN29 Line of GPTA0**
	IN29	I		**IN29 Line of GPTA1**
	IN29	I		**IN29 Line of LTCA2**
	OUT29	O1		**OUT29 Line of GPTA0**
	OUT29	O2		**OUT29 Line of GPTA1**
	SLSO22	O3		**SSC2 Output**
AD18	P4.6	I/O	A1+/ PU	**Port 4 General Purpose I/O Line 6**
	IN30	I		**IN30 Line of GPTA0**
	IN30	I		**IN30 Line of GPTA1**
	IN30	I		**IN30 Line of LTCA2**
	OUT30	O1		**OUT30 Line of GPTA0**
	OUT30	O2		**OUT30 Line of GPTA1**
	SLSO23	O3		**SSC2 Output**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AE18	P4.7	I/O	A1+/ PU	**Port 4 General Purpose I/O Line 7**
	IN31	I		**IN31 Line of GPTA0**
	IN31	I		**IN31 Line of GPTA1**
	IN31	I		**IN31Line of LTCA2**
	T6INB	I		**GPT120**
	T6INA	I		**GPT121**
	OUT31	O1		**OUT31 Line of GPTA0**
	OUT31	O2		**OUT31 Line of GPTA1**
	SLSO24	O3		**SSC2 Output**
AA19	P4.8	I/O	A1/ PU	**Port 4 General Purpose I/O Line 8**
	IN32	I		**IN32 Line of GPTA0**
	IN32	I		**IN32 Line of GPTA1**
	CCPOS1A	I		**CCU60**
	T13HRB	I		**CCU61**
	T3EUDA	I		**GPT120**
	T3EUDB	I		**GPT121**
	OUT32	O1		**OUT32 Line of GPTA0**
	OUT32	O2		**OUT32 Line of GPTA1**
	OUT0	O3		**OUT0 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AB19	P4.9	I/O	A1/ PU	**Port 4 General Purpose I/O Line 9**
	IN33	I		**IN33 Line of GPTA0**
	IN33	I		**IN33 Line of GPTA1**
	CCPOS2A	I		**CCU60**
	T12HRC	I		**CCU61**
	T13HRC	I		**CCU61**
	T4INA	I		**GPT120**
	T4INB	I		**GPT121**
	$\overline{\text{SLSI2}}$	I		**SSC2**
	OUT33	O1		**OUT33 Line of GPTA0**
	OUT33	O2		**OUT33 Line of GPTA1**
	OUT1	O3		**OUT1 Line of LTCA2**
AD19	P4.10	I/O	A1/ PU	**Port 4 General Purpose I/O Line 10**
	IN34	I		**IN34 Line of GPTA0**
	IN34	I		**IN34 Line of GPTA1**
	T12HRB	I		**CCU60**
	CCPOS0A	I		**CCU61**
	T2INA	I		**GPT120**
	T2INB	I		**GPT121**
	OUT34	O1		**OUT34 Line of GPTA0**
	OUT34	O2		**OUT34 Line of GPTA1**
	OUT2	O3		**OUT2 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AJ13	P4.11	I/O	A1/ PU	**Port 4 General Purpose I/O Line 11**
	IN35	I		**IN35 Line of GPTA0**
	IN35	I		**IN35 Line of GPTA1**
	OUT35	O1		**OUT35 Line of GPTA0**
	OUT35	O2		**OUT35 Line of GPTA1**
	OUT3	O3		**OUT3 Line of LTCA2**
AA20	P4.12	I/O	A1/ PU	**Port 4 General Purpose I/O Line 12**
	IN36	I		**IN36 Line of GPTA0**
	IN36	I		**IN36 Line of GPTA1**
	T13HRB	I		**CCU60**
	CCPOS1A	I		**CCU61**
	T2EUDA	I		**GPT120**
	T2EUDB	I		**GPT121**
	OUT36	O1		**OUT36 Line of GPTA0**
	OUT36	O2		**OUT36 Line of GPTA1**
	OUT4	O3		**OUT4 Line of LTCA2**
AJ14	P4.13	I/O	A1/ PU	**Port 4 General Purpose I/O Line 13**
	IN37	I		**IN37 Line of GPTA0**
	IN37	I		**IN37 Line of GPTA1**
	OUT37	O1		**OUT37 Line of GPTA0**
	OUT37	O2		**OUT37 Line of GPTA1**
	OUT5	O3		**OUT5 Line of LTCA2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AB20	P4.14	I/O	A1/ PU	**Port 4 General Purpose I/O Line 14**
	IN38	I		**IN38 Line of GPTA0**
	IN38	I		**IN38 Line of GPTA1**
	T12HRC	I		**CCU60**
	T13HRC	I		**CCU60**
	CCPOS2A	I		**CCU61**
	T4EUDA	I		**GPT120**
	T4EUDB	I		**GPT121**
	OUT38	O1		**OUT38 Line of GPTA0**
	OUT38	O2		**OUT38 Line of GPTA1**
	OUT6	O3		**OUT6 Line of LTCA2**
AK14	P4.15	I/O	A1/ PU	**Port 4 General Purpose I/O Line 15**
	IN39	I		**IN39 Line of GPTA0**
	IN39	I		**IN39 Line of GPTA1**
	OUT39	O1		**OUT39 Line of GPTA0**
	OUT39	O2		**OUT39 Line of GPTA1**
	OUT7	O3		**OUT7 Line of LTCA2**
Port 5				
F20	P5.0	I/O	A1+/ PU	**Port 5 General Purpose I/O Line 0**
	RXD0A	I		**ASC0 Receiver Input/Output A**
	T6EUDA	I		**GPT120**
	T6EUDB	I		**GPT121**
	RXD0A	O1		**ASC0 Receiver Input/Output A**
	OUT72	O2		**OUT72 Line of GPTA0**
	OUT72	O3		**OUT72 Line of GPTA1**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
F19	P5.1	I/O	A1+/ PU	**Port 5 General Purpose I/O Line 1**
	TXD0	O1		**ASC0 Transmitter Output A**
	OUT73	O2		**OUT73 Line of GPTA0**
	OUT73	O3		**OUT73 Line of GPTA1**
J20	P5.2	I/O	A2/ PU	**Port 5 General Purpose I/O Line 2**
	RXD1A	I		**ASC1 Receiver Input/Output A**
	RXD1A	O1		**ASC1 Receiver Input/Output A**
	OUT74	O2		**OUT74 Line of GPTA0**
	OUT74	O3		**OUT74 Line of GPTA1**
G20	P5.3	I/O	A1+/ PU	**Port 5 General Purpose I/O Line 3**
	TXD1	O1		**ASC1 Transmitter Output A**
	OUT75	O2		**OUT75 Line of GPTA0**
	OUT75	O3		**OUT75 Line of GPTA1**
F23	P5.4	I/O	A2/ PU	**Port 5 General Purpose I/O Line 4**
	T13HRB	I		**CCU62**
	CCPOS1A	I		**CCU63**
	T2EUDB	I		**GPT120**
	T2EUDA	I		**GPT121**
	EN00	O1		**MSC0 Device Select Output 0**
	RREADY0B	O2		**MLI0 Receive Channel ready Output B**
	OUT76	O3		**OUT76 Line of GPTA0**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K20	P5.5	I/O	A1+/ PU	**Port 5 General Purpose I/O Line 5**
	SDI0	I		**MSC0 Serial Data Input**
	T12HRC	I		**CCU62**
	T13HRC	I		**CCU62**
	CCPOS2A	I		**CCU63**
	T4EUDB	I		**GPT120**
	T4EUDA	I		**GPT121**
	OUT77	O1		**OUT77 Line of GPTA0**
	OUT77	O2		**OUT77 Line of GPTA1**
	OUT101	O3		**OUT101 Line of LTCA2**
G25	P5.6	I/O	A2/ PU	**Port 5 General Purpose I/O Line 6**
	CC60INA	I		**CCU62**
	CC60INB	I		**CCU63**
	EN10	O1		**MSC1 Device Select Output 0**
	TVALID0B	O2		**MLI0 transmit Channel valid Output B**
	CC60	O3		**CCU62**
J21	P5.7	I/O	A1+/ PU	**Port 5 General Purpose I/O Line 7**
	SDI1	I		**MSC1 Serial Data Input**
	CC61INA	I		**CCU62**
	CC61INB	I		**CCU63**
	OUT79	O1		**OUT79 Line of GPTA0**
	OUT79	O2		**OUT79 Line of GPTA1**
	CC61	O3		**CCU62**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
G21	P5.8	I/O	F/ PU	**Port 5 General Purpose I/O Line 8**
	CC62INA	I		**CCU62**
	CC62INB	I		**CCU63**
	SON0	O1		**MSC0 Differential Driver Serial Data Output Negative**
	OUT80	O2		**OUT80 Line of GPTA0**
	CC62	O3		**CCU62**
G22	P5.9	I/O	F/ PU	**Port 5 General Purpose I/O Line 9**
	SOP0A	O1		**MSC0 Differential Driver Serial Data Output Positive A**
	OUT81	O2		**OUT81 Line of GPTA0**
	COUT60	O3		**CCU62**
F21	P5.10	I/O	F/ PU	**Port 5 General Purpose I/O Line 10**
	FCLN0	O1		**MSC0 Differential Driver Clock Output Negative**
	OUT82	O2		**OUT82 Line of GPTA0**
	COUT61	O3		**CCU62**
F22	P5.11	I/O	F/ PU	**Port 5 General Purpose I/O Line 11**
	FCLP0A	O1		**MSC0 Differential Driver Clock Output Positive A**
	OUT83	O2		**OUT83 Line of GPTA0**
	COUT62	O3		**CCU62**
J19	P5.12	I/O	F/ PU	**Port 5 General Purpose I/O Line 12**
	SON1	O1		**MSC1 Differential Driver Serial Data Output Negative**
	OUT84	O2		**OUT84 Line of GPTA0**
	OUT84	O3		**OUT84 Line of GPTA1**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
G19	P5.13	I/O	F/ PU	**Port 5 General Purpose I/O Line 13**
	SOP1A	O1		**MSC1 Differential Driver Serial Data Output Positive A**
	OUT85	O2		**OUT85 Line of GPTA0**
	OUT85	O3		**OUT85 Line of GPTA1**
G18	P5.14	I/O	F/ PU	**Port 5 General Purpose I/O Line 14**
	FCLN1	O1		**MSC1 Differential Driver Clock Output Negative**
	OUT86	O2		**OUT86 Line of GPTA0**
	OUT86	O3		**OUT86 Line of GPTA1**
F18	P5.15	I/O	F/ PU	**Port 5 General Purpose I/O Line 15**
	FCLNP1A	O1		**MSC1 Differential Driver Clock Output Positive A**
	OUT87	O2		**OUT87 Line of GPTA0**
	OUT87	O3		**OUT87 Line of GPTA1**
Port 6				
G9	P6.4	I/O	A1+/ PU	**Port 6 General Purpose I/O Line 4**
	MTSR1	I		**SSC1 Slave Receive Input (Slave Mode)**
	MRSTG1	I		**SSC Guardian 1 Master Receive Input (Master Mode)**
	MTSR1	O1		**SSC1 Master Transmit Output (Master Mode)[3)]**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
F8	P6.5	I/O	A1+/ PU	**Port 6 General Purpose I/O Line 5**
	MRST1	I		**SSC1 Master Receive Input (Master Mode)**
	MRST1	O1		**SSC1 Slave Transmit Output (Slave Mode)**
	Reserved	O2		**-**
	Reserved	O3		**-**
F9	P6.6	I/O	A1+/ PU	**Port 6 General Purpose I/O Line 6**
	SCLK1	I		**SSC1 Clock Input/Output**
	SCLK1	O1		**SSC1 Clock Input/Output**
	Reserved	O2		**-**
	Reserved	O3		**-**
J10	P6.7	I/O	A1+/ PU	**Port 6 General Purpose I/O Line 7**
	SLSI1	I		**SSC1 slave Select Input**
	T6OFL	O1		**GPT120**
	Reserved	O2		**-**
	Reserved	O3		**-**
G10	P6.8	I/O	A2/ PU	**Port 6 General Purpose I/O Line 8**
	RXDCAN0	I		**CAN Node 0 Receiver Input 0** **CAN Node 3 Receiver Input 1**
	RXD0B	I		**ASC0 Receiver Input/Output B**
	CAPINB	I		**GPT120**
	CAPINA	I		**GPT121**
	Reserved	O1		**-**
	RXD0B	O2		**ASC0 Receiver Input/Output B**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
F10	P6.9	I/O	A2/ PU	**Port 6 General Purpose I/O Line 9**
	TXDCAN0	O1		**CAN Node 0 Transmitter Output**
	TXD0	O2		**ASC0 Transmitter Output B**
	T60FL	O3		**GPT120**
H7	P6.10	I/O	A2/ PU	**Port 6 General Purpose I/O Line 10**
	RXDCAN1	I		**CAN Node 1 Receiver Input 0** **CAN Node 0 Receiver Input 1**
	RXD1B	I		**ASC1 Receiver Input/Output B**
	Reserved	O1		**-**
	RXD1B	O2		**ASC1 Receiver Input/Output B**
	TXENA	O3		**E-Ray Channel A transmit Data Output enable** [2]
J7	P6.11	I/O	A2/ PU	**Port 6 General Purpose I/O Line 11**
	TXDCAN1	O1		**CAN Node 1 Transmitter Output**
	TXD1	O2		**ASC1 Transmitter Output B**
	TXENB	O3		**E-Ray Channel B transmit Data Output enable** [2]
G6	P6.12	I/O	A1/ PU	**Port 6 General Purpose I/O Line 12**
	RXDCAN2	I		**CAN Node 2 Receiver Input 0** **CAN Node 1 Receiver Input 1**
	RXDA1	I		**E-Ray Channel A Receive Data Input 1** [2]
	Reserved	O1		**-**
	Reserved	O2		**-**
	COUT61	O3		**CCU60**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
H6	P6.13	I/O	A2/ PU	**Port 6 General Purpose I/O Line 13**
	TXDCAN2	O1		**CAN Node 2 Transmitter Output**
	TXDA	O2		**E-Ray Channel A transmit Data Output** [2]
	COUT62	O3		**CCU60**
J6	P6.14	I/O	A1/ PU	**Port 6 General Purpose I/O Line 14**
	RXDCAN3	I		**CAN Node 3 Receiver Input 0** **CAN Node 2 Receiver Input 1**
	RXDB1	I		**E-Ray Channel B Receive Data Input 1** [2]
	Reserved	O1		**-**
	Reserved	O2		**-**
	COUT63	O3		**CCU60**
K6	P6.15	I/O	A2/ PU	**Port 6 General Purpose I/O Line 15**
	CC60INB	I		**CCU60**
	CC60INA	I		**CCU61**
	TXDCAN3	O1		**CAN Node 3 Transmitter Output**
	TXDB	O2		**E-Ray Channel B transmit Data Output** [2]
	CC60	O3		**CCU61**
Port 7				
N10	P7.0	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 0**
	MRST3	I		**SSC3 Master Receive Input (Master Mode)**
	REQ4	I		**External trigger Input 4**
	AD2EMUX2	O1		**ADC2 external multiplexer Control Output 2**
	MRST3	O2		**SSC3 Slave Transmit Output (Slave Mode)**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
P6	P7.1	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 1**
	REQ5	I		**External trigger Input 5**
	MTSR3	I		**SSC3 Slave Receive Input (Master Mode)**
	MRSTG3B	I		**SSC Guardian 3 Master Receive Input B (Master Mode)**
	AD0EMUX2	O1		**ADC0 external multiplexer Control Output 2**
	MTSR3	O2		**SSC3 Master Transmit Output (Master Mode)[3)]**
	Reserved	O3		**-**
P7	P7.2	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 2**
	SCLK3	I		**SSC3 Input**
	AD0EMUX0	O1		**ADC0 external multiplexer Control Output 0**
	SCLK3	O2		**SSC3 Output**
	Reserved	O3		**-**
P9	P7.3	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 3**
	AD0EMUX1	O1		**ADC0 external multiplexer Control Output 1**
	SLSO30	O2		**SSC3 Output**
	Reserved	O3		**-**
P10	P7.4	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 4**
	REQ6	I		**External trigger Input 6**
	AD2EMUX0	O1		**ADC2 external multiplexer Control Output 0**
	SLSO31	O2		**SSC3 Output**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
R9	P7.5	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 5**
	REQ7	I		**External trigger Input 7**
	AD2EMUX1	O1		**ADC2 external multiplexer Control Output 1**
	SLSO32	O2		**SSC3 Output**
	Reserved	O3		**-**
P2	P7.6	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 6**
	AD1EMUX0	O1		**ADC1 external multiplexer Control Output 0**
	SLSO33	O2		**SSC3 Output**
	Reserved	O3		**-**
P1	P7.7	I/O	A1+/ PU	**Port 7 General Purpose I/O Line 7**
	AD1EMUX1	O1		**ADC1 external multiplexer Control Output 1**
	SLSO34	O2		**SSC3 Output**
	Reserved	O3		**-**
Port 8				
L6	P8.0	I/O	A2/ PU	**Port 8 General Purpose I/O Line 0**
	IN40	I		**IN40 Line of GPTA0**
	IN40	I		**IN40 Line of GPTA1**
	SENT0	I		**SENT Digital Input**
	OUT40	O1		**OUT40 Line of GPTA0**
	COUT62	O2		**CCU61**
	TCLK1	O3		**MLI1 transmit Channel Clock Output**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K11	P8.1	I/O	A1/ PU	**Port 8 General Purpose I/O Line 1**
	IN41	I		**IN41 Line of GPTA0**
	IN41	I		**IN41 Line of GPTA1**
	TREADY1A	I		**MLI1 transmit Channel ready Input A**
	SENT1	I		**SENT Digital Input**
	CC61INA	I		**CCU60**
	CC61INB	I		**CCU61**
	OUT41	O1		**OUT41 Line of GPTA0**
	CC61	O2		**CCU60**
	SENT1	O3		**SENT Digital Output**
K9	P8.2	I/O	A2/ PU	**Port 8 General Purpose I/O Line 2**
	IN42	I		**IN42 Line of GPTA0**
	IN42	I		**IN42 Line of GPTA1**
	SENT2	I		**SENT Digital Input**
	CAPINA	I		**GPT120**
	CAPINB	I		**GPT121**
	COUT63	O1		**CCU61**
	OUT42	O2		**OUT42 Line of GPTA1**
	TVALID1A	O3		**MLI1 transmit Channel valid Output A**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K7	P8.3	I/O	A2/ PU	**Port 8 General Purpose I/O Line 3**
	IN43	I		**IN43 Line of GPTA0**
	IN43	I		**IN43 Line of GPTA1**
	SENT3	I		**SENT Digital Input**
	CC62INA	I		**CCU60**
	CC62INB	I		**CCU61**
	OUT43	O1		**OUT43 Line of GPTA0**
	CC62	O2		**CCU60**
	TDATA1	O3		**MLI1 transmit Channel Data Output A**
L7	P8.4	I/O	A1/ PU	**Port 8 General Purpose I/O Line 4**
	IN44	I		**IN44 Line of GPTA0**
	IN44	I		**IN44 Line of GPTA1**
	RCLK1A	I		**MLI1 Receive Channel Clock Input A**
	SENT4	I		**SENT Digital Input**
	CC62INB	I		**CCU60**
	CC62INA	I		**CCU61**
	OUT44	O1		**OUT44 Line of GPTA0**
	CC62	O2		**CCU61**
	T3OUT	O3		**GPT121**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
L10	P8.5	I/O	A2/ PU	**Port 8 General Purpose I/O Line 5**
	IN45	I		**IN45 Line of GPTA0**
	IN45	I		**IN45 Line of GPTA1**
	SENT5	I		**SENT Digital Input**
	CTRAPA	I		**CCU60**
	CTRAPB	I		**CCU62**
	CC60INC	I		**CCU60**
	T12HRE	I		**CCU61**
	CC61INC	I		**CCU61**
	OUT45	O1		**OUT45 Line of GPTA0**
	OUT45	O2		**OUT45 Line of GPTA1**
	RREADY1A	O3		**MLI1 Receive Channel ready Output A**
M9	P8.6	I/O	A1/ PU	**Port 8 General Purpose I/O Line 6**
	IN46	I		**IN46 Line of GPTA0**
	IN46	I		**IN46 Line of GPTA1**
	RVALID1A	I		**MLI1 Receive Channel valid Input A**
	SENT6	I		**SENT Digital Input**
	OUT46	O1		**OUT46 Line of GPTA0**
	COUT60	O2		**CCU61**
	T6OUT	O3		**GPT120**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
L9	P8.7	I/O	A1/ PU	**Port 8 General Purpose I/O Line 7**
	IN47	I		**IN47 Line of GPTA0**
	IN47	I		**IN47 Line of GPTA1**
	RDATA1A	I		**MLI1 Receive Channel Data Input A**
	SENT7	I		**SENT Digital Input**
	OUT47	O1		**OUT47 Line of GPTA0**
	COUT61	O2		**CCU61**
	T6OUT	O3		**GPT121**
Port 9				
K22	P9.0	I/O	A2/ PU	**Port 9 General Purpose I/O Line 0**
	IN48	I		**IN48 Line of GPTA0**
	IN48	I		**IN48 Line of GPTA1**
	COUT63	O1		**CCU62**
	OUT48	O2		**OUT48 Line of GPTA1**
	EN12	O3		**MSC1 Device Select Output 2**
J24	P9.1	I/O	A2/ PU	**Port 9 General Purpose I/O Line 1**
	IN49	I		**IN49 Line of GPTA0**
	IN49	I		**IN49 Line of GPTA1**
	CC60INB	I		**CCU62**
	CC60INA	I		**CCU63**
	CC60	O1		**CCU63**
	OUT49	O2		**OUT49 Line of GPTA1**
	EN11	O3		**MSC1 Device Select Output 1**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
J25	P9.2	I/O	A2/ PU	**Port 9 General Purpose I/O Line 2**
	IN50	I		**IN50 Line of GPTA0**
	IN50	I		**IN50 Line of GPTA1**
	CC61INB	I		**CCU62**
	CC61INA	I		**CCU63**
	CC61	O1		**CCU63**
	OUT50	O2		**OUT50 Line of GPTA1**
	SOP1B	O3		**MSC1 serial Data Output**
H25	P9.3	I/O	A2/ PU	**Port 9 General Purpose I/O Line 3**
	IN51	I		**IN51 Line of GPTA0**
	IN51	I		**IN51 Line of GPTA1**
	CC62INB	I		**CCU62**
	CC62INA	I		**CCU63**
	CC62	O1		**CCU63**
	OUT51	O2		**OUT51 Line of GPTA1**
	FCLP1B	O3		**MSC1 Clock Output**
H24	P9.4	I/O	A2/ PU	**Port 9 General Purpose I/O Line 4**
	IN52	I		**IN52 Line of GPTA0**
	IN52	I		**IN52 Line of GPTA1**
	COUT60	O1		**CCU63**
	OUT52	O2		**OUT52 Line of GPTA1**
	EN03	O3		**MSC0 Device Select Output 3**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
L22	P9.5	I/O	A2/ PU	**Port 9 General Purpose I/O Line 5**
	IN53	I		**IN53 Line of GPTA0**
	IN53	I		**IN53 Line of GPTA1**
	SENT1	I		**SENT Digital Input**
	COUT61	O1		**CCU63**
	OUT53	O2		**OUT53 Line of GPTA1**
	EN02	O3		**MSC0 Device Select Output 2**
L21	P9.6	I/O	A2/ PU	**Port 9 General Purpose I/O Line 6**
	IN54	I		**IN54 Line of GPTA0**
	IN54	I		**IN54 Line of GPTA1**
	SENT3	I		**SENT Digital Input**
	OUT54	O1		**OUT54 Line of GPTA0**
	SENT3	O2		**SENT Digital Output**
	EN01	O3		**MSC0 Device Select Output 1**
K25	P9.7	I/O	A2/ PU	**Port 9 General Purpose I/O Line 7**
	IN55	I		**IN55 Line of GPTA0**
	IN55	I		**IN55 Line of GPTA1**
	SENT4	I		**SENT Digital Input**
	OUT55	O1		**OUT55 Line of GPTA0**
	SENT4	O2		**SENT Digital Output**
	SOP0B	O3		**MSC0 serial Data Output**
K24	P9.8	I/O	A2/ PU	**Port 9 General Purpose I/O Line 8**
	SENT6	I		**SENT Digital Input**
	COUT62	O1		**CCU63**
	SENT6	O2		**SENT Digital Output**
	FCLP0B	O3		**MSC0 Clock Output**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A28	P9.9	I/O	A1/ PU	**Port 9 General Purpose I/O Line 9**
	SENT0	I		**SENT Digital Input**
	Reserved	O1		**-**
	SENT0	O2		**SENT Digital Output**
	Reserved	O3		**-**
L25	P9.10	I/O	A1/ PU	**Port 9 General Purpose I/O Line 10**
	EMGSTOP	I		**Emergency Stop**
	SENT7	I		**SENT Digital Input**
	COUT63	O1		**CCU63**
	SENT7	O2		**SENT Digital Output**
	Reserved	O3		**-**
A27	P9.11	I/O	A1/ PU	**Port 9 General Purpose I/O Line 11**
	SENT2	I		**SENT Digital Input**
	Reserved	O1		**-**
	SENT2	O2		**SENT Digital Output**
	Reserved	O3		**-**
B27	P9.12	I/O	A1/ PU	**Port 9 General Purpose I/O Line 12**
	SENT5	I		**SENT Digital Input**
	Reserved	O1		**-**
	SENT5	O2		**SENT Digital Output**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
M21	P9.13	I/O	A2/ PU	**Port 9 General Purpose I/O Line 13**
	$\overline{\text{BRKIN}}$	I		**OCDS Break Input**
	ECTT1	I		**TTCAN Input**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	$\overline{\text{BRKOUT}}$	O		**OCDS Break Output**
N21	P9.14	I/O	A2/ PU	**Port 9 General Purpose I/O Line 14**
	$\overline{\text{BRKIN}}$	I		**OCDS Break Input**
	ECTT2	I		**TTCAN Input**
	REQ15	I		**External trigger Input 15**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	$\overline{\text{BRKOUT}}$	O		**OCDS Break Output**
Port 10				
AE20	P10.0	I/O	A2/ PU	**Port 10 General Purpose I/O Line 0**
	MRST0	I		**SSC0 Master Receive Input (Master Mode)**
	MRST0	O1		**SSC0 Slave Transmit Output (Slave Mode)**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AD20	P10.1	I/O	A2/ PU	**Port 10 General Purpose I/O Line 1**
	MTSR0	I		**SSC0 Slave Receive Input (Slave Mode)**
	MRSTG0	I		**SSC Guardian 0 Master Receive Input (Master Mode)**
	MTSR0	O1		**SSC0 Master Transmit Output (Master Mode)[3)]**
	Reserved	O2		**-**
	Reserved	O3		**-**
AB21	P10.2	I/O	A1/ PU	**Port 10 General Purpose I/O Line 2**
	SLSI0	I		**SSC0 Slave Select Input**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
AE19	P10.3	I/O	A2/ PU	**Port 10 General Purpose I/O Line 3**
	SCLK0	I		**SSC0 Clock Input/Output**
	SCLK0	O1		**SSC0 Clock Input/Output**
	Reserved	O2		**-**
	Reserved	O3		**-**
AD21	P10.4	I/O	A1+/ PU	**Port 10 General Purpose I/O Line 4**
	SLSO0	O1		**SSC0 Slave Select Output Line 0**
	Reserved	O2		**-**
	Reserved	O3		**-**
AE21	P10.5	I/O	A1+/ PU	**Port 10 General Purpose I/O Line 5**
	SLSO1	O1		**SSC0 Slave Select Output Line 1**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
Port 11				
E30	P11.0	I/O	B/ PU	**Port 11 General Purpose I/O Line 0**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A0	O		**EBU Address Bus Line 0**
E29	P11.1	I/O	B/ PU	**Port 11 General Purpose I/O Line 1**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A1	O		**EBU Address Bus Line 1**
F30	P11.2	I/O	B/ PU	**Port 11 General Purpose I/O Line 2**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A2	O		**EBU Address Bus Line 2**
F29	P11.3	I/O	B/ PU	**Port 11 General Purpose I/O Line 3**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A3	O		**EBU Address Bus Line 3**
G30	P11.4	I/O	B/ PU	**Port 11 General Purpose I/O Line 4**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A4	O		**EBU Address Bus Line 4**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
G29	P11.5	I/O	B/ PU	**Port 11 General Purpose I/O Line 5**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A5	O		**EBU Address Bus Line 5**
H30	P11.6	I/O	B/ PU	**Port 11 General Purpose I/O Line 6**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A6	O		**EBU Address Bus Line 6**
H29	P11.7	I/O	B/ PU	**Port 11 General Purpose I/O Line 7**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A7	O		**EBU Address Bus Line 7**
J30	P11.8	I/O	B/ PU	**Port 11 General Purpose I/O Line 8**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A8	O		**EBU Address Bus Line 8**
J29	P11.9	I/O	B/ PU	**Port 11 General Purpose I/O Line 9**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A9	O		**EBU Address Bus Line 9**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
K30	P11.10	I/O	B/ PU	**Port 11 General Purpose I/O Line 10**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A10	O		**EBU Address Bus Line 10**
K29	P11.11	I/O	B/ PU	**Port 11 General Purpose I/O Line 11**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A11	O		**EBU Address Bus Line 11**
L30	P11.12	I/O	B/ PU	**Port 11 General Purpose I/O Line 12**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A12	O		**EBU Address Bus Line 12**
L29	P11.13	I/O	B/ PU	**Port 11 General Purpose I/O Line 13**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A13	O		**EBU Address Bus Line 13**
M30	P11.14	I/O	B/ PU	**Port 11 General Purpose I/O Line 14**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A14	O		**EBU Address Bus Line 14**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
M29	P11.15	I/O	B/ PU	**Port 11 General Purpose I/O Line 15**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A15	O		**EBU Address Bus Line 15**
Port 12				
N30	P12.0	I/O	B/ PU	**Port 12 General Purpose I/O Line 0**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A16	O		**EBU Address Bus Line 16**
N29	P12.1	I/O	B/ PU	**Port 12 General Purpose I/O Line 1**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A17	O		**EBU Address Bus Line 17**
P30	P12.2	I/O	B/ PU	**Port 12 General Purpose I/O Line 2**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A18	O		**EBU Address Bus Line 18**
P29	P12.3	I/O	B/ PU	**Port 12 General Purpose I/O Line 3**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A19	O		**EBU Address Bus Line 19**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
V30	P12.4	I/O	B/ PU	**Port 12 General Purpose I/O Line 4**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A20	O		**EBU Address Bus Line 20**
V29	P12.5	I/O	B/ PU	**Port 12 General Purpose I/O Line 5**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A21	O		**EBU Address Bus Line 21**
D30	P12.6	I/O	B/ PU	**Port 12 General Purpose I/O Line 6**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A22	O		**EBU Address Bus Line 22**
D29	P12.7	I/O	B/ PU	**Port 12 General Purpose I/O Line 7**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	A23	O		**EBU Address Bus Line 23**
Port 13				

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
U21	P13.0	I/O	B/ PU	**Port 13 General Purpose I/O Line 0**
	AD0	I		**EBU Address/Data Bus Line 0**
	OUT88	O1		**OUT88 Line of GPTA0**
	OUT88	O2		**OUT88 Line of GPTA1**
	OUT80	O3		**OUT80 Line of LTCA2**
	AD0	O		**EBU Address/Data Bus Line 0**
U22	P13.1	I/O	B/ PU	**Port 13 General Purpose I/O Line 1**
	AD1	I		**EBU Address/Data Bus Line 1**
	OUT89	O1		**OUT89 Line of GPTA0**
	OUT89	O2		**OUT89 Line of GPTA1**
	OUT81	O3		**OUT81 Line of LTCA2**
	AD1	O		**EBU Address/Data Bus Line 1**
V21	P13.2	I/O	B/ PU	**Port 13 General Purpose I/O Line 2**
	AD2	I		**EBU Address/Data Bus Line 2**
	OUT90	O1		**OUT90 Line of GPTA0**
	OUT90	O2		**OUT90 Line of GPTA1**
	OUT82	O3		**OUT82 Line of LTCA2**
	AD2	O		**EBU Address/Data Bus Line 2**
V22	P13.3	I/O	B/ PU	**Port 13 General Purpose I/O Line 3**
	AD3	I		**EBU Address/Data Bus Line 3**
	OUT91	O1		**OUT91 Line of GPTA0**
	OUT91	O2		**OUT91 Line of GPTA1**
	OUT83	O3		**OUT83 Line of LTCA2**
	AD3	O		**EBU Address/Data Bus Line 3**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
V24	P13.4	I/O	B/ PU	**Port 13 General Purpose I/O Line 4**
	AD4	I		**EBU Address/Data Bus Line 4**
	OUT92	O1		**OUT92 Line of GPTA0**
	OUT92	O2		**OUT92 Line of GPTA1**
	OUT84	O3		**OUT84 Line of LTCA2**
	AD4	O		**EBU Address/Data Bus Line 4**
V25	P13.5	I/O	B/ PU	**Port 13 General Purpose I/O Line 5**
	AD5	I		**EBU Address/Data Bus Line 5**
	OUT93	O1		**OUT93 Line of GPTA0**
	OUT93	O2		**OUT93 Line of GPTA1**
	OUT85	O3		**OUT85 Line of LTCA2**
	AD5	O		**EBU Address/Data Bus Line 5**
W21	P13.6	I/O	B/ PU	**Port 13 General Purpose I/O Line 6**
	AD6	I		**EBU Address/Data Bus Line 6**
	OUT94	O1		**OUT94 Line of GPTA0**
	OUT94	O2		**OUT94 Line of GPTA1**
	OUT86	O3		**OUT86 Line of LTCA2**
	AD6	O		**EBU Address/Data Bus Line 6**
W22	P13.7	I/O	B/ PU	**Port 13 General Purpose I/O Line 7**
	AD7	I		**EBU Address/Data Bus Line 7**
	OUT95	O1		**OUT95 Line of GPTA0**
	OUT95	O2		**OUT95 Line of GPTA1**
	OUT87	O3		**OUT87 Line of LTCA2**
	AD7	O		**EBU Address/Data Bus Line 7**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
W24	P13.8	I/O	B/ PU	**Port 13 General Purpose I/O Line 8**
	AD8	I		**EBU Address/Data Bus Line 8**
	OUT96	O1		**OUT96 Line of GPTA0**
	OUT96	O2		**OUT96 Line of GPTA1**
	OUT88	O3		**OUT88 Line of LTCA2**
	AD8	O		**EBU Address/Data Bus Line 8**
W25	P13.9	I/O	B/ PU	**Port 13 General Purpose I/O Line 9**
	AD9	I		**EBU Address/Data Bus Line 9**
	OUT97	O1		**OUT97 Line of GPTA0**
	OUT97	O2		**OUT97 Line of GPTA1**
	OUT89	O3		**OUT89 Line of LTCA2**
	AD9	O		**EBU Address/Data Bus Line 9**
Y22	P13.10	I/O	B/ PU	**Port 13 General Purpose I/O Line 10**
	AD10	I		**EBU Address/Data Bus Line 10**
	OUT98	O1		**OUT98 Line of GPTA0**
	OUT98	O2		**OUT98 Line of GPTA1**
	OUT90	O3		**OUT90 Line of LTCA2**
	AD10	O		**EBU Address/Data Bus Line 10**
Y24	P13.11	I/O	B/ PU	**Port 13 General Purpose I/O Line 11**
	AD11	I		**EBU Address/Data Bus Line 11**
	OUT99	O1		**OUT99 Line of GPTA0**
	OUT99	O2		**OUT99 Line of GPTA1**
	OUT91	O3		**OUT91 Line of LTCA2**
	AD11	O		**EBU Address/Data Bus Line 11**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
Y25	P13.12	I/O	B/ PU	**Port 13 General Purpose I/O Line 12**
	AD12	I		**EBU Address/Data Bus Line 12**
	OUT100	O1		**OUT100 Line of GPTA0**
	OUT100	O2		**OUT100 Line of GPTA1**
	OUT92	O3		**OUT92 Line of LTCA2**
	AD12	O		**EBU Address/Data Bus Line 12**
AA24	P13.13	I/O	B/ PU	**Port 13 General Purpose I/O Line 13**
	AD13	I		**EBU Address/Data Bus Line 13**
	OUT101	O1		**OUT101 Line of GPTA0**
	OUT101	O2		**OUT101 Line of GPTA1**
	OUT93	O3		**OUT93 Line of LTCA2**
	AD13	O		**EBU Address/Data Bus Line 13**
AA25	P13.14	I/O	B/ PU	**Port 13 General Purpose I/O Line 14**
	AD14	I		**EBU Address/Data Bus Line 14**
	OUT102	O1		**OUT102 Line of GPTA0**
	OUT102	O2		**OUT102 Line of GPTA1**
	OUT94	O3		**OUT94 Line of LTCA2**
	AD14	O		**EBU Address/Data Bus Line 14**
AB24	P13.15	I/O	B/ PU	**Port 13 General Purpose I/O Line 15**
	AD15	I		**EBU Address/Data Bus Line 15**
	OUT103	O1		**OUT103 Line of GPTA0**
	OUT103	O2		**OUT103 Line of GPTA1**
	OUT95	O3		**OUT95 Line of LTCA2**
	AD15	O		**EBU Address/Data Bus Line 15**
Port 14				

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AB25	P14.0	I/O	B/ PU	**Port 14 General Purpose I/O Line 0**
	AD16	I		**EBU Address/Data Bus Line 16**
	CC60	O1		**CCU60**
	OUT96	O2		**OUT96 Line of GPTA1**
	OUT96	O3		**OUT96 Line of LTCA2**
	AD16	O		**EBU Address/Data Bus Line 16**
W30	P14.1	I/O	B/ PU	**Port 14 General Purpose I/O Line 1**
	AD17	I		**EBU Address/Data Bus Line 17**
	CC61	O1		**CCU60**
	OUT97	O2		**OUT97 Line of GPTA1**
	OUT97	O3		**OUT97 Line of LTCA2**
	AD17	O		**EBU Address/Data Bus Line 17**
AC25	P14.2	I/O	B/ PU	**Port 14 General Purpose I/O Line 2**
	AD18	I		**EBU Address/Data Bus Line 18**
	CC62	O1		**CCU60**
	OUT98	O2		**OUT98 Line of GPTA1**
	OUT98	O3		**OUT98 Line of LTCA2**
	AD18	O		**EBU Address/Data Bus Line 18**
Y30	P14.3	I/O	B/ PU	**Port 14 General Purpose I/O Line 3**
	AD19	I		**EBU Address/Data Bus Line 19**
	COUT60	O1		**CCU60**
	OUT99	O2		**OUT99 Line of GPTA1**
	OUT99	O3		**OUT99 Line of LTCA2**
	AD19	O		**EBU Address/Data Bus Line 19**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AD23	P14.4	I/O	B/ PU	**Port 14 General Purpose I/O Line 4**
	AD20	I		**EBU Address/Data Bus Line 20**
	COUT61	O1		**CCU60**
	OUT100	O2		**OUT100 Line of GPTA1**
	OUT100	O3		**OUT100 Line of LTCA2**
	AD20	O		**EBU Address/Data Bus Line 20**
AA30	P14.5	I/O	B/ PU	**Port 14 General Purpose I/O Line 5**
	AD21	I		**EBU Address/Data Bus Line 21**
	COUT62	O1		**CCU60**
	OUT101	O2		**OUT101 Line of GPTA1**
	OUT101	O3		**OUT101 Line of LTCA2**
	AD21	O		**EBU Address/Data Bus Line 21**
AE24	P14.6	I/O	B/ PU	**Port 14 General Purpose I/O Line 6**
	AD22	I		**EBU Address/Data Bus Line 22**
	COUT63	O1		**CCU60**
	OUT102	O2		**OUT102 Line of GPTA1**
	OUT102	O3		**OUT102 Line of LTCA2**
	AD22	O		**EBU Address/Data Bus Line 22**
AB30	P14.7	I/O	B/ PU	**Port 14 General Purpose I/O Line 7**
	AD23	I		**EBU Address/Data Bus Line 23**
	CC60	O1		**CCU61**
	OUT103	O2		**OUT103 Line of GPTA1**
	OUT103	O3		**OUT103 Line of LTCA2**
	AD23	O		**EBU Address/Data Bus Line 23**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AE23	P14.8	I/O	B/ PU	**Port 14 General Purpose I/O Line 8**
	AD24	I		**EBU Address/Data Bus Line 24**
	CC61	O1		**CCU61**
	T3OUT	O2		**GPT120**
	OUT104	O3		**OUT104 Line of LTCA2**
	AD24	O		**EBU Address/Data Bus Line 24**
AC30	P14.9	I/O	B/ PU	**Port 14 General Purpose I/O Line 9**
	AD25	I		**EBU Address/Data Bus Line 25**
	CC62	O1		**CCU61**
	T3OUT	O2		**GPT121**
	OUT105	O3		**OUT105 Line of LTCA2**
	AD25	O		**EBU Address/Data Bus Line 25**
AC29	P14.10	I/O	B/ PU	**Port 14 General Purpose I/O Line 10**
	AD26	I		**EBU Address/Data Bus Line 26**
	COUT60	O1		**CCU61**
	T6OUT	O1		**GPT120**
	OUT106	O3		**OUT106 Line of LTCA2**
	AD26	O		**EBU Address/Data Bus Line 26**
AD30	P14.11	I/O	B/ PU	**Port 14 General Purpose I/O Line 11**
	AD27	I		**EBU Address/Data Bus Line 27**
	COUT61	O1		**CCU61**
	T6OUT	O1		**GPT121**
	OUT107	O3		**OUT107 Line of LTCA2**
	AD27	O		**EBU Address/Data Bus Line 27**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AD29	P14.12	I/O	B/ PU	**Port 14 General Purpose I/O Line 12**
	AD28	I		**EBU Address/Data Bus Line 28**
	COUT62	O1		**CCU61**
	OUT108	O2		**OUT108 Line of GPTA1**
	OUT108	O3		**OUT108 Line of LTCA2**
	AD28	O		**EBU Address/Data Bus Line 28**
AE30	P14.13	I/O	B/ PU	**Port 14 General Purpose I/O Line 13**
	AD29	I		**EBU Address/Data Bus Line 29**
	COUT63	O1		**CCU61**
	OUT109	O2		**OUT109 Line of GPTA1**
	OUT109	O3		**OUT109 Line of LTCA2**
	AD29	O		**EBU Address/Data Bus Line 29**
AE29	P14.14	I/O	B/ PU	**Port 14 General Purpose I/O Line 14**
	AD30	I		**EBU Address/Data Bus Line 30**
	T3INC	I		**GPT120**
	T3IND	I		**GPT121**
	OUT110	O1		**OUT110 Line of GPTA0**
	OUT110	O2		**OUT110 Line of GPTA1**
	OUT110	O3		**OUT110 Line of LTCA2**
	AD30	O		**EBU Address/Data Bus Line 30**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AF30	P14.15	I/O	B/ PU	**Port 14 General Purpose I/O Line 15**
	AD31	I		**EBU Address/Data Bus Line 31**
	T3EUDC	I		**GPT120**
	T3EUDD	I		**GPT121**
	OUT111	O1		**OUT111 Line of GPTA0**
	OUT111	O2		**OUT111 Line of GPTA1**
	OUT111	O3		**OUT111 Line of LTCA2**
	AD31	O		**EBU Address/Data Bus Line 31**
Port 15				
AJ26	P15.0	I/O	B/ PU	**Port 15 General Purpose I/O Line 0**
	T4INC	I		**GPT120**
	T4IND	I		**GPT121**
	CCPOS2B	I		**CCU60**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	CS0	O		**Chip Select Output Line 0**
AK26	P15.1	I/O	B/ PU	**Port 15 General Purpose I/O Line 1**
	T4EUDC	I		**GPT120**
	T4EUDD	I		**GPT121**
	CCPOS2B	I		**CCU61**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	CS1	O		**Chip Select Output Line 1**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AJ25	P15.2	I/O	B/ PU	**Port 15 General Purpose I/O Line 2**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	CS2	O		**Chip Select Output Line 2**
AK24	P15.3	I/O	B/ PU	**Port 15 General Purpose I/O Line 3**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	CS3	O		**Chip Select Output Line 3**
AJ17	P15.4	I/O	B/ PU	**Port 15 General Purpose I/O Line 4**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BC0	O		**Byte Control Line 0**
AK18	P15.5	I/O	B/ PU	**Port 15 General Purpose I/O Line 5**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BC1	O		**Byte Control Line 1**
AJ18	P15.6	I/O	B/ PU	**Port 15 General Purpose I/O Line 6**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BC2	O		**Byte Control Line 2**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AK19	P15.7	I/O	B/ PU	**Port 15 General Purpose I/O Line 7**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BC3	O		**Byte Control Line 3**
AK25	P15.8	I/O	B/ PU	**Port 15 General Purpose I/O Line 8**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	RD	O		**Read Control Line**
AJ27	P15.9	I/O	B/ PU	**Port 15 General Purpose I/O Line 9**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	RD/WR	O		**Write Control Line**
AJ28	P15.10	I/O	B/ PU	**Port 15 General Purpose I/O Line 10**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	ADV	O		**Address Valid Output**
AJ24	P15.11	I/O	B/ PU	**Port 15 General Purpose I/O Line 11**
	WAIT	I		**Wait Input for inserting Wait-States**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AK20	P15.12	I/O	B/ PU	**Port 15 General Purpose I/O Line 12**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	MR/W	O		**Motorola-style Read/Write Control Signal**
AK29	P15.13	I/O	B/ PU	**Port 15 General Purpose I/O Line 13**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BAA	O		**Burst Address Advance Output**
AG30	P15.14	I/O	B/ PU	**Port 15 General Purpose I/O Line 14**
	BFCLKI	I		**Burst FLASH Clock Input (Clock Feedback).**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
AH30	P15.15	I/O	B/ PU	**Port 15 General Purpose I/O Line 15**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BFCLKO	O		**Burst Mode Flash Clock Output (Non-Differential)**
Port 16				

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AK17	P16.0	I/O	B/ PU	**Port 16 General Purpose I/O Line 0**
	HOLD	I		**Hold Request Input**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
AJ19	P16.1	I/O	B/ PU	**Port 16 General Purpose I/O Line 1**
	HLDA	I		**Hold Acknowledge Input**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	HLDA	O		**Hold Acknowledge Output**
AK28	P16.2	I/O	B/ PU	**Port 16 General Purpose I/O Line 2**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	BREQ	O		**Bus Request Output**
AJ20	P16.3	I/O	B/ PU	**Port 16 General Purpose I/O Line 3**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	CSCOMB	O		**Combined Chip Select Output**
AK23	P16.4	I/O	B/ PU	**Port 16 General Purpose I/O Line 4**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	$\overline{\text{RAS}}$	O		**Row Address Select/Strobe**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AJ23	P16.5	I/O	B/ PU	**Port 16 General Purpose I/O Line 5**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	$\overline{\text{CAS}}$	O		**Column Address Select/Strobe**
AG29	P16.6	I/O	B/ PU	**Port 16 General Purpose I/O Line 6**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	DDRCLK	O		**Double Data Rate Flash Clock**
AF29	P16.7	I/O	B/ PU	**Port 16 General Purpose I/O Line 7**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	DDRCLKN	O		**Inverted Double Data Rate Flash Clock**
AK27	P16.8	I/O	B/ PU	**Port 16 General Purpose I/O Line 8**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	CKE	O		**Inverted Double Data Rate Flash Clock**
W29	P16.9	I/O	B/ PU	**Port 16 General Purpose I/O Line 9**
	DQS0	I		**Data Strobe Signal 0**
	Reserved	O1		-
	Reserved	O2		-
	Reserved	O3		-
	DQS0	O		**Data Strobe Signal 0**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
Y29	P16.10	I/O	B/ PU	**Port 16 General Purpose I/O Line 10**
	DQS1	I		**Data Strobe Signal 1**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	DQS1	O		**Data Strobe Signal 1**
AA29	P16.11	I/O	B/ PU	**Port 16 General Purpose I/O Line 11**
	DQS2	I		**Data Strobe Signal 2**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	DQS2	O		**Data Strobe Signal 2**
AB29	P16.12	I/O	B/ PU	**Port 16 General Purpose I/O Line 12**
	DQS3	I		**Data Strobe Signal 3**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	DQS3	O		**Data Strobe Signal 3**
Port 17				
Y10	P17.0	I	D / S	**Port 17 General Purpose I Line 0[4)]**
	SENT0	I		**SENT Digital Input 0**
	AN8	I		**Analog Input : ADC0.CH8 [5)]**
Y9	P17.1	I	D / S	**Port 17 General Purpose I Line 1[4)]**
	SENT1	I		**SENT Digital Input 1**
	AN9	I		**Analog Input : ADC0.CH9 [5)]**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
W10	P17.2	I	D / S	**Port 17 General Purpose I Line 2[4)]**
	SENT2	I		**SENT Digital Input 2**
	AN10	I		**Analog Input : ADC0.CH10 [5)]**
W9	P17.3	I	D / S	**Port 17 General Purpose I Line 3[4)]**
	SENT3	I		**SENT Digital Input 3**
	AN11	I		**Analog Input : ADC0.CH11 [5)]**
W7	P17.4	I	D / S	**Port 17 General Purpose I Line 4[4)]**
	SENT4	I		**SENT Digital Input 4**
	AN12	I		**Analog Input : ADC0.CH12 [5)]**
W6	P17.5	I	D / S	**Port 17 General Purpose I Line 5[4)]**
	SENT5	I		**SENT Digital Input 5**
	AN13	I		**Analog Input : ADC0.CH13 [5)]**
V7	P17.6	I	D / S	**Port 17 General Purpose I Line 6[4)]**
	SENT6	I		**SENT Digital Input 6**
	AN14	I		**Analog Input : ADC0.CH14 [5)]**
V6	P17.7	I	D / S	**Port 17 General Purpose I Line 7[4)]**
	SENT7	I		**SENT Digital Input 7**
	AN15	I		**Analog Input : ADC0.CH15 [5)]**
AD9	P17.8	I	D / S	**Port 17 General Purpose I Line 8[4)]**
	SENT0	I		**SENT Digital Input 0**
	AN36	I		**Analog Input : ADC2.CH4 [5)]**
AE9	P17.9	I	D / S	**Port 17 General Purpose I Line 9[4)]**
	SENT1	I		**SENT Digital Input 1**
	AN37	I		**Analog Input : ADC2.CH5 [5)]**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AD10	P17.10	I	D / S	**Port 17 General Purpose I Line 10[4)]**
	SENT2	I		**SENT Digital Input 2**
	AN38	I		**Analog Input : ADC2.CH6 [5)]**
AE10	P17.11	I	D / S	**Port 17 General Purpose I Line 11[4)]**
	SENT3	I		**SENT Digital Input 3**
	AN39	I		**Analog Input : ADC2.CH7 [5)]**
AA11	P17.12	I	D / S	**Port 17 General Purpose I Line 12[4)]**
	SENT4	I		**SENT Digital Input 4**
	AN40	I		**Analog Input : ADC2.CH8 [5)]**
AB11	P17.13	I	D / S	**Port 17 General Purpose I Line 13[4)]**
	SENT5	I		**SENT Digital Input 5**
	AN41	I		**Analog Input : ADC2.CH9 [5)]**
AA12	P17.14	I	D / S	**Port 17 General Purpose I Line 14[4)]**
	SENT6	I		**SENT Digital Input 6**
	AN42	I		**Analog Input : ADC2.CH10 [5)]**
AB12	P17.15	I	D / S	**Port 17 General Purpose I Line 15[4)]**
	SENT7	I		**SENT Digital Input 7**
	AN43	I		**Analog Input : ADC2.CH11 [5)]**
Port 18				
B11	P18.0	I/O	A1+/ PU	**Port 18 General Purpose I/O Line 0**
	MRST2B	I		**SSC2 Master Receive Input B (Slave Mode)**
	MRST2	O1		**SSC2 Slave Transmit Output (Master Mode)**
	Reserved	O2		**-**
	Reserved	O3		**-**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
A11	P18.1	I/O	A1+/ PU	**Port 18 General Purpose I/O Line 1**
	MTSR2B	I		**SSC2 Slave Receive Input B (Slave Mode)**
	MRSTG2B	I		**SSC Guardian 2 Master Receive Input B (Master Mode)**
	MTSR2	O1		**SSC2 Master Transmit Output (Master Mode)[3)]**
	Reserved	O2		-
	Reserved	O3		-
B10	P18.2	I/O	A1+/ PU	**Port 18 General Purpose I/O Line 2**
	SCLK2B	I		**SSC2 Input**
	SCLK2	O1		**SSC2 Output**
	Reserved	O2		-
	Reserved	O3		-
A10	P18.3	I/O	A1+/ PU	**Port 18 General Purpose I/O Line 3**
	SLSO20	O1		**SSC2 Output**
	Reserved	O2		-
	Reserved	O3		-
B9	P18.4	I/O	A1+/ PU	**Port 18 General Purpose I/O Line 4**
	SLSO21	O1		**SSC2 Output**
	Reserved	O2		-
	Reserved	O3		-
A9	P18.5	I/O	A1+/ PU	**Port 18 General Purpose I/O Line 5**
	SLSO22	O1		**SSC2 Output**
	Reserved	O2		-
	Reserved	O3		-

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
B8	P18.6	I/O	A1+/ PU	**Port 18 General Purpose I/O Line 6**
	SLSO23	O1		**SSC2 Output**
	Reserved	O2		-
	Reserved	O3		-
A8	P18.7	I/O	A1+/ PU	**Port 18 General Purpose I/O Line 7**
	SLSO24	O1		**SSC2 Output**
	Reserved	O2		-
	Reserved	O3		-
Analog Input Port				
AA9	AN0	I	D	**Analog Input 0: ADC0.CH0** [5]
AE7	AN1	I	D	**Analog Input 1: ADC0.CH1** [5]
AD7	AN2	I	D	**Analog Input 2: ADC0.CH2** [5]
AD6	AN3	I	D	**Analog Input 3: ADC0.CH3** [5]
AC7	AN4	I	D	**Analog Input 4: ADC0.CH4** [5]
AB7	AN5	I	D	**Analog Input 5: ADC0.CH5** [5]
AA7	AN6	I	D	**Analog Input 6: ADC0.CH6** [5]
AA10	AN7	I	D	**Analog Input 7: ADC0.CH7** [5]
Y10	AN8	I	S	**Analog Input 8: ADC0.CH8, SENT0** [5]
Y9	AN9	I	S	**Analog Input 9: ADC0.CH9, SENT1** [5]
W10	AN10	I	S	**Analog Input 10: ADC0.CH10, SENT2** [5]
W9	AN11	I	S	**Analog Input 11: ADC0.CH11, SENT3** [5]
W7	AN12	I	S	**Analog Input 12: ADC0.CH12, SENT4** [5]
W6	AN13	I	S	**Analog Input 13: ADC0.CH13, SENT5** [5]
V7	AN14	I	S	**Analog Input 14: ADC0.CH14, SENT6** [5]
V6	AN15	I	S	**Analog Input 15: ADC0.CH15, SENT7** [5]
V10	AN16	I	D	**Analog Input 16: ADC1.CH0** [5]

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
V9	AN17	I	D	**Analog Input 17: ADC1.CH1** [5]
U10	AN18	I	D	**Analog Input 18: ADC1.CH2** [5]
U9	AN19	I	D	**Analog Input 19: ADC1.CH3** [5]
U7	AN20	I	D	**Analog Input 20: ADC1.CH4** [5]
U6	AN21	I	D	**Analog Input 21: ADC1.CH5** [5]
T7	AN22	I	D	**Analog Input 22: ADC1.CH6** [5]
T6	AN23	I	D	**Analog Input 23: ADC1.CH7** [5]
AB13	AN24	I	D	**Analog Input 24: ADC1.CH8** [5]
AD13	AN25	I	D	**Analog Input 25: ADC1.CH9** [5]
AE13	AN26	I	D	**Analog Input 26: ADC1.CH10** [5]
AA14	AN27	I	D	**Analog Input 27: ADC1.CH11** [5]
AB14	AN28	I	D	**Analog Input 28: ADC1.CH12** [5]
AD14	AN29	I	D	**Analog Input 29: ADC1.CH13** [5]
AE14	AN30	I	D	**Analog Input 30: ADC1.CH14** [5]
AA15	AN31	I	D	**Analog Input 31: ADC1.CH15** [5]
AB9	AN32	I	D	**Analog Input 32: ADC2.CH0** [5]
AD8	AN33	I	D	**Analog Input 33: ADC2.CH1** [5]
AE8	AN34	I	D	**Analog Input 34: ADC2.CH2** [5]
AA13	AN35	I	D	**Analog Input 35: ADC2.CH3** [5]
AD9	AN36	I	S	**Analog Input 36: ADC2.CH4, SENT0** [5]
AE9	AN37	I	S	**Analog Input 37: ADC2.CH5, SENT1** [5]
AD10	AN38	I	S	**Analog Input 38: ADC2.CH6, SENT2** [5]
AE10	AN39	I	S	**Analog Input 39: ADC2.CH7, SENT3** [5]
AA11	AN40	I	S	**Analog Input 40: ADC2.CH8, SENT4** [5]
AB11	AN41	I	S	**Analog Input 41: ADC2.CH9, SENT5** [5]
AA12	AN42	I	S	**Analog Input 42: ADC2.CH10, SENT6** [5]

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AB12	AN43	I	S	**Analog Input 43: ADC2.CH11, SENT7** [5]
AC6	AN44	I	D	**Analog Input 44: ADC2.CH12** [5]
AB6	AN45	I	D	**Analog Input 45: ADC2.CH13** [5]
AA6	AN46	I	D	**Analog Input 46: ADC2.CH14** [5]
AB10	AN47	I	D	**Analog Input 47: ADC2.CH15** [5]
W2	AN48	I	D	**Analog Input 48: ADC3.CH0** [5]
W1	AN49	I	D	**Analog Input 49: ADC3.CH1** [5]
AA2	AN50	I	D	**Analog Input 50: ADC3.CH2** [5]
AA1	AN51	I	D	**Analog Input 51: ADC3.CH3** [5]
AB2	AN52	I	D	**Analog Input 52: ADC3.CH4** [5]
AB1	AN53	I	D	**Analog Input 53: ADC3.CH5** [5]
AC2	AN54	I	D	**Analog Input 54: ADC3.CH6** [5]
AC1	AN55	I	D	**Analog Input 55: ADC3.CH7** [5]
AD2	AN56	I	D	**Analog Input 56: ADC3.CH8** [5]
AD1	AN57	I	D	**Analog Input 57: ADC3.CH9** [5]
AE2	AN58	I	D	**Analog Input 58: ADC3.CH10** [5]
AE1	AN59	I	D	**Analog Input 59: ADC3.CH11** [5]
AF2	AN60	I	D	**Analog Input 60: ADC3.CH12** [5]
AF1	AN61	I	D	**Analog Input 61: ADC3.CH13** [5]
AG2	AN62	I	D	**Analog Input 62: ADC3.CH14** [5]
AG1	AN63	I	D	**Analog Input 63: ADC3.CH15** [5]
AJ5	AN64	I	D	**Analog Input 64: FADC_FADIN0P** [6]
AK5	AN65	I	D	**Analog Input 65: FADC_FADIN0N** [6]
AJ6	AN66	I	D	**Analog Input 66: FADC_FADIN1P** [6]
AK6	AN67	I	D	**Analog Input 67: FADC_FADIN1N** [6]
AJ7	AN68	I	D	**Analog Input 68: FADC_FADIN2P** [6]

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AK7	AN69	I	D	**Analog Input 69: FADC_FADIN2N** [6]
AJ8	AN70	I	D	**Analog Input 70: FADC_FADIN3P** [6]
AK8	AN71	I	D	**Analog Input 71: FADC_FADIN3N** [6]
System I/O				
L24	$\overline{\text{PORST}}$	I	PD	**Power-on Reset Input**
M24	$\overline{\text{ESR0}}$	I/O	A2	**External System Request Reset Input 0** Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset.
M25	$\overline{\text{ESR1}}$	I/O	A2/ PD	**External System Request Reset Input 1**
N25	TCK	I	PD	**JTAG Module Clock Input**
	DAP0	I		**Device Access Port Line 0**
P22	TDI	I	A2/ PU	**JTAG Module Serial Data Input**
	$\overline{\text{BRKIN}}$	I		**OCDS Break Input (Alternate Output)**
	$\overline{\text{BRKOUT}}$	O		**OCDS Break Output (Alternate Input)**
M22	$\overline{\text{TESTMODE}}$	I	PU	**Test Mode Select Input**
P21	TMS	I	A2/ PD	**JTAG Module State Machine Control Input**
	DAP1	I/O		**Device Access Port Line 1**
N24	$\overline{\text{TRST}}$	I	PD	**JTAG Module Reset/Enable Input**
R25	XTAL1	I		**Main Oscillator/PLL/Clock Generator Input**
R24	XTAL2	O		**Main Oscillator/PLL/Clock Generator Output**
N22	TDO	O	A2/ PU	**JTAG Module Serial Data Output**
	$\overline{\text{BRKIN}}$	I		**OCDS Break Input (Alternate Input)**
	$\overline{\text{BRKOUT}}$	O		**OCDS Break Output (Alternate Output)**
	DAP2	O		**Device Access Port Line 2**
Power Supply				

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
Y7	V_{DDM}	-	-	**ADC Analog Part Power Supply (3.3V - 5V)**
Y1, Y2, Y6	V_{SSM}	-	-	**ADC Analog Part Ground**
AE11	V_{AREF0}	-	-	**ADC0 Reference Voltage**
AE12	V_{AGND0}	-	-	**ADC0 Reference Ground**
AD11	V_{AREF1}	-	-	**ADC1 Reference Voltage**
AK9	V_{AGND1}	-	-	**ADC1 Reference Ground**
AD12	V_{AREF2}	-	-	**ADC2 Reference Voltage**
AJ10	V_{AGND2}	-	-	**ADC2 Reference Ground**
AJ9	V_{AREF3}	-	-	**ADC3 Reference Voltage**
AK10	V_{AGND3}	-	-	**ADC3 Reference Ground**
AB15	V_{FAREF}	-	-	**FADC Reference Voltage**
AD15	V_{FAGND}	-	-	**FADC Reference Ground**
AB16	V_{DDMF}	-	-	**FADC Analog Part Power Supply (3.3V)**
AA16	V_{DDAF}	-	-	**FADC Analog Part Logic Power Supply (1.3V)**
AE15, AJ11, AK11	V_{SSMF}	-	-	**FADC Analog Part Ground**
	V_{SSAF}	-	-	**FADC Analog Part Logic Ground**
R10, T21	V_{DDFL3}	-	-	**Flash Power Supply (3.3V)**
R30, R29, P25	V_{SSOSC}	-	-	**Main Oscillator Ground**
	V_{SS}	-	-	**Digital Ground**
P24	V_{DDOSC}	-	-	**Main Oscillator Power Supply (1.3V)**
R21	V_{DDOSC3}	-	-	**Main Oscillator Power Supply (3.3V)**
R22	V_{DDPF}	-	-	**E-Ray PLL Power Supply (1.3V)**
T22	V_{DDPF3}	-	-	**E-Ray PLL Power Supply (3.3V)**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
AJ30, AH29, AD25, AC24, AA22, Y21	V_{DD}	-	-	**Digital Core Power Supply (1.3V)**
W18, W13, V19, V12, N19, N12, M18, M13	V_{DD}	-	-	**Digital Core Power Supply (1.3V, center balls)**
AK15, AJ15, AD16, T2, T1, R7, G23, G15, G8, F24, F7, B28, A29, B16, A16, B3, A2	V_{DDP}	-	-	**Port Power Supply (3.3V)**
AK21, AJ21, AD22, U24, U25, U29, U30, C30	V_{DDEBU}	-	-	**EBU Port Power Supply (1.8 - 2.5V - 3.3V)**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
T9, T10	V_{DDSB}	-	-	**Emulation Stand-by SRAM Power Supply (1.3V) (Emulation device only)** *Note: This pin is N.C. in a productive device.*
AK16, AJ16, AE16, R6, R2, R1, F15, K10, K21, J22, J9, G24, G7, F25, B29, B15, B2, A30, A15	V_{SSP}	-	-	**Digital Ground**
AK22, AJ22, AE22, T30, T29, T25, T24, B30	V_{SS}	-	-	**Digital Ground**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
W17, W16, W15, W14, , V17, V16, V15, V14	V_{SS}	-	-	**Digital Ground (center balls)**
N17, N16, N15, N14, , M17, M16, M15, M14	V_{SS}	-	-	**Digital Ground (center balls cont'd)**
U19, U18, U16, U15, U13, U12, P13, P12, P19, P18, P16, P15,	V_{SS}	-	-	**Digital Ground (center balls cont'd)**
R19, R18, R17, R16, R15, R14, R13, R12	V_{SS}	-	-	**Digital Ground (center balls cont'd)**

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
T19, T18, T17, T16, T15, T14, T13, T12	V_{SS}	-	-	**Digital Ground (center balls cont'd)**
AK30, AJ29, AE25, AD24, AB22, AA21	V_{SS}	-	-	**Digital Ground (center balls cont'd)**
A1, A3, A4, A5, A14, A17, A23, A24, A25, A26	N.C.	-	-	**Not connected.** These pins are reserved for future extension and shall not be connected externally.
B1, B4, B5, B14, B17, B23, B24, B25, B26	N.C.	-	-	**Not connected.** These pins are reserved for future extension and shall not be connected externally.

Table 2 Pin Definitions and Functions (PG-LFBGA- 516 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
C1, C2, C29, D1, D2, E1, E2, F1, F2, F6, G1, G2, N1, N2	N.C.	-	-	**Not connected.** These pins are reserved for future extension and shall not be connected externally.
U1, U2, V1, V2, AE6, AH1, AH2, AJ1, AJ2, AJ3	N.C.	-	-	**Not connected.** These pins are reserved for future extension and shall not be connected externally.
AJ4, AJ12, AK1, AK2, AK3, AK4, AK12, AK13	N.C.	-	-	**Not connected.** These pins are reserved for future extension and shall not be connected externally.

1) Only applicable in TC1798ED. Reserved in TC1798PD.

2) Only available for SAK-TC1798F-512F300EL, SAK-TC1798F-512F300EP, and SAK-TC1798S-512F300EP.

3) The MTSR output of SSCx is overlayed with the MRSTG input of the related SSCGx

4) Analog Input overlayed with a SENT Digitial Input. The related port logic is used configure the input as either analog input (default after reset) or digital input. The related port logic supports only the port input features as the connected pads are input pads only.

5) IOZ1 valid for this pin is the parameter with overlayed = No in the ADC parameter table.

6) IOZ1 valid for this pin is the parameter with overlayed = Yes in the ADC parameter table.

Legend for Table 2

Column “**Ctrl.**”:

I = Input (for GPIO port lines with IOCR bit field selection PCx = $0XXX_B$)

O = Output
O0 = Output with IOCR bit field selection PCx = $1X00_B$
O1 = Output with IOCR bit field selection PCx = $1X01_B$ (ALT1)
O2 = Output with IOCR bit field selection PCx = $1X10_B$(ALT2)
O3 = Output with IOCR bit field selection PCx = 1X11(ALT3)

Column “**Type**”:

A1 = Pad class A1 (LVTTL)
A1+ = Pad class A1+ (LVTTL)
A2 = Pad class A2 (LVTTL)
B = Pad class B (LVTTL)
F = Pad class F (LVDS/CMOS)
D = Pad class D (ADC)
S = Pad class D (ADC) / Pad class S(SENT)

PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
TR = tri-state during reset ($\overline{\text{PORST}}$ = 0)

4 Identification Registers

The Identification Registers uniquely identify the whole device.

Table 3 SAK-TC1798F-512F300EL Identification Registers

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350$_H$	F000 0408$_H$	AB
CBS_JTAGID	1018 E083$_H$	F000 0464$_H$	AB
SCU_CHIPID	0700 9802$_H$	F000 0640$_H$	AB
SCU_MANID	0000 1820$_H$	F000 0644$_H$	AB
SCU_RTID	0000 0000$_H$	F000 0648$_H$	AB

Table 4 SAK-TC1798F-512F300EP Identification Registers

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350$_H$	F000 0408$_H$	AB
CBS_JTAGID	1018 E083$_H$	F000 0464$_H$	AB
SCU_CHIPID	8700 9802$_H$	F000 0640$_H$	AB
SCU_MANID	0000 1820$_H$	F000 0644$_H$	AB
SCU_RTID	0000 0000$_H$	F000 0648$_H$	AB

Table 5 SAK-TC1798N-512F300EP Identification Registers

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350$_H$	F000 0408$_H$	AB
CBS_JTAGID	1018 E083$_H$	F000 0464$_H$	AB
SCU_CHIPID	8700 B002$_H$	F000 0640$_H$	AB
SCU_MANID	0000 1820$_H$	F000 0644$_H$	AB
SCU_RTID	0000 0000$_H$	F000 0648$_H$	AB

Table 6 SAK-TC1798S-512F300EP Identification Registers

Short Name	Value	Address	Stepping
CBS_JDPID	0000 6350$_H$	F000 0408$_H$	AB
CBS_JTAGID	1018 E083$_H$	F000 0464$_H$	AB
SCU_CHIPID	8700 AC02$_H$	F000 0640$_H$	AB

Table 6 SAK-TC1798S-512F300EP Identification Registers (cont'd)

Short Name	Value	Address	Stepping
SCU_MANID	$0000\ 1820_H$	$F000\ 0644_H$	AB
SCU_RTID	$0000\ 0000_H$	$F000\ 0648_H$	AB

5 Electrical Parameters

This specification provides all electrical parameters of the TC1798.

5.1 General Parameters

5.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1798 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1798 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1798 designed in.

5.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 5.2.1**.

Table 7 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade [1]	Load [1]	Leakage 150oC [1]	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	1 µA	Series termination recommended
			A2 (e.g. serial I/Os)	40 MHz	50 pF	3 µA	Series termination recommended
B	3.3 V [2]	LVTTL I/O		75 MHz	35 pF	6 µA	Series termination recommended
	2.5 V [2]			75 MHz	35 pF		
	1.8 V [2]						
F	3.3 V	LVDS	–	50 MHz	–	–	Parallel termination, 100 Ω ± 10% [3]
		CMOS	–	6 MHz	50 pF	–	
DE	5 V	ADC	–	–	–	–	
I	3.3 V	LVTTL (input only)	–	–	–	–	

1) These values show typical application configurations for the pad. Complete and detailed pad parameters are available in the individual pad parameter table on the following pages.

2) Supplied via V_{DDEBU}.

3) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100 Ω ± 10%.

5.1.3 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 8 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Voltage at 1.3 V power supply pins with respect to V_{SS}	V_{DD}	SR	–	–	2.0	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.33	V	–
Voltage at 5 V power supply pins with respect to V_{SS}	V_{DDM}	SR	–	–	7.0	V	–
Voltage on any Class A input pin and dedicated input pins with respect to V_{SS}	V_{IN}	SR	-0.7	–	V_{DDP} + 0.5 or max. 4.33	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{AGND}	V_{AIN} V_{AREFx}	SR	-0.6	–	7.0	V	–
Voltage on any shared Class D analog input pin with respect to V_{SSAF}, if the FADC is switched through to the pin.	V_{AINF} V_{FAREF}	SR	-0.6	–	7.0	V	–
Voltage on any shared Class D analog input pin with respect to V_{SSAF}, if the FADC is switched through to the pin.	V_{AINF}	SR	-0.5	–	7.0	V	–
Input current on any pin during overload condition[1)]	I_{IN}		-10	–	+10	mA	[2)]

Table 8 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Absolute maximum sum of all input circuit currents for one port group during overload condition[3)]	I_{IN}	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}	-200	–	200	mA	

1) This parameter is an Absolute Maximum Rating. Exposure to Absolute Maximum Ratings for extended periods of time may damage the device.

2) Refers to possibility of current caused degradation, where the voltages in overload do not violate the normal operating conditions. In case that the overvoltages violate the normal operating conditions, the reliability considerations caused by overvoltage apply independently, as described in this document.

3) The port groups are defined in **Table 13**.

5.1.4 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 9 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time (24000 h) is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDM})
  - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Table 9 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition except LVDS pins	I_{IN}	-5	–	+5	mA	
Input current on LVDS pins	I_{INLVDS}	-3	–	+3	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1)]	I_{ING}	-20	–	+20	mA	
Input current on analog pins	I_{INANA}	-3	–	+3	mA	
Absolute sum of all analog input currents for analog inputs during overload condition	I_{INSA}	-45	–	+45	mA	
Absolute sum of all input circuit currents during overload condition	ΣI_{INS}	-100	–	100	mA	

1) The port groups are defined in **Table 13**.

Note: FADC input pins count as analog pin as they are overlayed with an ADC pins.

Table 10 PN-Junction Characterisitics for positive Overload

Pad Type	I_{IN} = 3 mA	I_{IN} = 5 mA
A1 / A1+ / F	$U_{IN} = V_{DDP} + 0.6$ V	$U_{IN} = V_{DDP} + 0.7$ V
A2	$U_{IN} = V_{DDP} + 0.5$ V	$U_{IN} = V_{DDP} + 0.6$ V
LVDS	$U_{IN} = V_{DDP} + 0.7$ V	-
D	$U_{IN} = V_{DDM} + 0.6$ V	-
S	$U_{IN} = V_{DDM} + 0.6$ V	-

Table 11 PN-Junction Characterisitics for negative Overload

Pad Type	I_{IN} = -3 mA	I_{IN} = -5 mA
A1 / A1+ / F	$U_{IN} = V_{SS} - 0.6$ V	$U_{IN} = V_{SS} - 0.7$ V
A2	$U_{IN} = V_{SS} - 0.5$ V	$U_{IN} = V_{SS} - 0.6$ V
LVDS	$U_{IN} = V_{SS} - 0.7$ V	-
D	$U_{IN} = V_{SSM} - 0.6$ V	-
S	$U_{IN} = V_{SSM} - 0.6$ V	-

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery without having any negative reliability impact on the operational life-time.

5.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC1798. All parameters specified in the following tables refer to these operating conditions, unless otherwise noticed.

Digital supply voltages applied to the TC1798 must be static regulated voltages which allow a typical voltage swing of ± 5 %.

All parameters specified in the following tables (**Table 14** and following) refer to these operating conditions (**Table 12**), unless otherwise noticed in the Note / Test Condition column.

The **Extended Range Operating Conditions** did not increase area of validity of the parameters defined in table 10 and later.

Table 12 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for analog inputs, negative	K_{OVAN} CC	–	–	0.0001		$I_{OV}\leq$ 0 mA; $I_{OV}\geq$ -2 mA; analog pad= 5.0 V
Overload coupling factor for analog inputs, positive	K_{OVAP} CC	–	–	0.00001		$I_{OV}\leq$ 3 mA; $I_{OV}\geq$ 0 mA; analog pad= 5.0 V
CPU Frequency	f_{CPU} SR	–	–	300	MHz	
Modulated f_{CPU}	$f_{CPU\_modulated}$ SR	–	–	300-2*MA[1)]	MHz	
FPI bus frequency	f_{FPI} SR	–	–	100	MHz	
Modulated f_{FPI}	$f_{FPI\_modulated}$ SR	–	–	100-2*MA[1)]	MHz	
FSI frequency	f_{FSI} SR	–	–	150	MHz	
Modulated f_{FSI}	$f_{FSI\_modulated}$ SR	–	–	150-2*MA[1)]	MHz	
PCP Frequency	f_{PCP} SR	–	–	200	MHz	
Modulated f_{PCP}	$f_{PCP\_modulated}$ SR	–	–	200-2*MA[1)]	MHz	
SRI Frequency	f_{SRI} SR	–	–	300	MHz	

Table 12 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Modulated f_{SRI}	$f_{SRI\_modulated}$ SR	–	–	300-2*MA[1]	MHz	
Inactive device pin current	I_{ID} SR	-1	–	1	mA	All power supply voltages V_{DDx} = 0
Short circuit current of digital outputs[2]	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} CC	–	–	100	mA	
Absolute sum of short circuit currents per pin group	ΣI_{SC_PG} CC	–	–	20	mA	
Ambient Temperature	T_A SR	-40	–	125	°C	
Junction temperature	T_J SR	-40	–	150	°C	
Core Supply Voltage	V_{DD} SR	1.235	1.3	1.365[3]	V	for duration limitation see **Section 5.1.5.1**
EBU supply voltage	V_{DDEBU} SR	3.135	3.3	3.465[5]	V	for duration limitation see **Section 5.1.5.1**
		2.375	2.5	2.625	V	
		1.71	1.8	1.89	V	
Flash supply voltage 3.3V	V_{DDFL3} SR	3.135	3.3	3.63[5]	V	for duration limitation see **Section 5.1.5.1**
ADC analog supply voltage	V_{DDM} SR	3.135	5	5.5[4]	V	
Oscillator core supply voltage	V_{DDOSC} SR	1.235	1.3	1.43[3]	V	for duration limitation see **Section 5.1.5.1**
Oscillator 3.3V supply voltage	V_{DDOSC3} SR	3.135	3.3	3.63[5]	V	for duration limitation see **Section 5.1.5.1**

Table 12 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage for IO pads	V_{DDP} SR	3.135	3.3	3.63 [5]	V	for duration limitation see Section 5.1.5.1
E-Ray PLL core voltage supply	V_{DDPF} SR	1.235	1.3	1.43[3]	V	for duration limitation see Section 5.1.5.1
E-Ray PLL 3.3V supply	V_{DDPF3} SR	3.135	3.3	3.63[5]	V	for duration limitation see Section 5.1.5.1
VDDP voltage to ensure defined pad states[6]	V_{DDPPA} CC	0.65	–	–	V	
Digital ground voltage	V_{SS} SR	0	–	–	V	
Analog ground voltage for V_{DDM}	V_{SSM} SR	-0.1	0	0.1	V	
Analog core supply	V_{DDAF} SR	1.235	1.3	1.365[3]	V	for duration limitation see Section 5.1.5.1
FADC / ADC analog supply voltage	V_{DDMF} SR	3.135	3.3	3.47[5]	V	for duration limitation see Section 5.1.5.1
Analog ground voltage for V_{DDMF}	V_{SSAF} SR	-0.1	0	0.1	V	

1) MA equals the modulation amplitude in percentage times the configured PLL clock out frequency.

2) Applicable for digital outputs.

3) Voltage overshoot to 1.7V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

4) Voltage overshoot to 6.5V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

5) Voltage overshoot to 4.0V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

6) This parameter is valid under the assumption the $\overline{\text{PORST}}$ signal is constantly at low level during the power-up/power-down of V_{DDP}.

5.1.5.1 Extended Range Operating Conditions

The following extended operating conditions are defined:

- $1.3V + 5\% < V_{DD} / V_{DDOSC} / V_{DDPF} / V_{DDAF} < 1.3V + 7.5\%$ (overvoltage condition):

  - limited to 10000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- $1.3V + 7.5\% < V_{DD}$ / V_{DDOSC} / V_{DDPF} / V_{DDAF} < 1.3V + 10% (overvoltage condition):
  - limited to 1000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- V_{DDP} / V_{DDOSC3} / V_{DDPF3} / V_{DDFL3} / V_{DDMF} / V_{DDEBU}< 3.3 V ± 10%
  - $3.3V + 5\% < V_{DDP}$ / V_{DDOSC3} / V_{DDPF3} / V_{DDFL3} / V_{DDMF} / V_{DDEBU}< 3.3V + 10% (overvoltage condition):
    limited to 1000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.

Table 13 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
1	P2.[4:2], P6.[6:9]
2	P6.[5:4], P6.[11:10]
3	P6.[15:12]
4	P8.[5:0]
5	P8.[7:6], P1.[15:13]
6	P1.5, P1.[11:8]
7	P1.[4:2], P1.6, P1.12
8	P1.[1:0], P7.[2:0]
9	P7.[7:3]
10	P4.[6:0]
11	P4.[10:7]
12	P4.[15:11]
13	P10.[5:0]
14	P15.[7:4], P16.[1:0]
15	P15.3, P15.[12:11], P16.[5:3]
16	P15.[2:0], P15.[9:8], P16.2, P16.8
17	P15.10, P15.[15:13], P16.[7:6]
18	P14.[15:12]
19	P14.[11:8], P16.12
20	P14.[7:3], P16.11
21	P13.15, P14.[2:0]

Table 13 Pin Groups for Overload / Short-Circuit Current Sum Parameter (cont'd)

Group	Pins
22	P13.[14:11]
23	P13.[10:8], P16.10
24	P13.[7:4], P16.9
25	P12.5, P13.[3:0]
26	P12.[4:0]
27	P11.[15:11]
28	P11.[10:6]
29	P11.[5:2]
30	P11.[1:0], P12.[7:6]
31	P9.10, P9.14
32	P9.7, P9.13
33	P9.[4:2], P9.6
34	P9.1, P9.5, P9.[9:8]
35	P9.0, P9.[12:11]
36	P5.[11:8]
37	P5.6, P5.[15:12]
38	P5.0, P5.[5:2], P5.7
39	P3.[5:0], P5.1
40	P3.[12:6]
41	P0.[3:0], P3.[15:13]
42	P0.[11:4]
43	P0.[14:12]
44	P0.15, P18.[5:0]
45	P2.[15:11], P18.[7:6]
46	P2.[10:5]

5.2 DC Parameters

5.2.1 Input/Output Pins

Table 14 Standard_Pads Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	T_A= 25 °C; f= 1 MHz
Pull-down current	$\|I_{PDL}\|$ CC	–	–	150	µA	$V_i \geq 0.6 \times V_{DDP}$ V
		10	–	–	µA	$V_i \geq 0.36 \times V_{DDP}$ V
Pull-Up current	$\|I_{PUH}\|$ CC	10	–	–	µA	$V_i \leq 0.6 \times V_{DDP}$ V
		–	–	100	µA	$V_i \leq 0.36 \times V_{DDP}$ V
Spike filter always blocked pulse duration	t_{SF1} CC	–	–	10	ns	only PORST pin
Spike filter pass-through pulse duration	t_{SF2} CC	100	–	–	ns	only PORST pin

Table 15 Standard_Pads Class_A1

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A1 pads [1]	$HYSA1$ CC	0.1 x V_{DDP}	–	–	V	
Input Leakage Current Class A1	I_{OZA1} CC	-500	–	500	nA	$V_i \geq 0$ V; $V_i \leq V_{DDP}$ V
Ratio Vil/Vih, A1 pads	V_{ILA1} / V_{IHA1} CC	0.6	–	–		

Table 15 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of the class A1 pad, weak driver	R_{DSONW} CC	–	450	600	Ohm	I_{OH}> -0.5 mA; P_MOS
		–	210	340	Ohm	I_{OL}< 0.5 mA; N_MOS
On-Resistance of the class A1 pad, medium driver	R_{DSONM} CC	–	–	155	Ohm	I_{OH}> 2 mA; P_MOS
		–	–	110	Ohm	I_{OL}< 2 mA; N_MOS
Fall time,pad type A1	t_{FA1} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak

Table 15 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A1	t_{RA1} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak
Input high voltage class A1 pads	V_{IHA1} SR	0.6 x V_{DDP}	–	$min(V_{DDP}+0.3,3.6)$	V	
Input low voltage class A1 pads	V_{ILA1} SR	-0.3	–	0.36 x V_{DDP}	V	

Table 15 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage high class A1 pads	V_{OHA1} CC	V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= medium
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= medium
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -400 µA; pin out driver= weak
		2.4	–	–	V	I_{OH}≥ -500 µA; pin out driver= weak
Output voltage low class A1 pads	V_{OLA1} CC	–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= medium
		–	–	0.4	V	I_{OL}≤ 500 µA; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Table 16 Standard_Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A1+ pads 1)	*HYSA1* + CC	0.1 x V_{DDP}	–	–	V	
Input Leakage Current Class A1+	I_{OZA1+} CC	-1000	–	1000	nA	
On-Resistance of the class A1+ pad, weak driver	R_{DSONW} CC	–	450	600	Ohm	I_{OH}> -0.5 mA; P_MOS
		–	210	340	Ohm	I_{OL}< 0.5 mA; N_MOS

Table 16 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of the class A1+ pad, medium driver	R_{DSONM} CC	–	–	155	Ohm	I_{OH}> 2 mA; P_MOS
		–	–	110	Ohm	I_{OL}< 2 mA; N_MOS
On-Resistance of the class A1+ pad, strong driver	R_{DSON1+} CC	–	–	100	Ohm	I_{OH}> 2 mA; P_MOS
		–	–	80	Ohm	I_{OL}< 2 mA; N_MOS
Fall time, pad type A1+	t_{FA1+} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	28	ns	C_L= 50 pF; edge= slow ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak

Table 16 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A1+	t_{RA1+} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	28	ns	C_L= 50 pF; edge= slow ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak
Input high voltage, Class A1+ pads	V_{IHA1+} SR	0.6 x V_{DDP}	–	$min(V_{DDP}+0.3,3.6)$	V	
Input low voltage Class A1+ pads	V_{ILA1+} SR	-0.3	–	0.36 x V_{DDP}	V	
Ratio Vil/Vih, A1+ pads	V_{ILA1+} / V_{IHA1+} CC	0.6	–	–		

Table 16 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage high class A1+ pads	$V_{OHA1+CC}$	V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= medium
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= strong
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= medium
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= strong
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -400 µA; pin out driver= weak
		2.4	–	–	V	I_{OH}≥ -500 µA; pin out driver= weak
Output voltage low class A1+ pads	$V_{OLA1+CC}$	–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= medium
		–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= strong
		–	–	0.4	V	I_{OL}≤ 500 µA; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Table 17 Standard_Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for A2 pads [1]	$HYSA2$ CC	0.1 x V_{DDP}	–	–	V	
Input Leakage current Class A2	I_{OZA2} CC	-6000	–	6000	nA	$V_i < V_{DDP}$ / 2 - 1 V; $V_i > V_{DDP}$ / 2 + 1 V; $V_i \geq 0$ V; $V_i \leq V_{DDP}$ V
		-3000	–	3000	nA	$V_i > V_{DDP}$ / 2 - 1 V; $V_i < V_{DDP}$ / 2 + 1 V
Ratio Vil/Vih, A2 pads	V_{ILA2} / V_{IHA2} CC	0.6	–	–		
On-Resistance of the class A2 pad, weak driver	R_{DSONW} CC	–	450	600	Ohm	I_{OH}> -0.5 mA; P_MOS
		–	210	340	Ohm	I_{OL}< 0.5 mA; N_MOS
On-Resistance of the class A2 pad, medium driver	R_{DSONM} CC	–	–	155	Ohm	I_{OH}> 2 mA; P_MOS
		–	–	110	Ohm	I_{OL}< 2 mA; N_MOS
On-Resistance of the class A2 pad, strong driver	R_{DSON2} CC	–	–	28	Ohm	I_{OH}> 2 mA; P_MOS
		–	–	22	Ohm	I_{OL}< 2 mA; N_MOS

Table 17 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time, pad type A2	t_{FA2} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	7	ns	C_L= 50 pF; edge= medium ; pin out driver= strong
		–	–	10	ns	C_L= 50 pF; edge= medium-minus ; pin out driver= strong
		–	–	3.7	ns	C_L= 50 pF; edge= sharp ; pin out driver= strong
		–	–	5	ns	C_L= 50 pF; edge= sharp-minus ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	7.5	ns	C_L= 100 pF; edge= sharp ; pin out driver= strong
		–	–	140	ns	C_L= 150 pF; pin out driver= medium

Table 17 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak

Table 17 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A2	t_{RA2} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	7.0	ns	C_L= 50 pF; edge= medium ; pin out driver= strong
		–	–	10	ns	C_L= 50 pF; edge= medium-minus ; pin out driver= strong
		–	–	3.7	ns	C_L= 50 pF; edge= sharp ; pin out driver= strong
		–	–	5	ns	C_L= 50 pF; edge= sharp-minus ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	7.5	ns	C_L= 100 pF; edge= sharp ; pin out driver= strong
		–	–	140	ns	C_L= 150 pF; pin out driver= medium

Table 17 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak
Input high voltage, class A2 pads	V_{IHA2} SR	0.6 x V_{DDP}	–	$min(V_{DDP}+0.3, 3.6)$	V	
Input low voltage Class A2 pads	V_{ILA2} SR	-0.3	–	0.36 x V_{DDP}	V	
Output voltage high class A2 pads	V_{OHA2} CC	V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= medium
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= strong
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= medium
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= strong
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -400 µA; pin out driver= weak
		2.4	–	–	V	I_{OH}≥ -500 µA; pin out driver= weak

Table 17 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage low class A2 pads	V_{OLA2} CC	–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= medium
		–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= strong
		–	–	0.4	V	I_{OL}≤ 500 µA; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Table 18 Standard_Pads Class_B

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis, B class pads[1)]	*HYSB* CC	0.05 x V_{DDEBU}	–	–	V	V_{DDEBU}= 1.8 V
		0.08 x V_{DDEBU}	–	–	V	V_{DDEBU}= 2.5 V
		0.1 x V_{DDEBU}	–	–	V	V_{DDEBU}= 3.3 V
Input Leakage Current, class B pads	I_{OZB} CC	-3000	–	3000	nA	V_{DDEBU}= 1.8 V; V_i> 0 V; V_i< V_{DDEBU} V
		-6000	–	6000	nA	V_i> 0 V; V_i> V_{DDEBU}/2 + 0.6 V; V_i≤ V_{DDEBU} V; V_i≤ V_{DDEBU}/2 - 0.6 V
		-3000	–	3000	nA	V_i> V_{DDEBU}/2 - 0.6 V; V_i< V_{DDEBU}/2 + 0.6 V

Table 18 Standard_Pads Class_B (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ratio between low and high input threshold	V_{ILB} / V_{IHB} CC	0.6	–	–		
On-Resistance of the class B pad, weak driver	R_{DSONW} CC	–	450	600	Ohm	I_{OH}> -0.5 mA; P_MOS; V_{DDEBU}= 3.3 V
		–	210	340	Ohm	I_{OL}< 0.5 mA; N_MOS; V_{DDEBU}= 3.3 V
On-Resistance of the class B pad, medium driver	R_{DSONM} CC	–	–	155	Ohm	I_{OH}> -2 mA; P_MOS; V_{DDEBU}= 3.3 V
		–	–	110	Ohm	I_{OL}< 2 mA; N_MOS; V_{DDEBU}= 3.3 V
On-Resistance of the class B pad, strong driver	R_{DSON2} CC	–	–	28	Ohm	I_{OH}> -2 mA; P_MOS; V_{DDEBU}= 3.3 V
		–	–	22	Ohm	I_{OL}< 2 mA; N_MOS; V_{DDEBU}= 3.3 V

Table 18 Standard_Pads Class_B (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time, class B pads; edge= sharp ; pin out driver= strong [2]	t_{FB} CC	–	–	3.3	ns	C_L= 20 pF; V_{DDEBU} 1.53 V; V_{DDEBU}≤ 1.98 V
		–	–	5.0	ns	C_L= 35 pF; V_{DDEBU} 1.53 V; V_{DDEBU}≤ 1.98 V
		–	–	3.0	ns	C_L= 35 pF; V_{DDEBU} 2.375 ; V_{DDEBU}≤ 2.625
		–	–	2.5	ns	C_L= 35 pF; V_{DDEBU} 3.13 ; V_{DDEBU}≤ 3.47
		–	–	7.0	ns	C_L= 50 pF; V_{DDEBU} 1.53 V; V_{DDEBU}≤ 1.98 V
		–	–	4.0	ns	C_L= 50 pF; V_{DDEBU} 2.375 ; V_{DDEBU}≤ 2.625
		–	–	3.3	ns	C_L= 50 pF; V_{DDEBU} 3.13 ; V_{DDEBU}≤ 3.47
		–	–	12.0	ns	C_L= 100 pF; V_{DDEBU} 1.53 V; V_{DDEBU}≤ 1.98 V
		–	–	7.0	ns	C_L= 100 pF; V_{DDEBU} 2.375 ; V_{DDEBU}≤ 2.625
		–	–	6.0	ns	C_L= 100 pF; V_{DDEBU} 3.13 ; V_{DDEBU}≤ 3.47

Table 18 Standard_Pads Class_B (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, class B pads; edge= sharp ; pin out driver= strong [2]	t_{RB} CC	–	–	3.3	ns	C_L= 20 pF; V_{DDEBU} 1.53 V; V_{DDEBU}≤ 1.98 V
		–	–	5.0	ns	C_L= 35 pF; V_{DDEBU} 1.53 V; V_{DDEBU}≤ 1.98 V
		–	–	3.0	ns	C_L= 35 pF; V_{DDEBU} 2.375 ; V_{DDEBU}≤ 2.625
		–	–	3.0	ns	C_L= 35 pF; V_{DDEBU} 3.13 ; V_{DDEBU}≤ 3.47
		–	–	7.0	ns	C_L= 50 pF; V_{DDEBU} 1.53 V; V_{DDEBU}≤ 1.98 V
		–	–	4.0	ns	C_L= 50 pF; V_{DDEBU} 2.375 ; V_{DDEBU}≤ 2.625
		–	–	3.7	ns	C_L= 50 pF; V_{DDEBU} 3.13 ; V_{DDEBU}≤ 3.47
		–	–	12.0	ns	C_L= 100 pF; V_{DDEBU} 1.53 V; V_{DDEBU}≤ 1.98 V
		–	–	7.0	ns	C_L= 100 pF; V_{DDEBU} 2.375 ; V_{DDEBU}≤ 2.625
		–	–	6.0	ns	C_L= 100 pF; V_{DDEBU} 3.13 ; V_{DDEBU}≤ 3.47
Input high voltage, class B pads	V_{IHB} CC	0.6 x V_{DDEBU}	–	$max(V_{DDEBU}$ + 0.3, 3.6)	V	

Table 18 Standard_Pads Class_B (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage, Class B pads	V_{ILB} CC	-0.3	–	0.36 x V_{DDEBU}	V	
Output voltage high, class B pads	V_{OHB} CC	V_{DDEBU} - 0.4	–	–	V	I_{OH} -2 mA;
Output voltage low, class B pads	V_{OLB} CC	–	–	0.4	V	I_{OL}= 2 mA

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

2) For non strong driver and sharp edge settings see the class A2 definitions.

Table 19 Standard_Pads Class_F

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis F[1)]	$HYSF$ CC	0.05 x V_{DDP}	–	–	V	
Input Leakage Current Class F	I_{OZF} CC	-6000	–	6000	nA	V_i< V_{DDP} / 2 - 1 V; V_i> V_{DDP} / 2 + 1 V; V_i≥ 0 V; V_i≤ V_{DDP} V
		-3000	–	3000	nA	V_i> V_{DDP} / 2 - 1 V; V_i< V_{DDP} / 2 + 1 V
Ratio Vil/ Vih, F pads	V_{ILF} / V_{IHF} CC	0.6	–	–		
On-Resistance of the class F pad, medium driver	R_{DSONM} CC	–	–	170	Ohm	I_{OH}> -2 mA; P_MOS
		–	–	145	Ohm	I_{OL}< 2 mA; N_MOS
Fall time, pad type F, CMOS mode	t_{FF} CC	–	–	60	ns	C_L= 50 pF
Rise time, pad type F, CMOS mode	t_{RF} CC	–	–	60	ns	C_L= 50 pF

Table 19 Standard_Pads Class_F (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage, pad class F, CMOS mode	V_{IHF} SR	0.6 x V_{DDP}	–	*min(V DDP+* 0.3, 3.6)	V	
Input low voltage, Class F pads, CMOS mode	V_{ILF} SR	-0.3	–	0.36 x V_{DDP}	V	
Output high voltage, class F pads, CMOS mode	V_{OHF} CC	V_{DDP}-0.4	–	–	V	I_{OH}≥ -1.4 mA
		2.4	–	–	V	I_{OH}≥ -2 mA
Output low voltage, class F pads, CMOS mode	V_{OLF} CC	–	–	0.4	V	I_{OL}≤ 2 mA

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Table 20 Standard_Pads Class_I

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis Class I[1)]	*HYSI* CC	0.1 x V_{DDP}	–	–	V	
Input Leakage Current	I_{OZI} CC	-1000	–	1000	nA	
Ratio between low and high input threshold	V_{ILI} / V_{IHI} CC	0.6	–	–		
Input high voltage, class I pins	V_{IHI} SR	0.6 x V_{DDP}	–	*min(V DDP+* 0.3, 3.6)	V	
Input low voltage, Class I pads	V_{ILI} SR	-0.3	–	0.36 x V_{DDP}	V	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Class S pad parameters are only valid for V_{DDM} = 4.75 V to 5.25 V.

Table 21 Standard_Pads Class_S

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for class S pads[1]	$HYSS$ CC	0.3	–	–	V	
Input leakage current	I_{OZS} CC	-300	–	300	nA	
Input voltage high	V_{IHS} CC	–	–	3.6	V	
Input voltage low	V_{ILS} CC	1.9	–	–	V	
V_{ILS} Delta [2]	V_{ILSD} CC	-50	–	50	mV	Maximum input low state treshold variation over 1ms (V_{DDP} = constant)

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

2) V_{ILSD} is implemented to ensure J2716 specification. It can't be guaranteed that it suppresses switching due to external noise.

Table 22 LVDS_Pads Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output impedance, pad class F, LVDS mode	R_O CC	40	–	140	Ohm	
Fall time, pad type LVDS	t_{FL} CC	–	–	2	ns	termination 100 Ω ± 1 %; differential capacitance = 10 pF; input capacitance = 20 pF

Table 22 LVDS_Pads Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type LVDS	t_{RL} CC	–	–	2	ns	termination 100 Ω ± 1 %; differential capacitance = 10 pF; input capacitance = 20 pF
Pad set-up time	t_{SET_LVDS} CC	–	–	13	µs	termination 100 Ω ± 1 %
Output Differential Voltage	V_{OD} CC	150	–	400	mV	termination 100 Ω ± 1 %
Output voltage high, pad class F, LVDS mode	V_{OH} CC	–	–	1525	mV	termination 100 Ω ± 1 %
Output voltage low, pad class F, LVDS mode	V_{OL} CC	875	–	–	mV	termination 100 Ω ± 1 %
Output Offset Voltage	V_{OS} CC	1075	–	1325	mV	termination 100 Ω ± 1 %

5.2.2 Analog to Digital Converters (ADCx)

ADC parameter are valid for $V_{DD\,/\,DDAF}$ = 1.235 V to 1.365 V; V_{DDM} = 4.5 V to 5.5 V.

Table 23 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at the analog voltage inputs[1]	C_{AINSW} CC	–	9	20	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	20	30	pF	
Switched capacitance at the positive reference voltage input[2][3]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[2]	$C_{AREFTOT}$ CC	–	20	40	pF	
Differential Non-Linearity Error[4][5][6][7]	EA_{DNL} CC	-3	–	3	LSB	ADC resolution= 12-bit [8] [9]
Gain Error[4][5][6][7]	EA_{GAIN} CC	-3.5	–	3.5	LSB	ADC resolution= 12-bit [8] [9]
Integral Non-Linearity[4][5][7][7]	EA_{INL} CC	-3	–	3	LSB	ADC resolution= 12-bit [8] [9]; ADC = 0,1,2
		-3	–	3	LSB	ADC resolution= 12-bit [8] [9] ADC3 and $V_{AIN} \le V_{AREFx}$ - 0.15 V
		-15	–	15	LSB	ADC resolution= 12-bit [8] [9] ADC3 and V_{AREFx} - 0.15 V $\le V_{AIN} < V_{AREFx}$

Table 23 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Offset Error[4)5)6)7)]	EA_{OFF} CC	-4	–	4	LSB	ADC resolution= 12-bit [8) 9)]
Converter clock	f_{ADC} SR	4	–	100	MHz	f_{ADC}= f_{FPI}
Internal ADC clock	f_{ADCI} CC	1	–	18	MHz	ADC0
		1	–	18	MHz	ADC1
		1	–	20[10)]	MHz	ADC2
		1	–	16	MHz	ADC3
Charge consumption per conversion	Q_{CONV} CC	70	85[11)]	100	pC	charge needs to be provided via V_{AREF0}

Table 23 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage at analog inputs[12)]	I_{OZ1} CC	-100	–	500	nA	$V_i \leq V_{DDM}$ V; $V_i \geq 0.97$ x V_{DDM} V; overlayed= No
		-100	–	600	nA	$V_i \geq 0.97$ x V_{DDM} V; $V_i \leq V_{DDM}$ V; overlayed= Yes
		-500	–	100	nA	$V_i \leq 0.03$ x V_{DDM} V; $V_i \geq 0$ V; overlayed= No
		-600	–	100	nA	$V_i \leq 0.03$ x V_{DDM} V; $V_i \geq 0$ V; overlayed= Yes
		-100	–	200	nA	$V_i > 0.03$ x V_{DDM} V; $V_i < 0.97$ x V_{DDM} V; overlayed= No
		-100	–	300	nA	$V_i < 0.97$ x V_{DDM} V; $V_i > 0.03$ x V_{DDM} V; overlayed= Yes
Input leakage current at V_{AREFx}	I_{OZ2} CC	-1	–	1	µA	$V_{AREFx} \geq 0$ V; $V_{AREFx} \leq V_{DDM}$ V
Input leakage current at V_{AGNDx}	I_{OZ3} CC	-1	–	1	µA	$V_{AGNDx} \geq 0$ V; $V_{AGNDx} \leq V_{DDM}$ V
ON resistance of the transmission gates in the analog voltage path	R_{AIN} CC	–	900	1500	Ohm	
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	

Table 23 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistance of the reference voltage input path	R_{AREF} CC	–	500	1000	Ohm	
Sample time	t_S CC	2	–	257	T_{ADCI}	
Calibration time after bit ADC_GLOBCFG.SUCAL is set	t_{CAL} CC	–	–	4352	cycle s	
Total Unadjusted Error[6)5)13)]	*TUE* CC	-4	–	4[14)]	LSB	ADC resolution= 12-bit ADC = 0,1,2
		-4	–	4[14)]	LSB	ADC resolution= 12-bit [8) 9)] ADC3 and $V_{AIN} \le V_{AREFx}$ - 0.15 V
		-14	–	14[14)]	LSB	ADC resolution= 12-bit [8) 9)] ADC3 and V_{AREFx} - 0.15 V ≤ V_{AIN} < V_{AREFx}
Analog reference ground[2)]	V_{AGNDx} SR	V_{SSM} - 0.05	–	V_{AREFx} - 1	V	
Analog input voltage	V_{AIN} SR	V_{AGNDx}	–	V_{AREFx}	V	
Analog reference voltage[2)]	V_{AREFx} SR	V_{AGNDx} + 1	–	V_{DDM} + 0.05[15)16)]	V	
Analog reference voltage range[6)5)2)]	V_{AREFx} - V_{AGNDx} SR	V_{DDM}/2	–	V_{DDM} + 0.05	V	

1) The sampling capacity of the conversion C-network is pre-charged to V_{AREFx}/2 before the sampling moment. Because of the parasitic elements the voltage measured at AINx can deviate from V_{AREFx}/2.

2) Applies to AINx, when used as auxiliary reference input.

3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead smaller capacitances are successively switched to the reference voltage.
4) The sum of DNL/INL/GAIN/OFF errors does not exceed the related TUE total unadjusted error.
5) If a reduced analog reference voltage between 1V and V_{DDM} / 2 is used, then there are additional decrease in the ADC speed and accuracy.
6) If the analog reference voltage range is below V_{DDM} but still in the defined range of V_{DDM} / 2 and V_{DDM} is used, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE,DNL,INL,Gain, and Offset errors increase also by the factor 1/k.
7) If the analog reference voltage is > V_{DDM}, then the ADC converter errors increase.
8) For 10-bit conversions the error value must be multiplied with a factor 0.25.
9) For 8-bit conversions the error value must be multiplied with a factor 0.0625.
10) For f_{ADCI} between 18MHz and 20MHz the TUE and Gain Error can increase beyond the given limits. For STC < 2 INL, DNL , and Offset errors can also increase.
11) For a conversion time of 1 µs a rms value of 85µA result for I_{AREFx}.
12) The leakage current definition is a continuos function, as shown in figure ADCx Analoge Input Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function.
13) Measured without noise.
14) For 10-bit conversion the TUE is ±2LSB; for 8-bit conversion the TUE is ±1LSB
15) A running conversion may become inexact in case of violating the normal conditions (voltage overshoot).
16) If the reference voltage V_{AREFx} increase or the V_{DDM} decrease, so that V_{AREF} = (V_{DDM} + 0.05V to V_{DDM} + 0.07V), then the accuracy of the ADC decrease by 4LSB12.

Table 24 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Values	Unit	Note
Conversion time with post-calibration	t_C CC	$2 \times T_{ADC} + (4 + STC + n) \times T_{ADCI}$	µs	n = 8, 10, 12 for n - bit conversion $T_{ADC} = 1 / f_{FPI}$ $T_{ADCI} = 1 / f_{ADCI}$
Conversion time without post-calibration		$2 \times T_{ADC} + (2 + STC + n) \times T_{ADCI}$		

The power-up calibration of the ADC requires a maximum number of 4352 f_{ADCI} cycles.

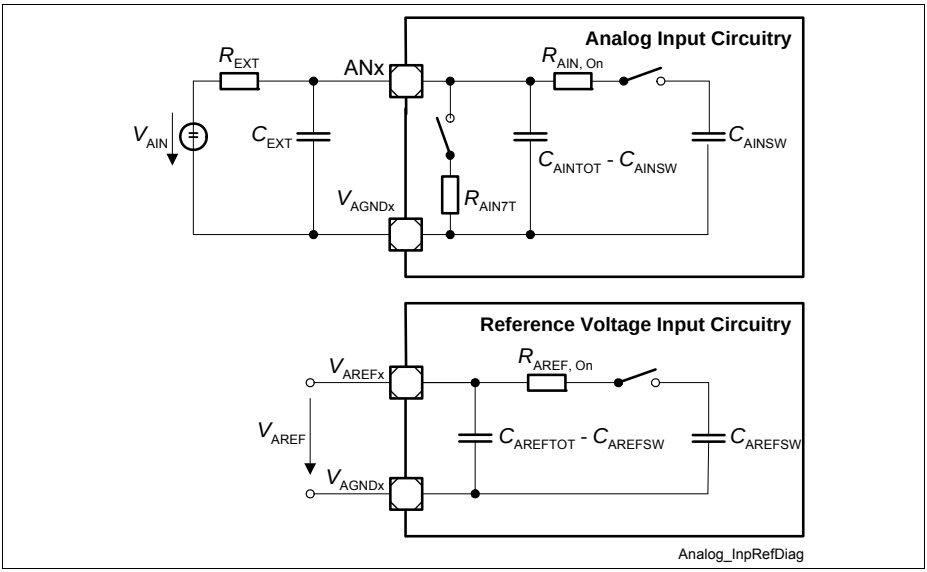


Figure 6 ADCx Input Circuits

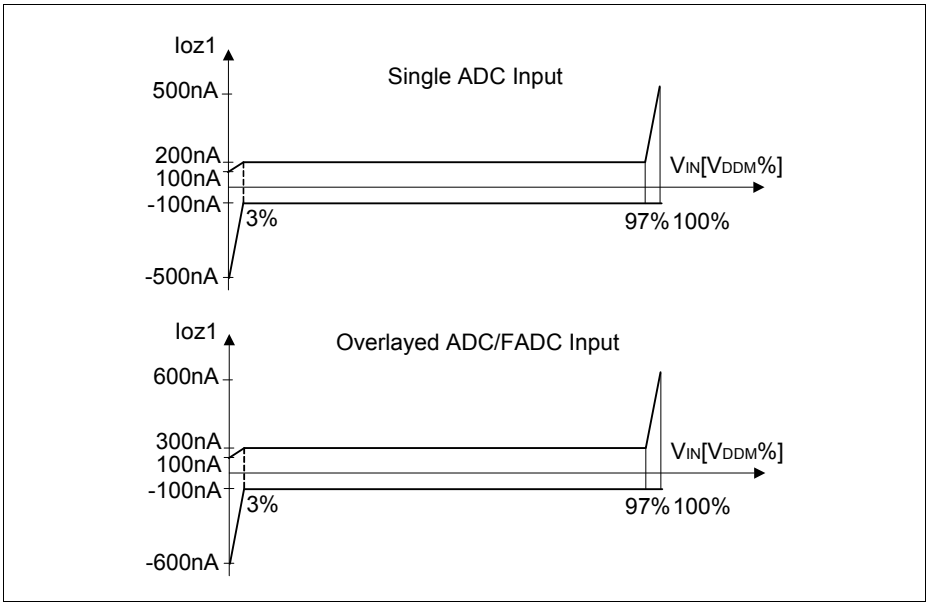


Figure 7 ADCx Analog Inputs Leakage

5.2.3 Fast Analog to Digital Converter (FADC)

FADC parameter are vaild for $V_{DD\,/\,DDAF}$ = 1.235 V to 1.365 V; V_{DDMF} = 2.97 V to 3.6 V.

Table 25 FADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at VFAREF	I_{FAREF} CC	–	–	120	µA	
Input leakage current at VFAREF[1)]	I_{FOZ2} CC	-500	–	500	nA	$V_{FAREF} \leq V_{DDMF}$ V; $V_{FAREF} \geq 0$ V
Input leakage current at VFAGND	I_{FOZ3} CC	-500	–	500	nA	
DNL error	EF_{DNL} CC	-1	–	1	LSB	V_{IN} mode= differential; Gain = 1 or 2
		-2	–	2	LSB	V_{IN} mode= differential; Gain = 4 or 8[2)]
		-1	–	1	LSB	V_{IN} mode= single ended; Gain = 1 or 2
		-2	–	2	LSB	V_{IN} mode= single ended; Gain = 4 or 8[2)]
GRADient error	EF_{GRAD} CC	-5	–	5	%	V_{IN} mode= differential ; Gain≤ 4
		-5	–	5	%	V_{IN} mode= single ended ; Gain≤ 4
		-6	–	6	%	V_{IN} mode= differential ; Gain= 8
		-6	–	6	%	V_{IN} mode= single ended ; Gain= 8

Table 25 FADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
INL error	EF_{INL} CC	-4	–	4	LSB	V_{IN} mode= differential
		-4	–	4	LSB	V_{IN} mode= single ended
Offset error	EF_{OFF} CC	-90	–	90	mV	V_{IN} mode= differential ; Calibration= No
		-90	–	90	mV	V_{IN} mode= single ended ; Calibration= No
		-20	–	20	mV	V_{IN} mode= differential ; Calibration= Yes [3)4)]
		-20	–	20	mV	V_{IN} mode= single ended ; Calibration= Yes [3)4)]
Error of commen mode voltage V_{FAREF}/2	EF_{REF} CC	-60	–	60	mV	
Channel amplifier cutoff frequency	f_{COFF} CC	2	–	–	MHz	
Converter clock	f_{FADC} SR	1	–	100	MHz	f_{FADC}= f_{FPI}
Conversion time	t_C CC	–	–	21	1 / f_{FADC}	For 10-bit conversion
Input resistance of the analog voltage path (Rn, Rp)	R_{FAIN} CC	100	–	200	kOhm	
Settling time of a channel amplifier after changing ENN or ENP	t_{SET} CC	–	–	5	µs	
Analog input voltage range	V_{AINF} SR	V_{FAGND}	–	V_{DDMF}	V	

Table 25 FADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference ground	V_{FAGND} SR	V_{SSAF} - 0.05	–	V_{SSAF} + 0.05	V	
Analog reference voltage	V_{FAREF} SR	2.97	–	3.63[5) 6)]	V	

1) This value applies in power-down mode.

2) No missing codes.

3) Calibration should be preformed at each power-up. In case of a continous operation, it should be performed minimium once per week.

4) The offser error voltage drifts over the whole temperature range maximum +-3LSB.

5) Voltage overshoot to 4V is permissible, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

6) A running conversion may become inexact in case of violating the nomal operating conditions (voltage overshoots).

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized.

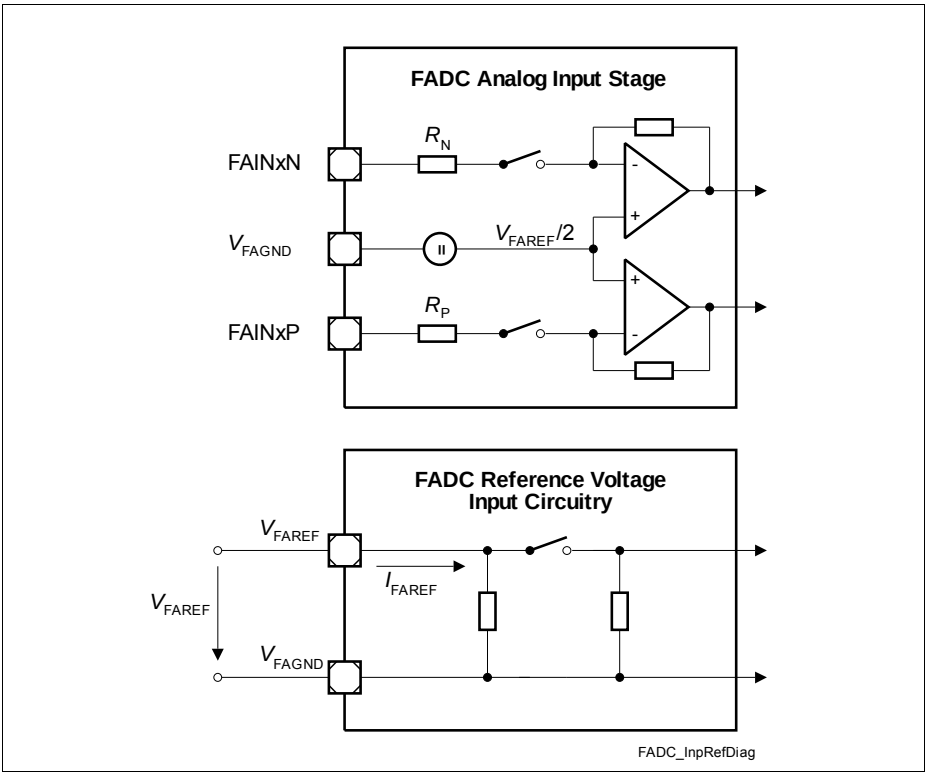


Figure 8 FADC Input Circuits

5.2.4 Oscillator Pins

Table 26 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-25	–	25	µA	$V_{IN}<V_{DDOSC3}$; $V_{IN}>0$ V
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		8	–	25	MHz	External Crystal Mode selected
Oscillator start-up time[1]	t_{OSCS} CC	–	–	10	ms	
Input high voltage at XTAL1[2]	V_{IHX} SR	0.7 x V_{DDOSC3}	–	V_{DDOSC3} + 0.5	V	
Input low voltage at XTAL1	V_{ILX} SR	-0.5	–	0.3 x V_{DDOSC3}	V	
Input Hysteresis for XTAL1 pad [3]	$HYSAX$ CC	–	–	200	mV	

1) t_{OSCS} is defined from the moment when V_{DDOSC3} = 3.13V until the oscillations reach an amplitude at XTAL1 of 0.3 * V_{DDOSC3}. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystral suppliers.

2) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of 0.4 * V_{DDOSC3} is necessary.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

5.2.5 Temperature Sensor

Table 27 DTS Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	100	µs	
Temperature sensor range	T_{SR} SR	-40	–	150	°C	
Sensor Accuracy (calibrated)	T_{TSA} CC	-6	–	6	°C	
Start-up time after resets inactive	t_{TSST} SR	–	–	20	µs	

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

(1)

$$Tj = \frac{DTSSTAT_{RESULT} - 596}{2,03}$$

5.2.6 Power Supply Current

The total power supply current defined below consists of leakage and switching component.

Application relevant values are typically lower than those given in the following two tables and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

The operating conditions for the parameters in the following table are:
VDD / V_{DDOSC} / V_{DDAF} / V_{DDPF}=1.365 V, VDDP / V_{DDOSC} / V_{DDMF} / V_{DDFL3} / V_{DDPF}=3.47 V, fSRI / CPU=300 MHz, fPCP=200 MHz, fSRI=100 MHz, TJ=150 oC

The realisic power pattern defines the following conditions:

- TJ=150 oC
- f_{SRI} = f_{CPU} = 300 MHz
- f_{PCP} = 200 MHz
- f_{FPI} = 100 MHz
- V_{DD} = V_{DDOSC} = V_{DDAF} = V_{DDPF} = 1.326 V
- V_{DDP} = V_{DDOSC3} = V_{DDFL3} V_{DDPF3} = V_{DDMF} = 3.366 V
- V_{DDM} = 5.1 V

The max power pattern defines the following conditions:

- TJ=150 oC
- f_{SRI} = f_{CPU} = 300 MHz
- f_{PCP} = 200 MHz
- f_{FPI} = 100 MHz
- V_{DD} = V_{DDOSC} = V_{DDAF} = V_{DDPF} = 1.43 V
- V_{DDP} = V_{DDOSC3} = V_{DDFL3} V_{DDPF3} = V_{DDMF} = 3.63 V
- V_{DDM} = 5.5 V

Table 28 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Core active mode supply current[1)2)]	I_{DD} CC	–	–	890[3)]	mA	power pattern= max; fCPU=300 MHz
		–	–	656[4)]	mA	power pattern= realistic; fCPU=300 MHz
I_{DD} current at PORST Low	I_{DD_PORST} CC	–	–	298	mA	TJ=150 oC
		–	–	249	mA	TJ=140 oC

Table 28 Power Supply Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
E-Ray PLL core supply current	I_{DDPF} CC	–	–	4	mA	
Oscillator core supply current	I_{DDOSC} CC	–	–	3	mA	
FADC core supply current	I_{DDAF} CC	–	–	26	mA	
Sum of all 1.3 V supply currents	I_{DDSUM} CC	–	–	689	mA	power pattern= realistic; fCPU=300 MHz
E-Ray PLL 3.3V supply	I_{DDPF3} CC	–	–	4	mA	
Oscillator power supply current, 3.3V	I_{DDOSC3} CC	–	–	11	mA	
FADC analog supply current, 3.3V	I_{DDMF} CC	–	–	15	mA	
I_{DDEBU} current at PORST Low	I_{DDEBU_PORST} CC	–	–	1	mA	
I_{DDP} current at PORST Low	I_{DDP_PORST} CC	–	–	7	mA	
I_{DDP} current no pad activity, LVDS off [5]	I_{DDP} CC	–	–	I_{DDP_PORST} + 25	mA	including flash read current
		–	–	I_{DDP_PORST} + 55	mA	including flash programming current [6]
		–	–	I_{DDP_PORST} + 40 [7]	mA	including flash erase verify current [6]

Table 28 Power Supply Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Flash memory current [5]	I_{DDFL3} CC	–	–	98	mA	flash read current
		–	–	29	mA	flash programming current [6]
		–	–	98	mA	flash erase current [6]
Current Consumption of LVDS Pad Pairs	I_{LVDS} CC	–	–	24	mA	in total for all LVDS pairs
Sum of all 3.3 V supply currents, no pad activity, LVDS off	I_{DD3SUM} CC	–	–	161 [8]	mA	including flash read current
ADC 5V power supply current	I_{DDM} CC	–	–	8	mA	
Maximum power dissipation	PD CC	–	–	1808	mW	power pattern= max; fCPU=300 MHz
		–	–	1547	mW	power pattern= realistic; fCPU=300 MHz

1) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each customer application will most probably be lower than this value, but must be evaluated seperately.

2) This current includes the E-Ray module power consumption, including the PCP operation component.

3) The I_{DD} decreases typically by 89mA if the f_{CPU} decreases by 50MHz, at constant T_J

4) The I_{DD} decreases typically by 70mA if the f_{CPU} decreases by 50MHz, at constant T_J

5) For operations including the D-Flash the required currents are always lower than the currents for non D-Flash operation.

6) Relevant for the power supply dimensioning, not for thermal considerations.

7) In case of erase of Program Flash PFx, internal flash array loading effects may generate transient current spikes of up to 15 mA for maximum 5 ms per flash module.

8) For power supply dimensioning of V_{DDP} 30 mA have to added for flash programming case.

5.2.6.1 Calculating the 1.3 V Current Consumption

The current consumption of the 1.3 V rail compose out of two parts:

- Static current consumption

- Dynamic current consumption

The static current consumption is related to the device temperature T_J and the dynamic current consumption depends of the configured clocking frequencies and the software application executed. These two parts needs to be added in order to get the rail current consumption.

(2)

$$I_0 = 3,75\left[\frac{mA}{C}\right] \times e^{0,02041 \times T_J[C]}$$

(3)

$$I_0 = 18,77\left[\frac{mA}{C}\right] \times e^{0,01825 \times T_J[C]}$$

Function 2 defines the typical static current consumption and Function 3 defines the maximum static current consumption. Both functions are valid for V_{DD} = 1.326 V.

For the dynamic current consumption using the application pattern and f_{SRI} = 2 * f_{PCP} = 3 * f_{FPI} the function 4 applies:

(4)

$$I_{Dym} = 1,19\left[\frac{mA}{MHz}\right] \times f_{CPU}[MHz]$$

and this finally results in

(5)

$$I_{DD} = I_0 + I_{DYM}$$

5.3 AC Parameters

That means, keeping the pads constantly at maximum strength.

5.3.1 Testing Waveforms

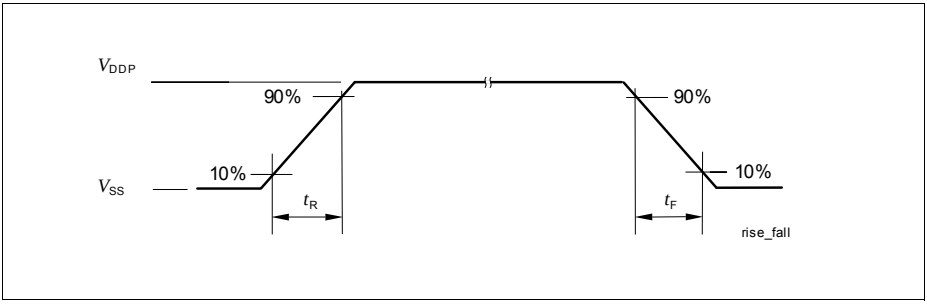


Figure 9 Rise/Fall Time Parameters

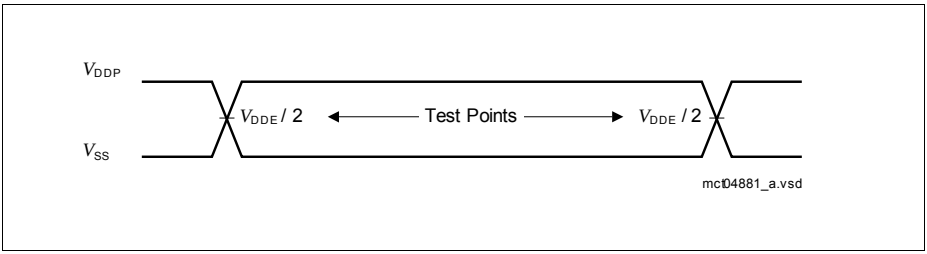


Figure 10 Testing Waveform, Output Delay

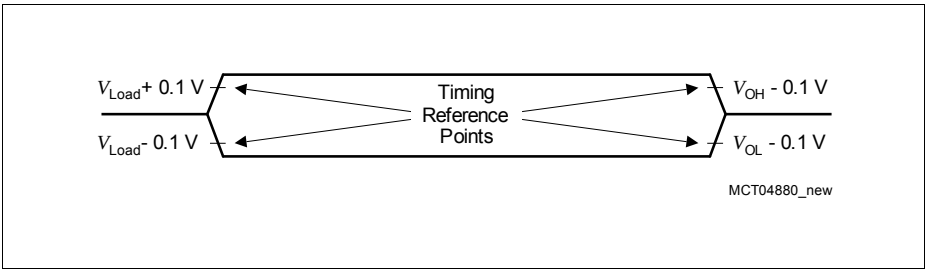


Figure 11 Testing Waveform, Output High Impedance

5.3.2 Power Sequencing

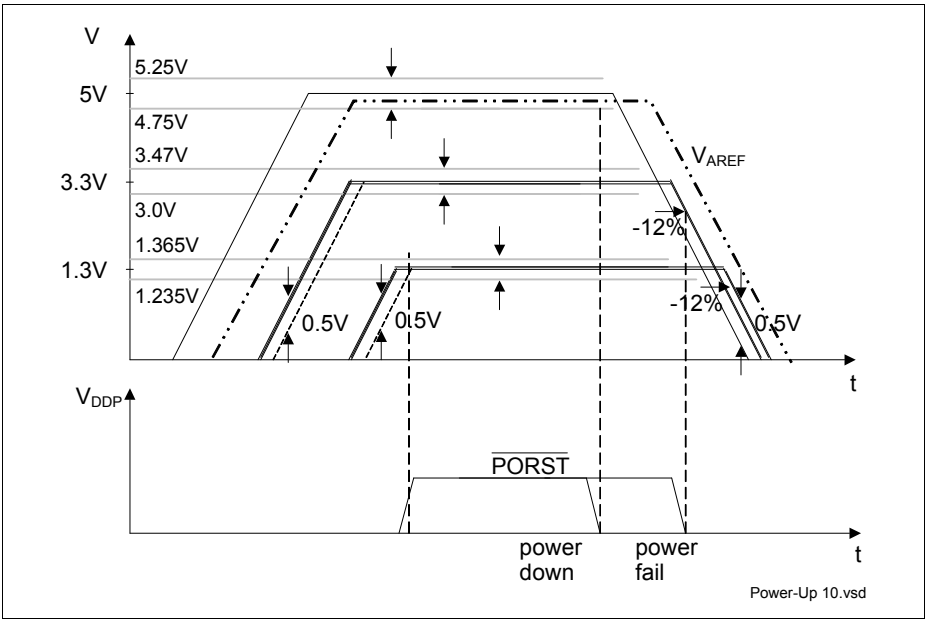


Figure 12 5 V / 3.3 V / 1.3 V Power-Up/Down Sequence

The following list of rules applies to the power-up/down sequence:

- All ground pins V_{SS} must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- At any moment in time to avoid increased latch-up risk,
  each power supply must be higher then any lower_power_supply - 0.5 V, or:
  VDD5 > VDD3.3 - 0.5 V; VDD5 > VDD1.3 - 0.5 V;VDD3.3 > VDD1.3 - 0.5 V, see **Figure 12**.
  – The latch-up risk is minimized if the I/O currents are limited to:
  – 20 mA for one pin group
  – AND 100 mA for the completed device I/Os
  – AND additionally before power-up / after power-down:
  1 mA for one pin in inactive mode (0 V on all power supplies)
- During power-up and power-down, the voltage difference between the power supply pins of the same voltage (3.3 V, 1.3 V, and 5 V) with different names (for example VDDP, VDDFL3 ...), that are internally connected via diodes, must be lower than

100 mV. On the other hand, all power supply pins with the same name (for example all VDDP), are internally directly connected. It is recommended that the power pins of the same voltage are driven by a single power supply.

- The PORST signal may be deactivated after all VDD5, VDD3.3, VDD1.3, and VAREF power-supplies and the oscillator have reached stable operation, within the normal operating conditions.
- At normal power down the PORST signal should be activated within the normal operating range, and then the power supplies may be switched off. Care must be taken that all Flash write or delete sequences have been completed.
- At power fail the PORST signal must be activated at latest when any 3.3 V or 1.3 V power supply voltage falls 12% below the nominal level. If, under these conditions, the PORST is activated during a Flash write, only the memory row that was the target of the write at the moment of the power loss will contain unreliable content. In order to ensure clean power-down behavior, the PORST signal should be activated as close as possible to the normal operating voltage range.
- In case of a power-loss at any power-supply, all power supplies must be powered-down, conforming at the same time to the rules number 2 and 4.
- Although not necessary, it is additionally recommended that all power supplies are powered-up/down together in a controlled way, as tight to each other as possible.
- Additionally, regarding the ADC reference voltage VAREF:
  – VAREF must power-up at the same time or later then VDDM, and
  – VAREF must power-down either earlier or at latest to satisfy the condition VAREF < VDDM + 0.5 V. This is required in order to prevent discharge of VAREF filter capacitance through the ESD diodes through the VDDM power supply. In case of discharging the reference capacitance through the ESD diodes, the current must be lower than 5 mA.

5.3.3 Power, Pad and Reset Timing

Table 29 Reset Timings Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time[1)2)]	t_B CC	–	–	880	µs	f_{CPU} = 300 MHz
Power on Reset Boot Time[3)4)]	t_{BP} CC	–	–	2.5	ms	
HWCFG pins hold time from ESR0 rising edge	t_{HDH} SR	16 / f_{FPI}	–	–	ns	
HWCFG pins setup time to ESR0 rising edge	t_{HDS} SR	0	–	–	ns	
Ports inactive after ESR0 reset active	t_{PI} CC	–	–	8/f_{FPI}	ns	
Ports inactive after PORST reset active[5)]	t_{PIP} CC	–	–	150	ns	
Minimum PORST active time after power supplies are stable at operating levels	t_{POA} SR	10	–	–	ms	
$\overline{\text{TESTMODE}}$ / $\overline{\text{TRST}}$ hold time from PORST rising edge	t_{POH} SR	100	–	–	ns	
PORST rise time	t_{POR} SR	–	–	50	ms	
$\overline{\text{TESTMODE}}$ / $\overline{\text{TRST}}$ setup time to PORST rising edge	t_{POS} SR	0	–	–	ns	
Application Reset inactive after PORST deassertion	t_{POR_APP} SR	–	–	40 [6)]	µs	

1) The duration of the boot time is defined between the rising edge of the internal application reset and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

2) The given time includes the time of the internal reset extension for a configured value of SCU_RSTCNTCON.RELSA = 0x05BE.

3) The duration of the boot time is defined between the rising edge of the $\overline{\text{PORST}}$ and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

4) The given time includes the internal reset extension time for the System and Application Reset which is visible through ESR0.
5) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.
6) Application Reset is assumed not to be extended from external, otherwise the time extends by the time the Application Reset is extended.

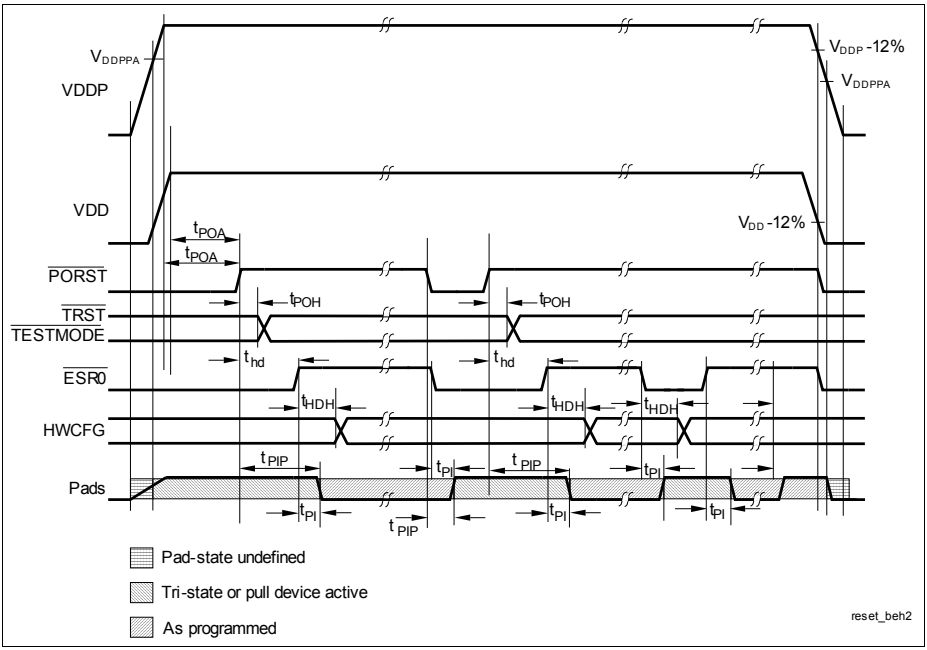


Figure 13 Power, Pad and Reset Timing

5.3.4 Phase Locked Loop (PLL)

Table 30 PLL_SysClk Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	-7	–	7	ns	
Modulation frequency	f_{MOD} SR	50	–	200	kHz	
PLL base frequency	$f_{PLLBASE}$ CC	50	200	320	MHz	
VCO input frequency	f_{REF} CC	8	–	16	MHz	
VCO frequency range	f_{VCO} CC	400	–	720	MHz	with inactive modulation
		400	–	600	MHz	with active modulation
Modulation jitter	J_{MOD} CC	–	–	2.5	ns	
Total long term jitter	J_{TOT} CC	–	–	9.5	ns	
Modulation Amplitude	MA SR	0	–	2.5	%	
PLL lock-in time	t_L CC	14	–	200	µs	N > 32
		14	–	400	µs	N ≤ 32
System frequency deviation	f_{SYSD} CC	–	–	0.01	%	with active modulation

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the SRI-Bus clock f_{SRI}) is constantly adjusted to the selected frequency. The PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or clock source), resulting in an accumulated jitter that is limited. This means that the relative deviation for periods of more than one clock cycle is lower than for a single clock cycle.

This is especially important for bus cycles using wait states and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

Two formulas are defined for the (absolute) approximate maximum value of jitter D_m in [ns] dependent on the K2 - factor, the SRI clock frequency f_{SRI} in [MHz], and the number m of consecutive f_{SRI} clock periods.

$$\text{for} \quad (K2 \leq 100) \quad \text{and} \quad (m \leq (f_{SRI}[MHz])/2)$$

$$|Dm[ns]| = \left(\frac{740}{K2 \times f_{SRI}[MHz]} + 5\right) \times \left(\frac{(1 - 0,01 \times K2) \times (m - 1)}{0,5 \times f_{SRI}[MHz] - 1} + 0,01 \times K2\right) \quad (6)$$

$$\text{else} \quad |Dm[ns]| = \frac{740}{K2 \times f_{SRI}[MHz]} + 5 \quad (7)$$

With rising number m of clock cycles the maximum jitter increases linearly up to a value of m that is defined by the K2-factor of the PLL. Beyond this value of m the maximum accumulated jitter remains at a constant value. Further, a lower SRI-Bus clock frequency f_{SRI} results in a higher absolute maximum jitter value.

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDOSC3} and V_{SSOSC}, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.

The maximum peak-to peak noise on the pad supply voltage, measured between V_{DDOSC} and V_{SSOSC}, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.

These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

Oscillator Watchdog (OSC_WDT)

The expected input frequency is selected via the bit field SCU_OSCCON.OSCVAL. The OSC_WDT checks for too low frequencies and for too high frequencies.

The frequency that is monitored is f_{OSCREF} which is derived for f_{OSC}.

$$f_{OSCREF} = \frac{f_{OSC}}{OSCVAL + 1} \quad (8)$$

The divider value SCU_OSCCON.OSCVAL has to be selected in a way that f_{OSCREF} is 2.5 MHz.

Note: f_{OSCREF} has to be within the range of 2 MHz to 3 MHz and should be as close as possible to 2.5 MHz.

The monitored frequency is too low if it is below 1.25 MHz and too high if it is above 7.5 MHz. This leads to the following two conditions:

- Too low: f_{OSC} < 1.25 MHz × (SCU_OSCCON.OSCVAL+1)
- Too high: f_{OSC} > 7.5 MHz × (SCU_OSCCON.OSCVAL+1)

Note: The accuracy is 30% for these boundaries.

Frequency Modulation

Frequency modulation defines a slow and predictable variation of the clock speed. The modulation configuration itself is controlled via register SCU_PLLCON2 where the two bit fields define the modulation properties.

(9)

$$f_{MOD} = \frac{f_{OSC}}{P} \times \frac{MODFREQ \times 31,32}{MODAMP}$$

(10)

$$MA = \frac{MODAMP}{N \times 161}$$

5.3.5 ERAY Phase Locked Loop (ERAY_PLL)

Table 31 PLL_ERAY Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated jitter at SYSCLK pin	D_{PP} CC	-0.8	–	0.8	ns	
Accumulated_Jitter	D_P CC	-0.5	–	0.5	ns	
PLL Base Frequency of the ERAY PLL	$f_{PLLBASE\_ERAY}$ CC	50	250	360	MHz	
VCO input frequency of the ERAY PLL	f_{REF} CC	20	–	40	MHz	
VCO frequency range of the ERAY PLL	f_{VCO_ERAY} CC	450	–	500	MHz	
PLL lock-in time	t_L CC	5.6	–	200	µs	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDPF3} and V_{SSPF}, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.
These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

5.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 32 JTAG Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t1 SR	25	–	–	ns	–
TCK high time	t2 SR	10	–	–	ns	–
TCK low time	t_3 SR	10	–	–	ns	–
TCK clock rise time	t_4 SR	–	–	4	ns	–
TCK clock fall time	t_5 SR	–	–	4	ns	–
TDI/TMS setup to TCK rising edge	t6 SR	6	–	–	ns	–
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	–
TDO valid after TCK falling edge[1] (propagation delay)	t_8 CC	–	–	13	ns	C_L = 50 pF
	t_8 CC	3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18} CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9 CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10} CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

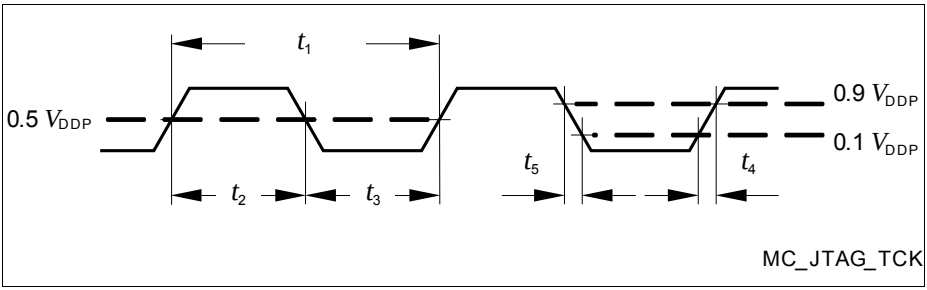


Figure 14 Test Clock Timing (TCK)

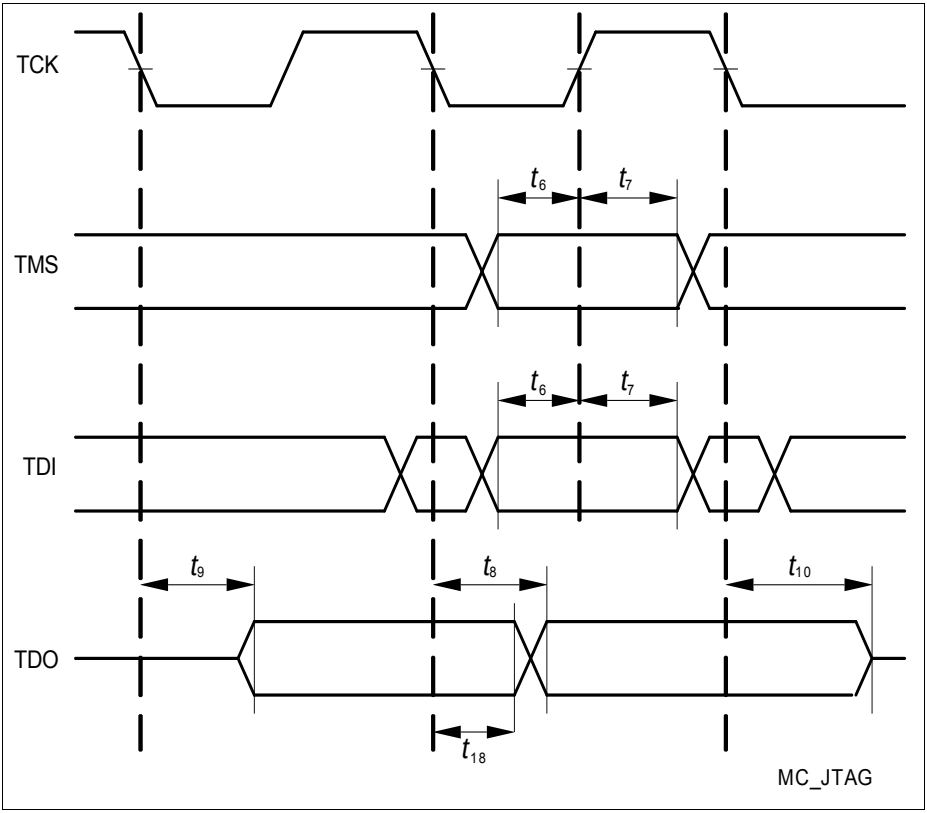


Figure 15 JTAG Timing

5.3.7 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 33 DAP Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period[1]	t_{TCK} SR	12.5	–	–	ns	
DAP0 high time	t_{12} SR	4	–	–	ns	
DAP0 low time[1]	t_{13} SR	4	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	2	ns	
DAP0 clock fall time	t_{15} SR	–	–	2	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6.0	–	–	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	6.0	–	–	ns	
DAP1 valid per DAP0 clock period[2]	t_{19} CC	8	–	–	ns	C_L= 20 pF; f= 80 MHz
		10	–	–	ns	C_L= 50 pF; f= 40 MHz

1) See the DAP chapter for clock rate restrictions in the Active:IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

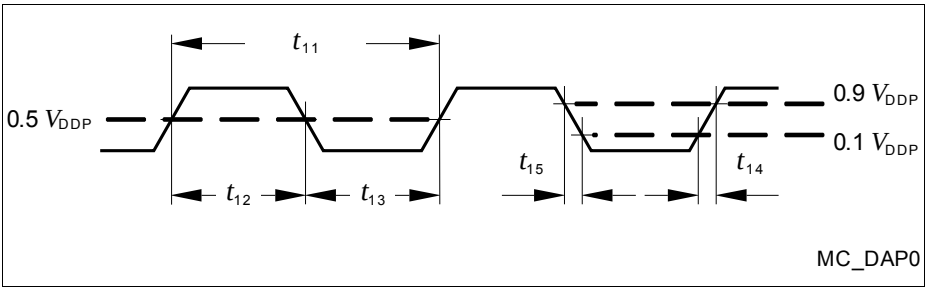


Figure 16 Test Clock Timing (DAP0)

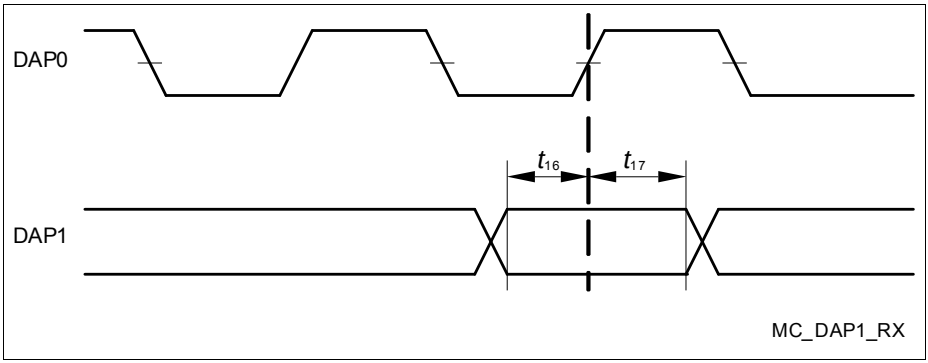


Figure 17 DAP Timing Host to Device

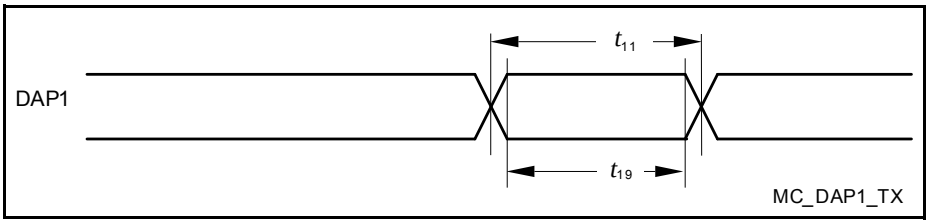


Figure 18 DAP Timing Device to Host

5.3.8 Micro Link Interface (MLI) Timing

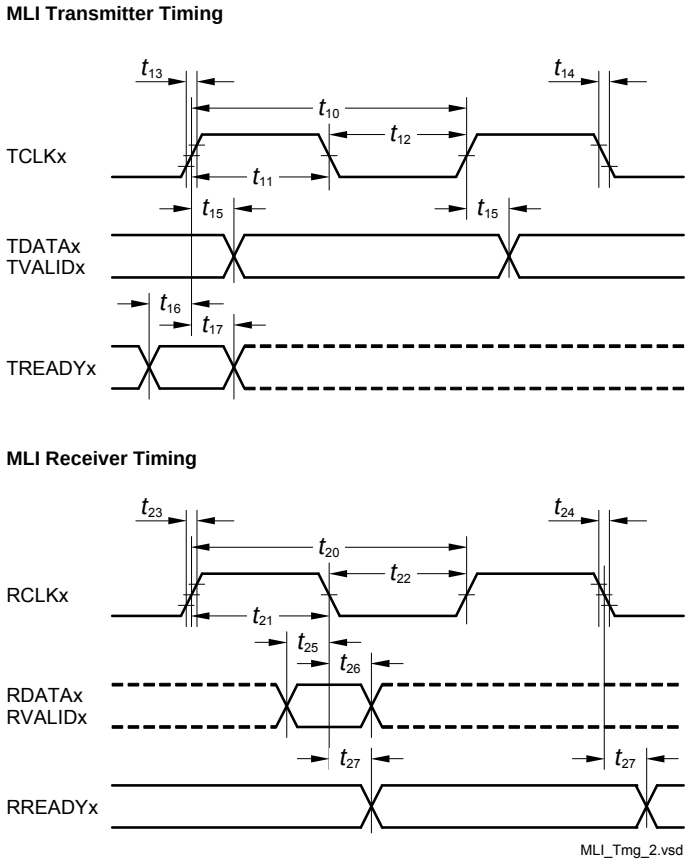


Figure 19 MLI Interface Timing

Note: The generation of RREADYx is in the input clock domain of the receiver. The reception of TREADYx is asynchronous to TCLKx.

The MLI parameters are vaild for C_L = 50 pF and strong driver medium edge.

Table 34 MLI Receiver

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RCLK clock period	t_{20} SR	1 / f_{FPI}	–	–	ns	
RCLK high time[1)2)]	t_{21} SR	–	0.5 x t_{20}	–	ns	
RCLK low time[1)2)]	t_{22} SR	–	0.5 x t_{20}	–	ns	
RCLK rise time[3)]	t_{23} SR	–	–	4	ns	
RCLK fall time[3)]	t_{24} SR	–	–	4	ns	
RDATA/RVALID setup time before RCLK falling edge	t_{25} SR	4.2	–	–	ns	
RDATA/RVALID hold time after RCLK falling edge	t_{26} SR	2.2	–	–	ns	
RREADY output delay time	t_{27} SR	0	–	16	ns	

1) The following formula is valid: t21 + t22 = t20.

2) Min and Max values for this parameter can be derived from the typ. value by considering the other receiver timing parameters.

3) The RCLK max. input rise/fall times are best case parameters for fSYS = 90 MHz. For reduction of EMI, slower input signal rise/fall times can be used for longer RCLK clock periods.

Table 35 MLI Transmitter

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCLK clock period	t_{10} CC	2 x 1 / f_{FPI}	–	–	ns	
TCLK high time[1)2)]	t_{11} CC	0.45 x t_{10}	0.5 x t_{10}	0.55 x t_{10}	ns	
TCLK low time[1)2)]	t_{12} CC	0.45 x t_{10}	0.5 x t_{10}	0.55 x t_{10}	ns	
TCLK rise time	t_{13} CC	–	–	0.3 x t_{10}[3)]	ns	
TCLK fall time	t_{14} CC	–	–	0.3 x t_{10}[3)]	ns	

Table 35 MLI Transmitter (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TDATA/TVALID output delay time	t_{15} CC	-3	–	4.4	ns	
TREADY setup time before TCLK rising edge	t_{16} SR	18	–	–	ns	
TREADY hold time after TCLK rising edge	t_{17} SR	-2	–	–	ns	

1) The following formula is valid: t11 + t12 = t10.

2) The min./max. TCLK low/high times t11/t12 include the PLL jitter of fSYS. Fractional divider settings must be regarded additionally to t11 / t12.

3) For high-speed MLI interface, strong driver sharp or medium edge selection (class A2 pad) is recommended for TCLK.

5.3.9 Micro Second Channel (MSC) Interface Timing

The MSC parameters are vaild for C_L = 50 pF.

Table 36 MSC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLP clock period[1)2)]	t_{40} CC	2 x T_{MSC}[3)]	–	–	ns	
SOP[4)]/ENx outputs delay from FCLP[4)] rising edge	t_{45} CC	-2	–	5	ns	ENx with strong driver and sharp (minus) edge
		-2	–	10	ns	ENx with strong driver and medium (minus) edge
		0	–	21	ns	ENx with strong driver and soft edge
SDI bit time	t_{46} CC	8 x T_{MSC}	–	–	ns	

Table 36 MSC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDI rise time	t_{48} SR	–	–	200	ns	
SDI fall time	t_{49} SR	–	–	200	ns	

1) FCLP signal rise/fall times are only defined by the pad rise/fall times.
2) FCLP signal high and low can be minimum $1xT_{MSC}$
3) TMSC = TSYS = 1 / fSYS.
4) SOP / FCLP either propagated by LVDS or by CMOS strong driver and non soft edge.

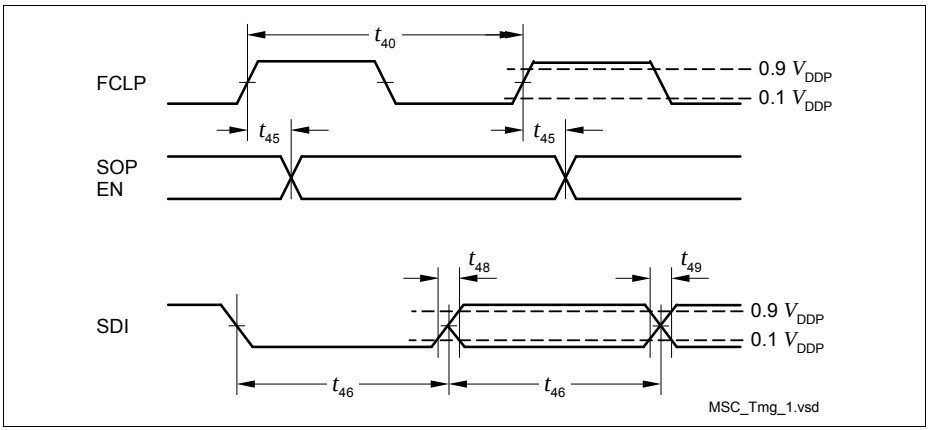


Figure 20 MSC Interface Timing

Note: The data at SOP should be sampled with the falling edge of FCLP in the target device.

5.3.10 SSC Master/Slave Mode Timing

The SSC parameters are vaild for C_L = 50 pF and strong driver medium edge.

Table 37 SSC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period[1)2)3)]	t_{50} CC	2 x 1 / f_{FPI}	–	–	ns	
MTSR/SLSOx delay form SCLK rising edge	t_{51} CC	0	–	8	ns	
MRST setup to SCLK latching edge[3)]	t_{52} SR	16.5	–	–	ns	
MRST hold from SCLK latching edge[3)]	t_{53} SR	0	–	–	ns	
SCLK input clock period[1)3)]	t_{54} SR	4 x 1 / f_{FPI}	–	–	ns	
SCLK input clock duty cycle	t_{55}_t_{54} SR	45	–	55	%	
MTSR setup to SCLK latching edge[3)4)]	t_{56} SR	1 / f_{FPI}	–	–	ns	
MTSR hold from SCLK latching edge	t_{57} SR	1 / f_{FPI} + 5	–	–	ns	
SLSI setup to first SCLK latching edge	t_{58} SR	1 / f_{FPI} + 5	–	–	ns	
SLSI hold from last SCLK latching edge[5)]	t_{59} SR	7	–	–	ns	
MRST delay from SCLK shift edge	t_{60} CC	0	–	16.5	ns	
SLSI to valid data on MRST	t_{61} CC	–	–	16.5	ns	

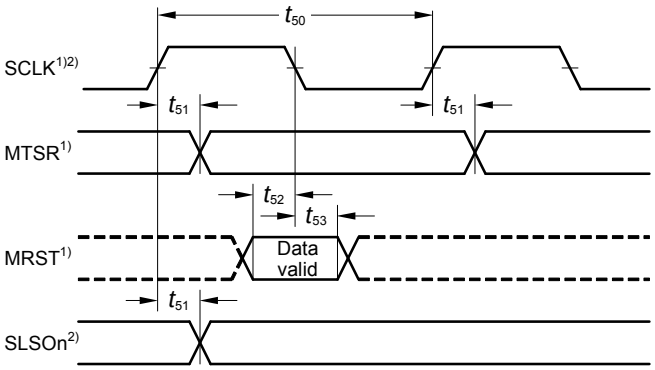
1) SCLK signal rise/fall times are the same as the rise/fall times of the pad.

2) SCLK signal high and low times can be minimum 1xTSSC.

3) TSSCmin = TSYS = 1/fSYS.

4) Fractional divider switched off, SSC internal baud rate generation used.

5) For CON.PH=1 slave select must not be removed before the following shifting edge. This mean, that what ever is configured (shifting / latching first), SLSI must not be de-actived before the last trailing edge from the pair of shifting / latching edges.



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

2) The transition at SLSOn is based on the following setup: SSOTC.TRAIL = 0 and the first SCLK high pulse is in the first one of a transmission.

SSC_TmgMM

Figure 21 SSC Master Mode Timing

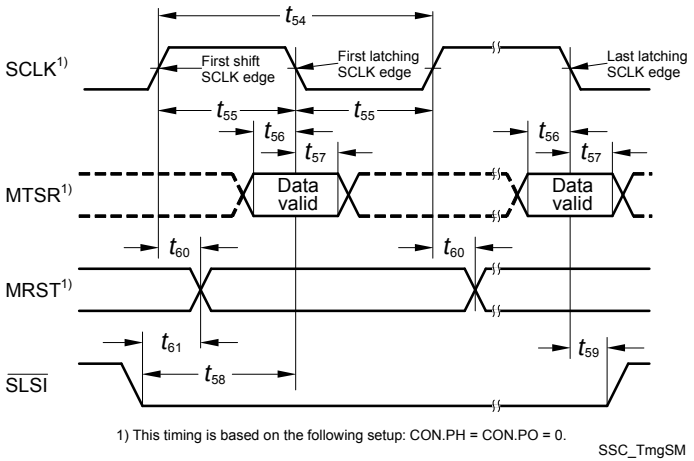


Figure 22 SSC Slave Mode Timing

5.3.11 ERAY Interface Timing

The timings of this section are valid for the strong driver and either sharp edge or medium edge settings of the output drivers with C_L = 25 pF.

The ERAY interface is only available for the SAK-TC1798F-512F300EP / SAK-TC1798F-512F300EL / SAK-TC1798S-512F300EP.

Table 38 ERAY Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Time span from last BSS to FES without the influence of quartz tolerancies (d10Bit_TX)[1]	t_{60} CC	997.75	–	1002.25	ns	
TxD data valid from fsample flip flop txd_reg TxDA, TxDB (dTxAsym)[2][3]	t_{61}-t_{62} CC	–	–	1.5	ns	Asymmetrical delay of rising and falling edge (TxDA, TxDB)
Time span between last BSS and FES without influence of quartz tolerancies (d10Bit_RX)[1][4][5]	t_{63} SR	966	–	1046.1	ns	
RxD capture by fsample (RxDA/RxDB sampling flip-flop) (dRxAsym)[6]	t_{64}-t_{65} CC	–	–	3.0	ns	Asymmetrical delay of rising and falling edge (RxDA, RxDB)
TxD data delay from sampling flip-flop	*dTxdly* CC	–	–	10.0	ns	Px_PDR.PDy = 000_B
		–	–	15.0	ns	Px_PDR.PDy = 001_B
RxD capture delay by sampling flip-flop	*dRxdly* CC	–	–	10.0	ns	

1) This includes the PLL_ERAY accumulated jitter.

2) Refers to delays caused by the asymmetries of the output drivers of the digital logic and the GPIO pad drivers. Quarz tolerance and PLL_ERAY accumulated jitter are not included.

3) E-Ray TxD output drivers have an asymmetry of rising and falling edges of $|t_{FA2} - t_{RA2}| \leq 1$ ns.

4) Limits of 966ns and 1046.1ns correspond to (30%, 70%) * V_{DDP} FlexRay standard input thresholds. For input thresholds of this product, a correction of - 0.5 ns and +0.1 ns has to be applied.

5) Valid for output slopes of the bus driver of dRxSlope ≤ 5ns, 20% * V_{DDP} to 80% * V_{DDP}, according to the FlexRay Electrical Physical Layer Specification V2.1B. For A2 pads, the rise and fall times of the incoming signal have to satisfy the following inequality: -1.6ns ≤ t_{FA2} - t_{RA2} ≤ 1.3ns.

6) Valid for output slopes of the bus driver of dRxSlope ≤ 5ns, 20% * V_{DDP} to 80% * V_{DDP}, according to the FlexRay Electrical Physical Layer Specification V2.1B. For A2 pads, the rise and fall times of the incoming signal have to satisfy the following inequality: -1.6ns ≤ t_{FA2} - t_{RA2} ≤ 1.3ns.

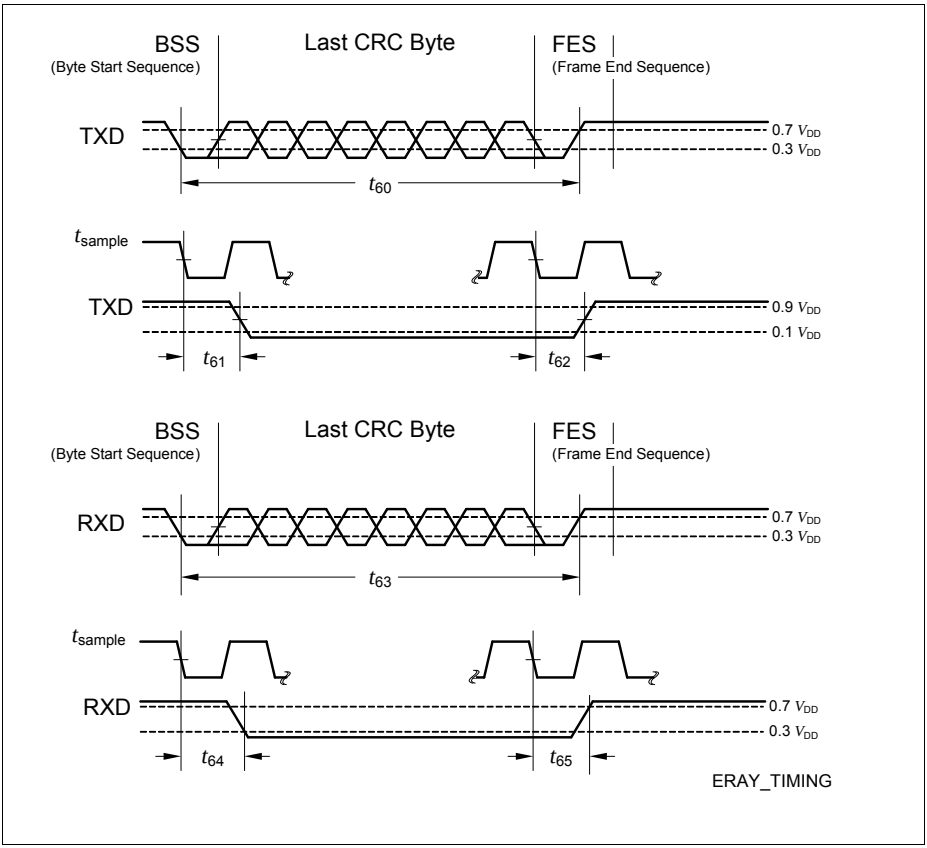


Figure 23 ERAY Timing

5.3.12 EBU Timings

5.3.12.1 BFCLKO Output Clock Timing

V_{SS} = 0 V;V_{DD} = 1.3 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%,;
C_L = 35 pF

Table 39 BFCLK0 Output Clock Timing Parameters[1)]

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
BFCLKO clock period	t_{BFCLKO}	CC	13.33[2)]	–	–	ns	–
BFCLKO high time	t_5	CC	3	–	–	ns	–
BFCLKO low time	t_6	CC	3	–	–	ns	–
BFCLKO rise time	t_7	CC	–	–	3	ns	–
BFCLKO fall time	t_8	CC	–	–	3	ns	–
BFCLKO duty cycle $t_5/(t_5 + t_6)$[3)]	DC		35	50	55	%	–

1) Not subject to production test, verified by design/characterization.

2) The PLL jitter characteristics add to this value according to the application settings. See the PLL jitter parameters.

3) The PLL jitter is not included in this parameter. If the BFCLKO frequency is equal to f_{CPU}, the K divider has to be regarded.

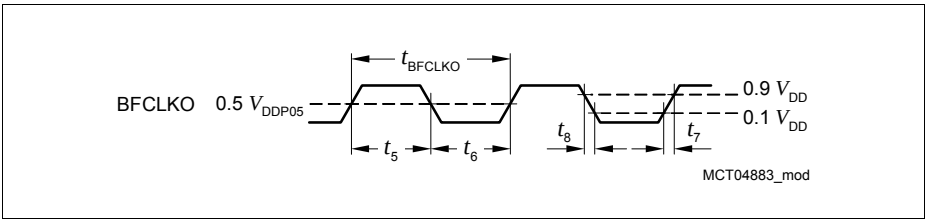


Figure 24 BFCLKO Output Clock Timing

5.3.12.2 EBU Asynchronous Timings

V_{SS} = 0 V;V_{DD} = 1.3 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
C_L = 35 pF for address/data; C_L = 40pF for the control lines.

For each timing, the accumulated PLL jitter of the programed duration in number of clock periods must be added separately. Operating conditions apply and C_L = 35 pF.

Table 40 EBU Common Asynchronous Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pulse wdih deviation from the ideal programmed width due to B pad asymmetry, rise delay - fall delay[1)]	t_a CC	-0.8	–	0.8	ns	edge= medium
		-0.8	–	0.8	ns	edge= sharp
AD(31:0) output delay to ADV# rising edge, multiplexed read / write[1)]	t_{13} CC	-5.5	–	2	ns	
AD(31:0) output delay to ADV# rising edge, multiplexed read / write[1)]	t_{14} CC	-5.5	–	2	ns	
Address valid to CS falling edge (deviation from programmed value)[1)]	t_{15} CC	-2	–	2	ns	
Address valid to ADV falling edge (deviation from programmed value)[1)]	t_{16} CC	-2	–	2	ns	
ADV falling edge -> CSfalling edge (deviation from programmed value)[1)]	t_{17} CC	-2	–	2	ns	

1) Not subject to production test, verified by design/characterization.

Table 41 EBU Asynchronous Read Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
A(23:0) output delay to $\overline{RD}$ rising edge, deviation from the ideal programmed value[1)]	t_0 CC	-2.5	–	2.5	ns	
A(23:0) output delay to RD rising edge, deviation from the ideal programmed value[1)]	t_1 CC	-2.5	–	2.5	ns	
CS rising edge to RD rising edge, deviation from the ideal programmed value[1)]	t_2 CC	-2	–	2.5	ns	
ADV rising edge to RD rising edge, deviation from the ideal programmed value[1)]	t_3 CC	-1.5	–	4.5	ns	
BC rising edge to RD rising edge, deviation from the ideal programmed value[1)]	t_4 CC	-2.5	–	2.5	ns	
WAIT input setup to RD rising edge, deviation from the ideal programmed value[1)]	t_5 SR	12	–	–	ns	
WAIT input hold to RD rising edge, deviation from the ideal programmed value[1)]	t_6 SR	0	–	–	ns	
Data input setup to RD rising edge, deviation from the ideal programmed value[1)]	t_7 SR	12	–	–	ns	

Table 41 EBU Asynchronous Read Timings (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data input hold to RD rising edge, deviation from the ideal programmed value[1)]	t_8 SR	-2	–	–	ns	
MR / W output delay to RD# rising edge, deviation from the ideal programmed value[1)]	t_9 CC	-2.5	–	1.5	ns	
Data input hold from CS rising edge[1)]	t_{18} CC	-2	–	–	ns	
Data input setup to CS rising edge[1)]	t_{19} CC	12	–	–	ns	

1) Not subject to production test, verified by design/characterization.

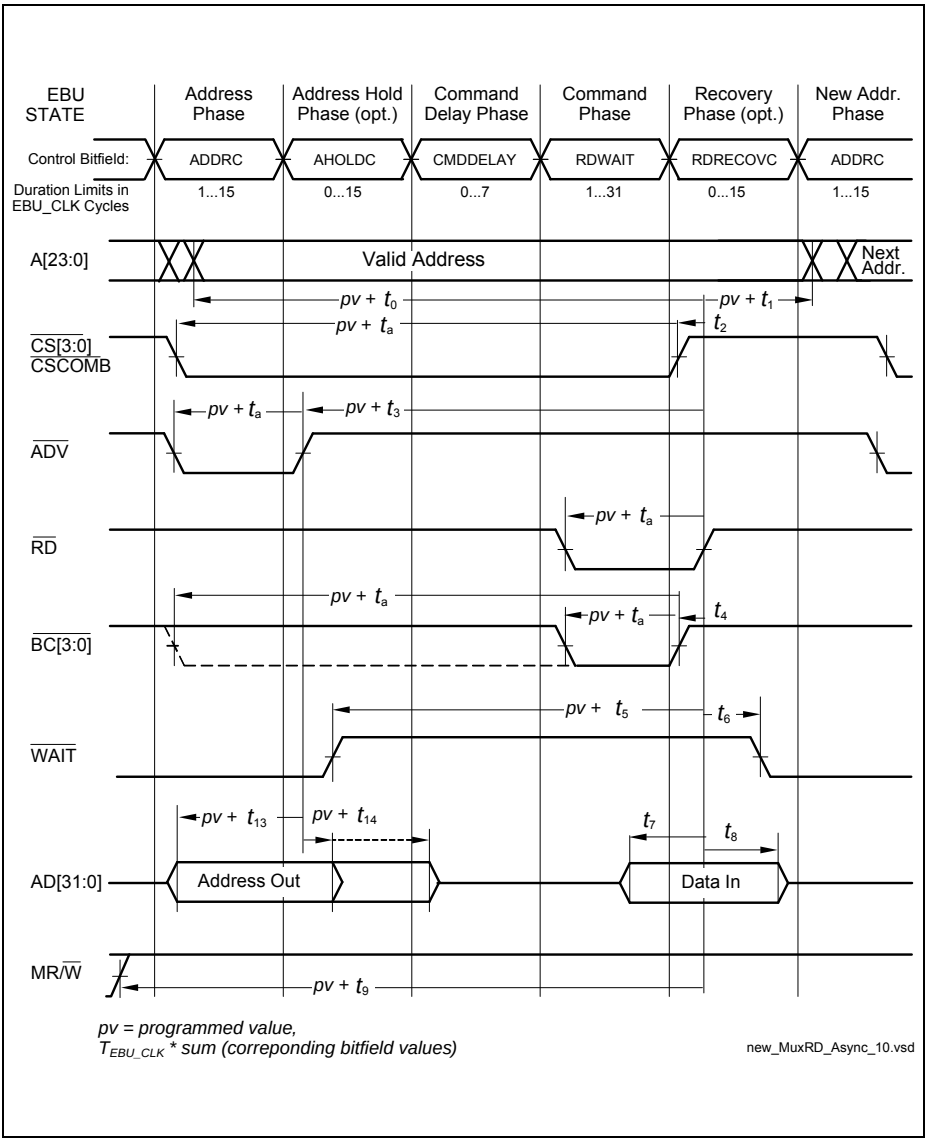


Figure 25 Multiplexed Read Access

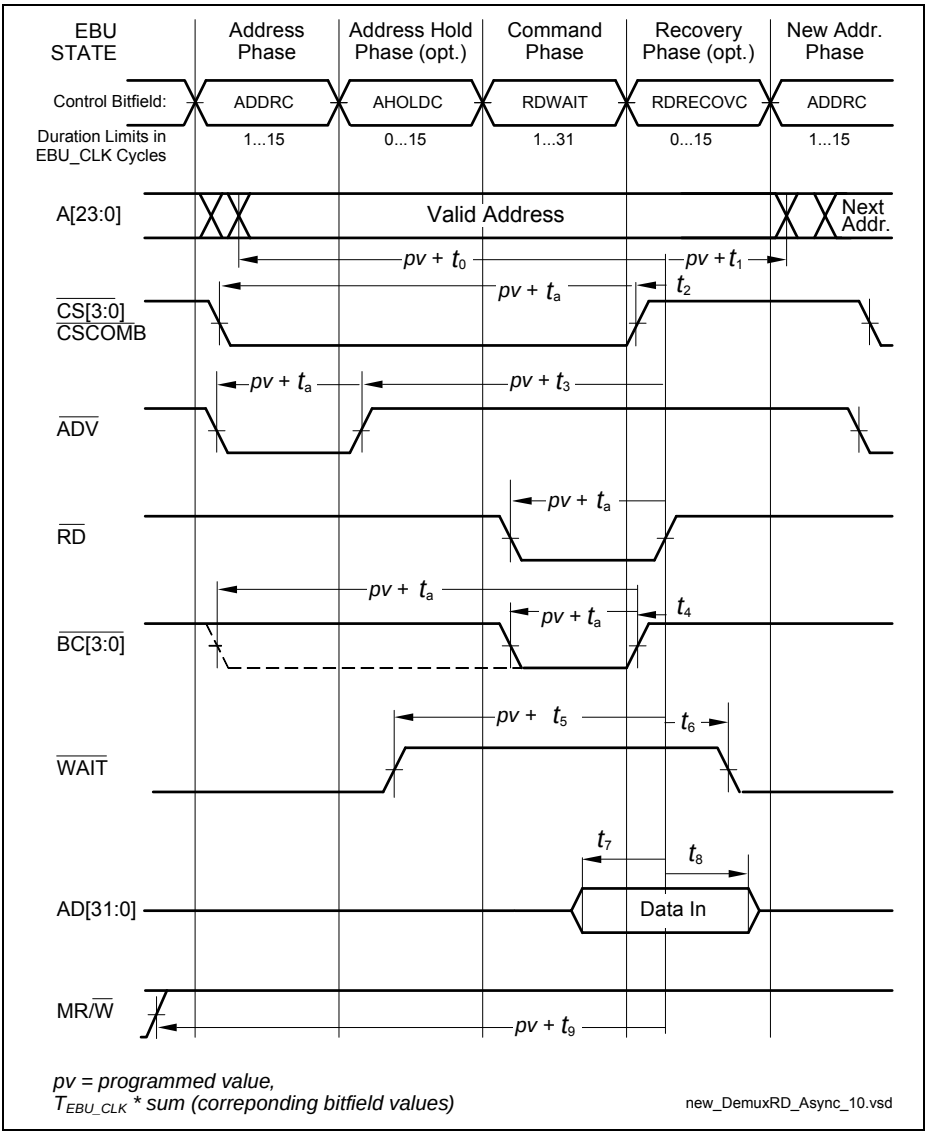


Figure 26 Demultiplexed Read Access

Table 42 EBU Asynchnronous Write Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
A(23:0) output delay to WR rising edge, deviation from the ideal programmed value[1)]	t_{30} CC	-2.5	–	2.5	ns	
A(23:0) output delay to WR rising edge, deviation from the ideal programmed value[1)]	t_{31} CC	-2.5	–	2.5	ns	
CS rising edge to WR rising edge, deviation from the ideal programmed value[1)]	t_{32} CC	-2	–	2	ns	
ADV rising edge to WR rising edge, deviation from the ideal programmed value[1)]	t_{33} CC	-2.5	–	2	ns	
BC rising edge to WR rising edge, deviation from the ideal programmed value[1)]	t_{34} CC	-2.5	–	2	ns	
WAIT input setup to WR rising edge, deviation from the ideal programmed value[1)]	t_{35} SR	12	–	–	ns	
WAIT input hold to WR rising edge, deviation from the ideal programmed value[1)]	t_{36} SR	0	–	–	ns	
Data output delay to WR falling edge, deviation from the ideal programmed value[1)]	t_{37} CC	-5.5	–	2	ns	

Table 42 EBU Asynchnronous Write Timings (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data output delay to WR rising edge, deviation from the ideal programmed value[1)]	t_{38} CC	-5.5	–	2	ns	
MR / W output delay to WR rising edge, deviation from the ideal programmed value[1)]	t_{39} CC	-2.5	–	1.5	ns	

1) Not subject to production test, verified by design/characterization.

5.3.12.3 EBU Burst Mode Access Timing

V_{SS} = 0 V;V_{DD} = 1.3 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
C_L = 35 pF;

Table 43 EBU Burst Read Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output delay from BFCLKO rising edge[1)]	t_{10} CC	-2	–	2	ns	
RD and RD/WR active/inactive after BFCLKO active edge[1)2)]	t_{12} CC	-2	–	2	ns	
CSx output delay from BFCLKO active edge[1)2)]	t_{21} CC	-2.5	–	1.5	ns	
ADV active/inactive after BFCLKO active edge[1)3)]	t_{22} CC	-2	–	2	ns	
BAA active/inactive after BFCLKO active edge[1)3)]	t_{22a} CC	-2.5	–	1.5	ns	
Data setup to BFCLKI rising edge[1)]	t_{23} SR	3	–	–	ns	
Data hold from BFCLKI rising edge[1)]	t_{24} SR	0	–	–	ns	

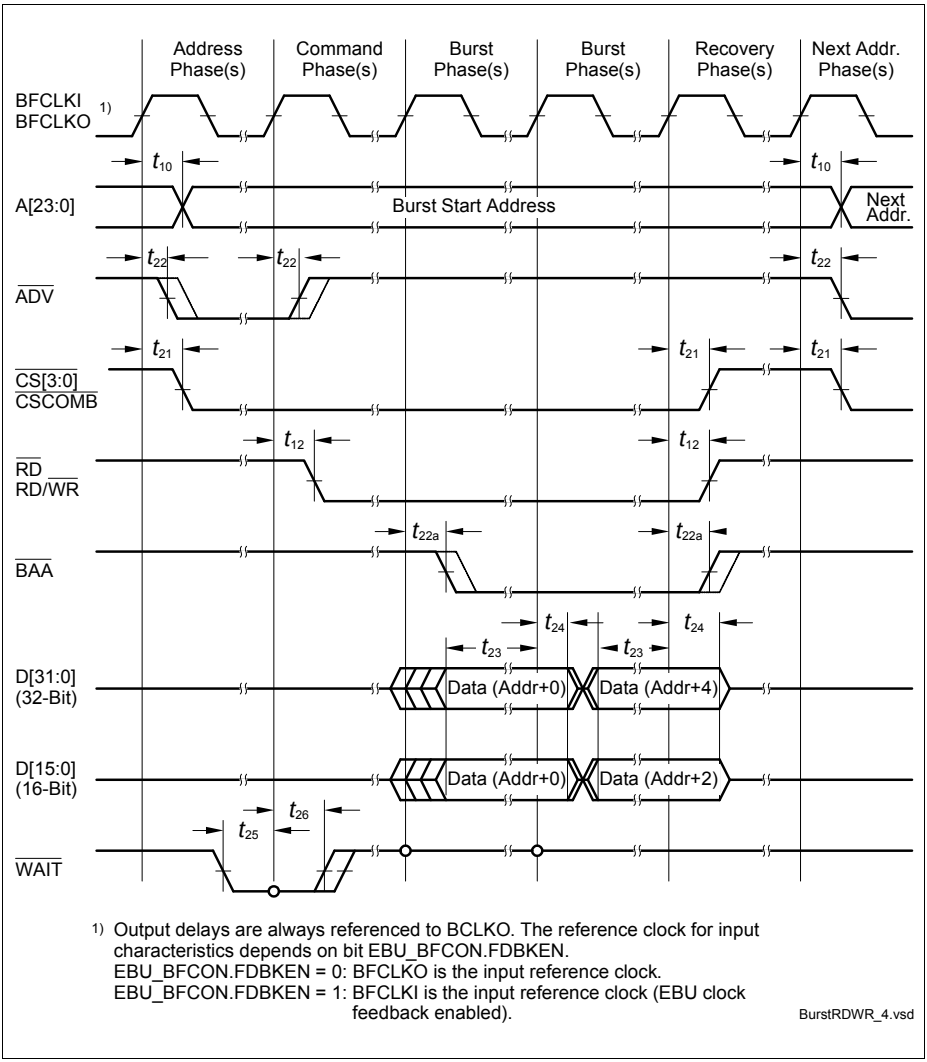
Table 43 EBU Burst Read Timings (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
WAIT setup (low or high) to BFCLKI rising edge [1]	t_{25} SR	3	–	–	ns	
WAIT hold (low or high) from BFCLKI rising edge[1]	t_{26} SR	0	–	–	ns	

1) Not subject to production test, verified by design/characterization.

2) An active edge can be rising or falling edge, depending on the settings of bits BFCON.EBSE / ECSE and clock divider ratio. Negative minimum values for these parameters mean that the last data read during a burst may be corrupted. However, with clock feedback enabled, this value is oversampling not required for the LMB transaction and will be discarded. If the clock feedback is not enabled, the input signals are latched using the internal clock in the same way as at asynchronous access. So t14, t15, t16, t17, t18 and t19 from the asynchronous timings apply.

3) For BUSCONx.EBSE=1B and BUSAPx.EXLCLK=00B, ADV will change normally on the clock edge so this parameter is used directly.
For BUSCONx.EBSE=1B and other values of BUSAPx.EXTCLK, ADV and BAA add the high pulse width of EBUCLK to this parameter.
For BUSCONx.EBSE=0B and BUSAPx.EXTCLK=00B add the high pulse width of EBUCLK to this parameter.
For BUSCONx.EBSE=0B and BUSAPx.EXTCLK=11B add two EBUCLK periodsto this parameter to get the hold time from BFCLKO rising edge to the ADV.
For BUSCONx.EBSE=0B and BUSAPx.EXTCLK=01B or 10B add 1 EBUCLK period.
Please note that the high pulse width of EBUCLK is defined by the high pulse width of fVCO of the used PLL.



1) Output delays are always referenced to BCLKO. The reference clock for input characteristics depends on bit EBU_BFCON.FDBKEN.
EBU_BFCON.FDBKEN = 0: BFCLKO is the input reference clock.
EBU_BFCON.FDBKEN = 1: BFCLKI is the input reference clock (EBU clock feedback enabled).

BurstRDWR_4.vsd

Figure 27 EBU Burst Mode Read / Write Access Timing

5.3.12.4 EBU Arbitration Signal Timing

V_{SS} = 0 V;V_{DD} = 1.5 V ± 5%; V_{DDEBU} = 2.5 V ± 5% and 3.3 V ± 5%, Class B pins;
T_A = -40°C to +125 °C; C_L = 35 pF;

Table 44 EBU EBU Arbitration Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output delay from BFCLKO rising edge[1)]	t_{27} CC	–	–	3	ns	
Data setup to BFCLKO falling edge[1)]	t_{28} SR	8	–	–	ns	
Data hold from BFCLKO falling edge[1)]	t_{29} SR	2	–	–	ns	

1) Not subject to production test, verified by design/characterization.

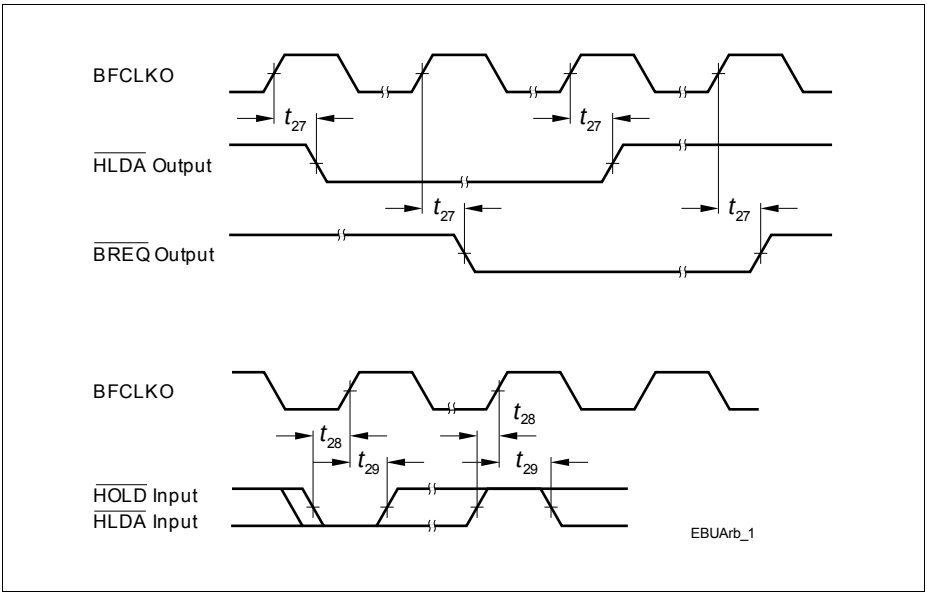


Figure 28 EBU Arbitration Signal Timing

5.3.12.5 EBU DDR Timing Parameters

Parameters applicable when using the EBU to access DDR memories

Table 45 is valid under the following conditions: $C_L \leq$ 20 pF; V_{DDEBU}= 1.8 ±5% V

Table 45 EBU DDR Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DDR Clock Signal fall time	t_{CF} CC	–	–	3.3	ns	
DDR Clock Signal high time	t_{CH} CC	29	–	71	%	
DDR Clock Signal period[1)]	t_{CK} CC	24.0	–	–	ns	
Skew between clock rising transition and DQS rising edge or clock falling transition and DQS falling edge[2)]	t_{CKDQS} CC	-1.2	–	1.2	ns	
DDR Clock Signal low time	t_{CL} CC	47	–	53	%	
DDR Clock Signal rise time	t_{CR} CC	–	–	3.3	ns	
Maximum time from falling clock edge until DDR Control signal is valid[3)]	t_{CVA} CC	–	–	5	ns	
Maximum time before falling clock edge that DDR control signal can become invalid[3)]	t_{CVB} CC	–	–	5	ns	
DLL Delay time for duty cycle correction when locked	t_{DCC} CC	t_{EBU} / 2 - 0.3	–	t_{EBU} / 2 + 0.3	ns	
byte lane x signals valid value hold time (DQ & DM) after DQSx edge[4)]	t_{DH1} CC	-1.6[5)]	–	–	ns	
DLL Delay time for for DQ and DM when locked with DLLCON.WR_ADJ=0d	t_{DLL} CC	t_{EBU} / 4 - 0.2	–	t_{EBU} / 4 + 0.2	ns	

Table 45 EBU DDR Timings (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DLL Delay time for DQS when locked with DLLCON.RD_ADJ=0d	t_{DLLR} CC	t_{EBU} / 4 - 0.15	–	t_{EBU} / 4 + 0.15	ns	
DQ and DQS all signals hold time after DDRCLK0 edge, DDRCLK0 controlled read	t_{DQCKH} CC	1.0	–	–	ns	
DQ and DQS all signal valid to DDRCLK0 edge, DDRCLK0 controlled read	t_{DQCKS} CC	1.2	–	–	ns	
DQSx edge to byte lane x signals valid (DQ & DM)[4)]	t_{DS1} CC	–	–	1.0	ns	
Maximum Peak to Peak jitter of the DDR clock output	t_{PKPK} CC	–	–	0	ns	
DQ byte lane hold time after DQSx edge, minimum hold time to guarantee read data capture, DLL Controlled read	t_{QH} SR	1.0	–	–	ns	
DQ byte lane valid to DQSx edge minimum setup time to guarantee read data capture, DLL Controlled read[6)4)]	t_{QS} SR	1.0	–	–	ns	

1) This is a configuration constraint and not a design limit. Application code must not configure the EBU to generate a DDR clock with a period of less than 12ns.

2) To allow for the differential clock trigger point being different from the trigger point on each of the individual signals, this parameter will be characterised separately for each of the clock signals OCLKO, DDRCLKO and DDRCLKO with a limit of ±1 ns

3) To allow for the differential clock trigger point being different from the trigger point on each of the individual signals, this parameter will be characterised separately for each of the clock signals DDRCLKO (SDCLKO) and DDRCLKO with a limit of ±2.4 ns

4) x = 0 to 3

5) i.e. signal can become invalid at most tDH1 before the clock edge

6) falling or rising edge

Timing for EBU DDR Clock Outputs

The EBU provides three possible DDR clock outputs depending on the type of device being accessed. These are

- Differential clock for accessing devices using a DDRAM type protocol on the DDRCLKO and $\overline{\text{DDRCLKO}}$ pins.
- Differential clock for accessing devices using a burst flash type protocol on the BFCLKO and $\overline{\text{DDRCLKO}}$ pins.
- A single-ended clock on OCLKO (MR/$\overline{\text{W}}$) for interfacing to ONFI 2 compliant devices.

All these clocks operate with identical timing parameters and have a restricted load limit of 10pF for DDR operation.

The rising edge on the differential clocks is defined as when a rising edge on DDRCLKO or BFCLKO transitions past a falling edge on $\overline{\text{DDRCLKO}}$.

Timings apply at VDD_{EBU} = 1.8 volts

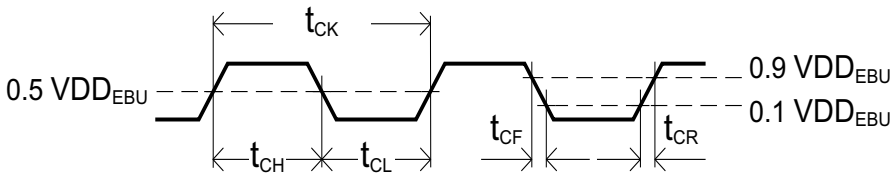


Figure 29 Timing Waveform for DDR Clock Signals

Timing for EBU DDR Control Outputs

The EBU control state machine will ensure that commands and signal transitions are generated in the correct clock cycle to meet device requirements. This section also applies when accessing SDRAM devices.

The EBU will generate address (A[15:0]) and control (CKE, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WR}}$) outputs on the falling edge of the DDR clock to allow nominally symmetric setup and hold margins around the rising edge of the clock. For SDRAM devices, the same address and control signals are required but, in addition, the write data (AD[31:0]) and DQM signals ($\overline{\text{BC}}$[3:0]) are required to meet the same timing requirements.

As these parameters apply to SDRAM as well as DDR devices, the load limit should be taken to be 40pF.

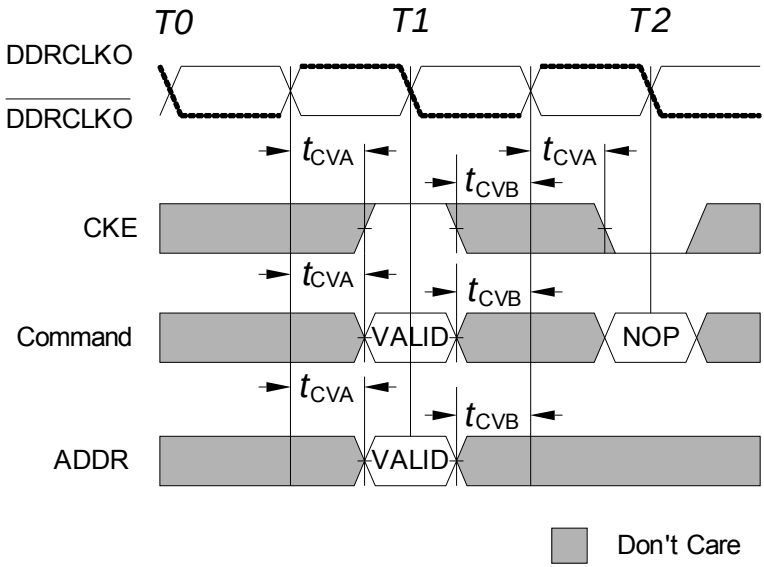


Figure 30 DDR command and Address Timing

Using the DDRNCON.AMODE field, the timing of the address can be changed so that the address changes on the rising clock edge and is held for two clock cycles. This allows a nominal setup and hold margin of a full clock cycle. This mode is not compatible with burst length of two as commands needing a valid address output can then be generated in consecutive clock cycles.

Timing of DDR Write Data

The EBU will generate the DQ (write data) DM and DQS signals in two different modes depending on the ratio of the internal to external clocks.

If the ratio is 1:1, then the clock used to generate the DQ and DM outputs must be shifted by the DLL by 25% of the external clock period (nominal value).

If the ratio is 1:2 or 1:4, then the DQ and DM signals will be generated using edges of the internal clock and the DLL must not be used to further adjust the edge timing.

A ratio of 1:3 is not supported.

In all cases, the edges of the DQS signals are nominally aligned to the clock output and the DQS waveform is in phase with, and the same frequency as, the memory device clock input.

The EBU is characterised with the DLL inactive, so the timing parameters are specified for this case. For the 1:1 operating mode, the DLL shift time and its error margin has to be added where appropriate. For the 1:2 or 1:4 cases, the signals will be generated by the appropriate clock edge so will be delayed by the correct number of EBU clock periods (t_{EBU}). In this case the clock jitter will need to be subtracted from the available setup and hold margins.

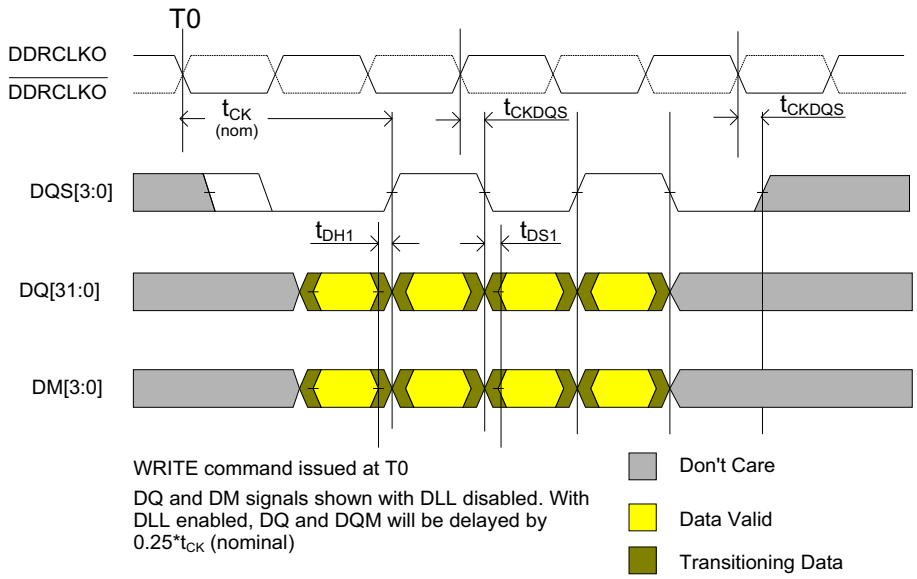


Figure 31 Signal Relationship for DDR writes

1:1 internal to external clock ratio

If the external bus clock is running at the same frequency as the internal clock, then the DLL is used to generate intermediate clock edges at the intervals necessary to correctly position the transitions on DQ and DM

Using the defined parameters. In the case where the DDR memory clock is the same frequency as the internal EBU clock and the DLL is enabled but the DLL's internal duty cycle correction is not in use:

- t_{DH} for the memory will be $t_{CK}/2+t_{DH1}$-tDLL
- t_{DS} for the memory will be $t_{CK}/2-t_{DS1}$-tDLL-t_{JIT}[1)]

If the duty cycle correction is in use (DLLCON.DCC_EN=1_B), then the equation for setup becomes:

1) t_{JIT} is the pk-pk clock jitter of the EBU internal clock

- t_{DS} for the memory will be $t_{CK}/2-t_{DS1}$-tDLL-$(2*t_{JIT})$
- t_{DH} for the memory will be $t_{CK}/2+t_{DH1}$-tDLL

1:2 internal to external clock ratio

If the external bus clock is running at half the internal clock frequency, then the negative phase clock is used to generate intermediate clock edges at the intervals necessary to correctly position the transitions on DQ and DM

The negative phase clock is generated either by:

- If the EBU internal clock is a pulse swallowed version of the system clock then the negative phase clock is generated by swallowing alternate pulses. So if the main clock is divide by 4 and generated by passing pulses 0..4..8.. etc, then the neagtive phase clock will be generated by passing pulses 2..6..10..
  - t_{DH} for the memory will be $t_{EBU}/2+t_{DH1}-(n^{1)}/2*t_{JIT}^{2)})$
  - t_{DS} for the memory will be $t_{EBU}/4-t_{DS1}-(n/2*t_{JIT})$
- If the EBU internal clock is a buffered version of the system clock input then the negative phase clock will be an inverted version of the system clock
  - t_{DH} for the memory will be $t_{CK}/4+t_{DH1}-t_{JIT2}^{3)}$
  - t_{DS} for the memory will be $t_{CK}/4-t_{DS1}-t_{JIT2}$
- If the duty cycle correction function of the DLL is enabled, then the negative phase clock will be the main clock delayed by $0.5*t_{CK}$
  - t_{DH} for the memory will be $t_{DCC}+t_{DH1}$
  - t_{DS} for the memory will be $t_{DCC}-t_{DS1}$

1:4 internal to external clock ratio

If the external bus clock is running at one quarter the internal clock frequency, then EBU internal clock clock is used to generate intermediate clock edges at the intervals necessary to correctly position the transitions on DQ and DM

The negative phase clock is generated either by:

- t_{DH} for the memory will be $t_{EBU}+t_{DH1}-t_{JIT}$
- t_{DS} for the memory will be $t_{EBU}-t_{DS1}-t_{JIT}$

Timing of DDR Read Data

DDR read data can be captured in two modes. The first mode uses the DLL to shift the DQS signals internally to provide setup and hold margins between the DQS and DQ lines. The DQS signals are then used as a clock to latch the data into internal registers.

The second mode is suitable only for lower frequencies and uses the $\overline{\text{DDRCLKO}}$ signal internally as a clock to latch both the DQ and DQS signals. The state of the latched DQS

1) where n is the divide ratio between the system clock input and the EBU internal clock

2) t_{JIT} is the pk-pk clock jitter of the system clock source

3) t_{JIT2} is the rising to falling edge jitter of the system clock source

signal is used to determine whether DQ is valid at any given clock edge. The restriction is that the DDRCLKO signal must propagate through the TC1798 output pad in both directions in time for the DQ and DQS signals to be latched before the next rising edge of DDRCLKO at the clock generating flip-flop inside the EBU, i.e.

(Pad Output Delay)+(Pad Input Delay)+(Latch CK->Q valid) = $t_{TIME} < t_{ck}$

In addition the clock to output valid delay of the attached memory device must be less than 0.5 * t_{CK}

DLL Controlled Read

The EBU interface is characterised with the DLL disabled. The relative positioning of the DQ and DQS edges are then adjusted to determine the setup and hold times. The parameters in the following table are therefore specified with the DLL inactive

A standard DDR device will output the DQ and DQS signals with edges that are nominally aligned and the DLL will delay the DQS inputs internally to re-establish the setup and hold margins.

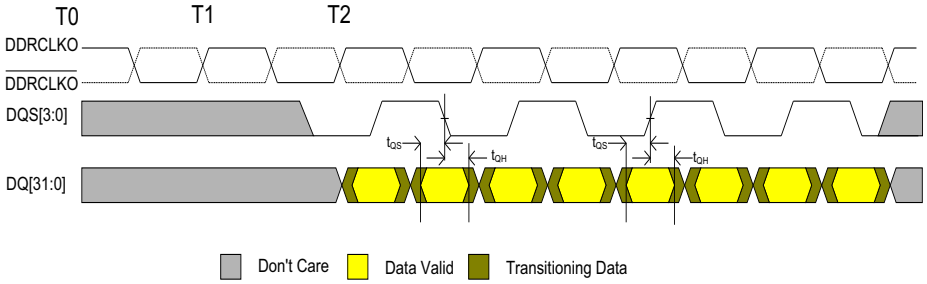


Figure 32 DLL Controlled Read

Once the DLL is enabled, to satisfy the setup time, the DQ output from the memory device must be valid less than t_{DLLR}-t_{QS} ns after the DQS edge.

To satisfy the hold time, the DQ output from the memory device must remain valid until the time (t_{CK}/2)-t_{JITn}-t_{DLLR}-t_{DH} before the next DQS edge.

DDRCLKO Controlled Read

A standard DDR device will output the DQ and DQS signals with edges that are nominally aligned. In this mode, the data will be latched on both edges of the feedback clock. This clock is generated from DDRCLKO.

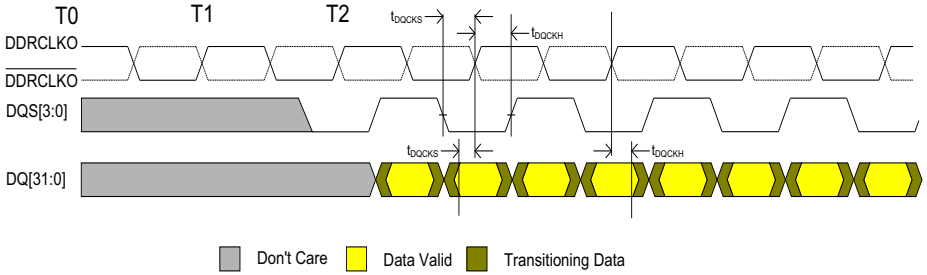


Figure 33 DDRCLKO Controlled Read

In order for the read data to be captured successfully, the maximum clock to DQS & DQ valid limit for the attached memory device must be less than half an external bus clock period by the setup margin, t_{DQCKS} and the hold time for the DQS and data after the clock edge must be greater than t_{DQCKH}.

Timing of SDRAM Read Data

For SDRAM read accesses, DDRCLKO (SDCLKO) must be connected to $\overline{\text{DDRCLKO}}$ (SDCLKI) to establish a path for the feedback clock. Then tDQCKS and tDQCKH can be used to calculate timing margins in the same ways as for a DDR read except that only the rising edge of SDCLKI is used for capturing data.

In order for the read data to be captured successfully, the maximum clock to DQ valid limit for the attached memory device must be less than an external bus clock period by the setup margin, t_{DQCKS} and the hold time for the data after the clock edge must be greater than t_{DQCKH}.

5.4 Flash Memory Parameters

The data retention time of the TC1798's Flash memory depends on the number of times the Flash memory has been erased and programmed.

Table 46 FLASH32 Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Sector	t_{ERD} CC	–	–	4.2[1)]	s	
Program Flash Erase Time per 256 KByte Sector	t_{ERP} CC	–	–	5	s	

Table 46 FLASH32 Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program time data flash per page[2]	t_{PRD} CC	–	–	5.3	ms	without reprogramming
		–	–	15.9	ms	with two reprogramming cycles
Program time program flash per page[3]	t_{PRP} CC	–	–	5.3	ms	without reprogramming
		–	–	10.6	ms	with one reprogramming cycle
Data Flash Endurance	N_E CC	60000 [4]	–	–	cycles	Min. data retention time 5 years
Erase suspend delay	t_{FL_ErSusp} CC	–	–	15	ms	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	10	–	–	µs	
Aborted logical sector erase soft-programming recovery	t_{FL_SPREC} CC	–	–	400	ms	
Program Flash Retention Time, Physical Sector[5][6]	t_{RET} CC	20	–	–	years	Max. 1000 erase/program cycles
Program Flash Retention Time, Logical Sector[5][6]	t_{RETL} CC	20	–	–	years	Max. 100 erase/program cycles
UCB Retention Time[5][6]	t_{RTU} CC	20	–	–	years	Max. 4 erase/program cycles per UCB
Wake-Up time	t_{WU} CC	–	–	270	µs	
DFlash wait state configuration	WS_{DF} CC	$50\,ns \times f_{FSI}$	–	–		
PFlash wait state configuration	WS_{PF} CC	$26\,ns \times f_{FSI}$	–	–		

1) In case of wordline oriented defects (see robust EEPROM emulation in the User's Manual) this erase time can increase by up to 100%.
2) In case the Program Verify feature detects weak bits, these bits will be programmed up to twice more. Each reprogramming takes additional 5 ms.
3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5 ms.
4) Only valid when a robust EEPROM emulation algorithm is used. For more details see the User´s Manual.
5) Storage and inactive time included.
6) At average weighted junction temperature T_j = 100°C, or the retention time at average weighted temperature of T_j = 110°C is minimum 10 years, or the retention time at average weighted temperature of T_j = 150°C is minimum 0.7 years.

5.5 Package and Reliability

5.5.1 Package Parameters

Table 47 Thermal Characteristics of the Package

Device	Package	RΘJCT 1)	RΘJCB 1)	RΘJA	Unit	Note
TC1798	PG-LFBGA- 516	3,5	6,1	14,7	K/W	

1) The top and bottom thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) are to be combined with the thermal resistances between the junction and the case given above (R_{TJCT}, R_{TJCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.
Thermal resistances as measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1).

5.5.2 Package Outline

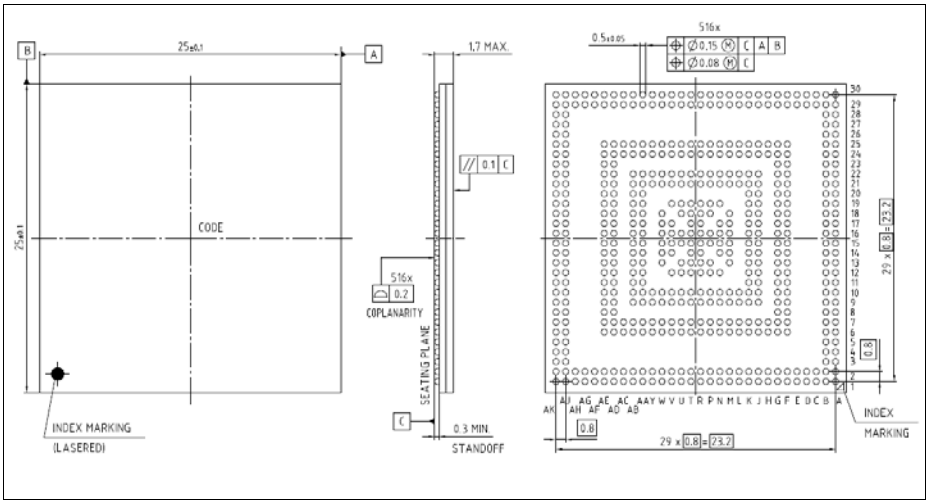


Figure 34 Package Outlines PG-LFBGA- 516

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

5.5.3 Quality Declarations

Table 48 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation Lifetime[1)]	t_{OP}	–	–	24000	hours	–[2)]
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	–	–	2000	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins	V_{HBM1}	–	–	500	V	–

Table 48 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM}	–	–	500	V	Conforming to JESD22-C101-C
Moisture Sensitivity Level	MSL	–	–	3	–	Conforming to Jedec J-STD-020C for 240°C

1) This lifetime refers only to the time when the device is powered on.

2) For worst-case temperature profile equivalent to:
1200 hours at T_j = 125...150°C
3600 hours at T_j = 110...125°C
7200 hours at T_j = 100...110°C
11000 hours at T_j = 25...110°C
1000 hours at T_j = -40...25°C

6 History

The following changes where done between Version 0.6 and 0.62 of this document:

- change wdith for port 2 in figure 2
- change numbers of V_{DDFL3} and V_{SS} in figure 2
- update figure 3 according to pinning changes
- remove typo in Ctrl. line from I/O0 to I/O
- change for port 2.8 the symbol from CTRAPB (CCU60) to CCPOS0A (CCU62)
- change for port 2.8 the symbol from T13HRE (CCU61) to T12HRB (CCU63)
- add for port 2.8 the symbol from T3INB (GPT120)
- add for port 2.8 the symbol from T3INA (GPT121)
- change for port 2.10 the symbol from CC60INC (CCU61) to CTRAPB (CCU63)
- change for port 2.12 the symbol from CTRAPB (CCU61) to CCPOS0A (CCU63)
- change for port 2.12 the symbol from T13HRE (CCU60) to T12HRB (CCU62)
- add for port 2.12 the symbol from T2INB (GPT120)
- add for port 2.12 the symbol from T2INA (GPT121)
- add for port 3.0 the symbol CTRAPB (CCU61)
- change for port 3.0 for symbol CC60INC from CCU62 to CCU61
- move pin P3.1 from B20 to B22
- move pin P3.2 from J19 to A22
- move pin P3.3 from A20 to B21
- move pin P3.4 from G19 to K18
- move pin P3.5 from B19 to A21
- move pin P3.6 from K18 to B19
- move pin P3.7 from A19 to A20
- move pin P3.8 from J18 to B19
- move pin P3.9 from B18 to A19
- move pin P3.10 from G18 to J18
- move pin P3.11 from A18 to B18
- move pin P3.12 from F18 to K17
- move pin P3.13 from B13 to A18
- move pin P3.14 from K17 to B13
- removed for port 3.2 the symbol CTRAPB (CCU62)
- add for port 3.4 the symbol CTRAPA (CCU63)
- change for port 3.4 the symbol from CC61INC (CCU62) to CTRAPB (CCU60)
-
- removed for port 3.6 the symbol CTRAPB (CCU63)
- change for port 3.8 the symbol from T12HRB (CCU63) to T13HRE (CCU61)
- removed for port 3.8 the symbol CCPOS0A (CCU62)
- removed for port 3.8 the symbol T3INB (GPT120)
- removed for port 3.8 the symbol T3INA (GPT121)
- change for port 3.14 the symbol from T12HRB (CCU62) to T13HRE (CCU60)
- removed for port 3.14 the symbol CCPOS0A (CCU63)

- removed for port 3.14 the symbol T2INB (GPT120)
- removed for port 3.14 the symbol T2INA (GPT121)
- change function description for port 4.1 alternate output 3 MTSR2 from Slave to Master Mode
- add footnote to port 4.1 alternate output 3 MTSR2
- change function description for port 4.1 alternate output 3 MTSR2 from Slave to Master Transmit
- move pin P5.12 from B22 to J19
- move pin P5.12 from B23 to G19
- move pin P5.12 from A22 to G18
- move pin P5.12 from A23 to F18
- add footnote to port 6.4 alternate output 1 MTSR1
- change for port 7.0 the symbol from ADEMUX0 to ADEMUX2
- change function description for port 7.1 alternate output 2 MTSR3 from Slave to Master Mode
- add footnote to port 7.1 alternate output 2 MTSR3
- change for port 8.3 the symbol from OUT43 (GPTA1) to CC62 (CCU60)
- add for port 8.5 the symbol CTRAPB (CCU62)
- change for port 9.13 the symbol from ECTT2 to ECTT1
- change for port 9.14 the symbol from ECTT1 to ECTT2
- add for port 9.14 the symbol REQ15
- add footnote to port 10.1 alternate output 1 MTSR0
- change for port 15 the type from S to D / S
- change function description for port 18.1 alternate input MTSR2B from Master to Slave Mode
- change function description for port 18.1 alternate output 1 MTSR2 from Slave to Master Mode
- add footnote to port 18.1 alternate output 1 MTSR2
- move pin V_{DDP} from AD15 to AD16
- add clarification that table 9 defines the conditions for all other parameters
- add conditions for MLI, MSC, SSC, parameters
- add parameters dTxdly and dRxdly to ERAY parameters
- correct footnotes for ERAY parameters
- split flash parameters tPRD and tPRP in two conditions
- add conditions to LVDS pad parameters
- remove Pin Reliability in Overload section
- add parameters IIN and Sum IIN to absolute ratings
- add parameter HYSX to PSC_XTAL
- added RDSON values for all driver settings (weak, medium, and strong)
- removed footnote 2 of table 10
- change load for timing of SSC, MSC, and MLI from C_L = 25 pF to C_L = 50 pF (typical)
- add to parameters t_{RF} and t_{FF} condition C_L = 50 pF
- add new footnote 7) to ADC parameter table

- add min and max value for Q_{CONV} and adapt typ value
- add load conditions for t_{FF1} and t_{RF1}
- add conditions to PLL parameter t_L
- change DAP parameter t_{19} from SR to CC classification
- remove footnote 2 for the FADC
- adapt IDs for AB step
- move pin AN49 from W2 to W1
- move pin AN48 from W1 to W2
- removed footnote 2 in table 9
- change max value for ADC parameter t_S from 255 to 257
-
- change P1.7 input CC60INB to CC61INB
- remove O2 OUT105 for GPTA1 of P14.9
- add O2 T3OUt for GPT121 of P14.9
- changed the name for O3 from EVTO2 to EVTO1 for P0.5
- changed the name for O3 from EVTO3 to EVTO2 for P0.6
- changed the name for O3 from EVTO4 to EVTO3 for P0.7
- changed the name for O1 and O2 from OUT70 to OUT71 for P1.15
- add input function $\overline{\text{SLSI2}}$ for SSC2 to P4.9

The following changes where done between Version 0.62 and 0.63 of this document:

- change P1.7 input CC60INB to CC61INB
- remove O2 OUT105 for GPTA1 of P14.9
- add O2 T3OUt for GPT121 of P14.9
- changed the name for O3 from EVTO2 to EVTO1 for P0.5
- changed the name for O3 from EVTO3 to EVTO2 for P0.6
- changed the name for O3 from EVTO4 to EVTO3 for P0.7
- changed the name for O1 and O2 from OUT70 to OUT71 for P1.15
- add input function $\overline{\text{SLSI2}}$ for SSC2 to P4.9
- add input function CC60INC forCCU61 for P2.10
- change back for port 3.0 for symbol CC60INC from CCU61 to CCU62
- change input function T13HRE from CCU60 to CCU63
- change for port 6.15 the symbol from CC61(CCU60) to CC60(CCU61)
- change for port 8.2 the symbol from CC61(CCU60) to COUT63(CCU61)
- change for port 14.10 the symbol from T3OUT(GPT120) to T6OUT(GPT121)
- add to all SSC signal the assosiated SSC module where is was missing in the pinning
- add section Pin Reliability in Overload
- incease values for absolute maximium parameters I_{IN} and SumI_{IN}
- correct P14.8 O2 as this was incorrected label as O1

The following changes where done between Version 0.63 and 0.7 of this document:

- change value $\mathbf{R_{\Theta JCT}}$ from 2.6 to 3.5 K/W
- change value $\mathbf{R_{\Theta JCB}}$ from 4.3 to 6.1 K/W
- change value $\mathbf{R_{\Theta JA}}$ from 13.6 to 14.7 K/W

- add parameter t_{POR_APP}
- replace in Operating Conditions Parameter Note MA = modulation amplitude by footnote 1)
- remove the redundant test condition I_{OH} for RDSON NMOS
- remove the redundant test condition I_{OL} for RDSON PMOS
- add parameter V_{ILSD} to class S pads
- remove footnote 2 from FADC
- remove capacitance conditions for LVDS pad parameters as loads are defined by interface (MSC) timings

The following changes where done between Version 0.7 and 1.0 of this document:

- add product options **SAK-TC1798S-512F300EP and SAK-TC1798N-512F300EP**
- remove product options **SAK-TC1798F-512F240EP and SAK-TC1798F-512F240EL**
- update block diagrams to cover new options
- add note to TC1798 Logic Symbol figure and pin list for E-RAY pins availability
- add identification registers for new options
- adapt Absolute Maximum Rating
- clarify pad supply levels in Pin Reliability in Overload section
- correct errors for analog inputs in tables 10 and 11
- add note at the end of Pin Reliability in Overload section
- clarify wording for valid operating conditions
- correct section Extended Range Operating Conditions for the 3.3 V area
- increase limit in Extended Range Operating Conditions from 1 hour to 1000 hours
- add negative limit for class S pad leakage
- removed RDSON parameters for class F pads weak driver as only medium is available and update values
- change description of parameter t_{CAL} for the ADC
- update footnote 10 for the ADC
- update definition of INL and TUE for ADC3
- split FADC DNL parameter into two conditions and change value for gain 4 and 8
- update all current values of table 28 (Power Supply Parameters)
- add footnote 5 to I_{DDP}
- improve parameters I_{DDFL3}
- add footnote for D-Flash currents in power section
- add section 5.2.6.1.
- rework first sentence for chapter 5.3
- increase max values for parameter t_B
- reduce min value for t_L for both PLLs
- split f_{VCO} for the system PLL into two conditions
- change formula 10
- add for MLI and SSC timing parameter: valid strong driver medium edge only
- change MLI parameter t_{17} min value

- update parameter description for SSC parameters t_{52}, t_{53}, t_{56}, t_{57}, t_{58}, and t_{59}
- change SSC parameters from CC to SR Symbol for t_{56}, t_{57}, t_{58} and t_{59}
- add note to ERAY parameters for availability
- add parameters t_{15}, t_{16}, t_{17}, t_{18}, and t_{19} to the EBU
- adapt EBU parameters for DDR Timming
- add footnote to Flash parameter t_{ERD}
- change for parameter N_E note from Max. data retention to Min.
- rework the 3.3 V current part of the Power Supply Parameters for better description and usage
  - Parameters I_{DDP_FP}, I_{DDFL3E} and I_{DDFL3R} are removed and replaced in the following way
  - I_{DDP_FP} is replaced by I_{DDP} with the condition including flash programming current
  - I_{DDFL3E} is replaced by I_{DDP} with the condition including flash erase verify current
  - I_{DDFL3R} is replaced by I_{DDP} with the condition including flash read current
  - parameter I_{DDFL3R} was renamed to I_{DDFL3}

The rework of the 3.3 V current part of the Power Supply Parameters was done for simplification and clarification. Former given values could still be used if liked, the new definition results in the same resulting values or slightly better values. The flash module is supplied via I_{DDFL3} and I_{DDP}. For the different flash operating modes in worst case different allocations for the two domains resulting.

The application typical case ‘flash read’ has max I_{DDP} of 25 mA and max I_{DDFL3} of 98 mA resulting is a sum of 123 mA.

The case ‘flash programming’ has max I_{DDP} of 55 mA and max I_{DDFL3} of 29 mA resulting is a sum of 84 mA.

The case ‘flash erase verify’ has max I_{DDP} of 40 mA and max I_{DDFL3} of 98 mA resulting is a sum of 138 mA.

So for the old parameter I_{DDP} with 35 mA, the new version reads as I_{DDP} = 25+I_{DDP_PORST} = 32 mA for the same application relevant case.

The following changes where done between Version 1.0 and 1.1 of this document:

- change V_{ILS} from 2.1V to 1.9V in table 23
- change t_{48} from 100ns to 200ns in table 42
- change t_{49} from 100ns to 200ns in table 42
- extend K_{OVAN} conditon from I_{OV}≤ 0 mA; I_{OV}≥ -1 mA to I_{OV}≤ 0 mA; I_{OV}≥ -2 mA
- change t_8 from -4ns to -2ns in table 43
- change t_{18} from -4ns to -2ns in table 43
- change t_{37} parameter description from ‘Data output delay to WR rising edge, deviation from the ideal programmed value’ to ‘Data output delay to WR falling edge, deviation from the ideal programmed value’ in table 44
- Add R_{DSONx} information for class B pads to table 18
- Add exact definition ‘edge= sharp ; pin out driver= strong’ for the pad conviguration of the rise and fall times in table 18

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