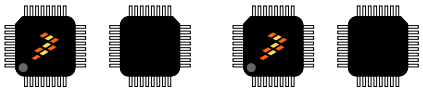
Kinetis KE1xF with up to 512 KB Flash

Up to 168 MHz ARM® Cortex®-M4 Based Microcontroller

MKE1xF512VLL16
MKE1xF512VLH16
MKE1xF256VLL16
MKE1xF256VLH16

The KE1xF microcontroller is built on the ARM® Cortex®-M4 processor with stronger performance and higher memory densities in multiple packages. This device offers up to 168 MHz performance with integrated single-precision floating point unit (FPU) and digital signal processor (DSP). Embedded flash memory sizes range from 256 KB to 512 KB.



100 LQFP (LL)
14x14x1.4 mm Pitch
0.5 mm

64 LQFP (LH)
10x10x1.4 mm Pitch
0.5 mm

Core Processor and System

- ARM® Cortex®-M4 core, supports up to 168 MHz frequency with 1.25 Dhrystone MIPS per MHz
- ARM Core based on the ARMv7 Architecture and Thumb®-2 ISA
- Integrated Digital Signal Processor (DSP)
- Configurable Nested Vectored Interrupt Controller (NVIC)
- Single-precision Floating Point Unit (FPU)
- 16-channel DMA controller extended up to 64 channels with DMAMUX

Reliability, safety and security

- Error-correcting code (ECC) on Flash and SRAM memories
- System memory protection unit (MPU) module
- Flash Access Control (FAC)
- Cyclic Redundancy Check (CRC) generator module
- 128-bit unique identification (ID) number
- Internal watchdog (WDOG) with independent clock source
- External watchdog monitor (EWM) module
- ADC self calibration feature
- On-chip clock loss monitoring

Human-machine interface (HMI)

- Supports up to 92 interrupt request (IRQ) sources
- Up to 89 GPIO pins with interrupt functionality
- 8 high drive pins
- Digital filters

Memory and memory interfaces

- Up to 512 KB program flash with ECC
- Up to 64 KB SRAM with ECC
- 64 KB FlexNVM with ECC for data flash and with EEPROM emulation
- 4 KB FlexRAM for EEPROM emulation
- 8 KB I/D cache to minimize performance impact of memory access latencies
- Boot ROM with built in bootloader

Mixed-signal analog

- 3× 12-bit analog-to-digital converter (ADC) with up to 16 channel analog inputs per module, up to 1M sps
- 3× high-speed analog comparators (CMP) with internal 8-bit digital to analog converter (DAC)
- 1× 12-bit digital to analog converter (DAC)

Timing and control

- 4× Flex Timers (FTM) for PWM generation, offering up to 32 standard channels
- 1× Low-Power Timer (LPTMR) working at Stop mode, with flexible wake up control
- 3× Programmable Delay Block (PDB) with flexible trigger system, to provide accurate delay and trigger generation for inter-module synchronization
- 1× Low-power Periodic Interrupt Timer (LPIT) with 4 independent channels, for general purpose
- Pulse Width Timer (PWT)
- Real timer clock (RTC)

Clock interfaces

- 3 - 40 MHz fast external oscillator (OSC)
- 32 kHz slow external oscillator (OSC32)
- 48 - 60 MHz high-accuracy (up to 1%) fast internal reference clock (FIRC) for high-speed run
- 8 MHz / 2 MHz high-accuracy (up to 3%) slow internal reference clock (SIRC) for low-speed run
- 128 kHz low power oscillator (LPO)
- Phased lock loop (PLL)
- Up to 60 MHz DC external square wave input clock
- System clock generator (SCG)
- Real time counter (RTC)

Power management

- Low-power ARM Cortex-M4 core with excellent energy efficiency
- Power management controller (PMC) with multiple power modes: HSRun, Run, Wait, Stop, VLPR, VLPW and VLPS
- Supports clock gating for unused modules, and specific peripherals remain working in low power modes
- POR, LVD/LVR

Operating Characteristics

- Voltage range: 2.7 to 5.5 V
- Ambient temperature range: –40 to 105 °C

Connectivity and communications interfaces

- TriggerMUX: for module inter-connectivity
- 3× low-power universal asynchronous receiver/ transmitter (LPUART) modules with DMA support and working at Stop mode
- 2 low-power serial peripheral interface (LPSPI) modules with DMA support and working at Stop mode
- 2× low-power inter-integrated circuit (LPI2C) modules with DMA support and working at Stop mode
- Up to 2 ×FlexCAN modules, with flexible message buffers and mailboxes
- FlexIO module for flexible and high performance serial interfaces emulation

Debug functionality

- Serial Wire JTAG Debug Port (SWJ-DP) combines
- Debug Watchpoint and Trace (DWT)
- Instrumentation Trace Macrocell (ITM)
- Test Port Interface Unit (TPIU)
- Flash Patch and Breakpoints (FPB)

Related Resources

Type	Description	Resource
Selector Guide	The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KE1xF512PB [1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KE1xFP100M168SF0RM [1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document: KE1xFP100M168SF0
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_E_0N79P [1]
Package drawing	Package dimensions are provided in package drawings.	100-LQFP: 98ASS23308W 64-LQFP: 98ASS23234W

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

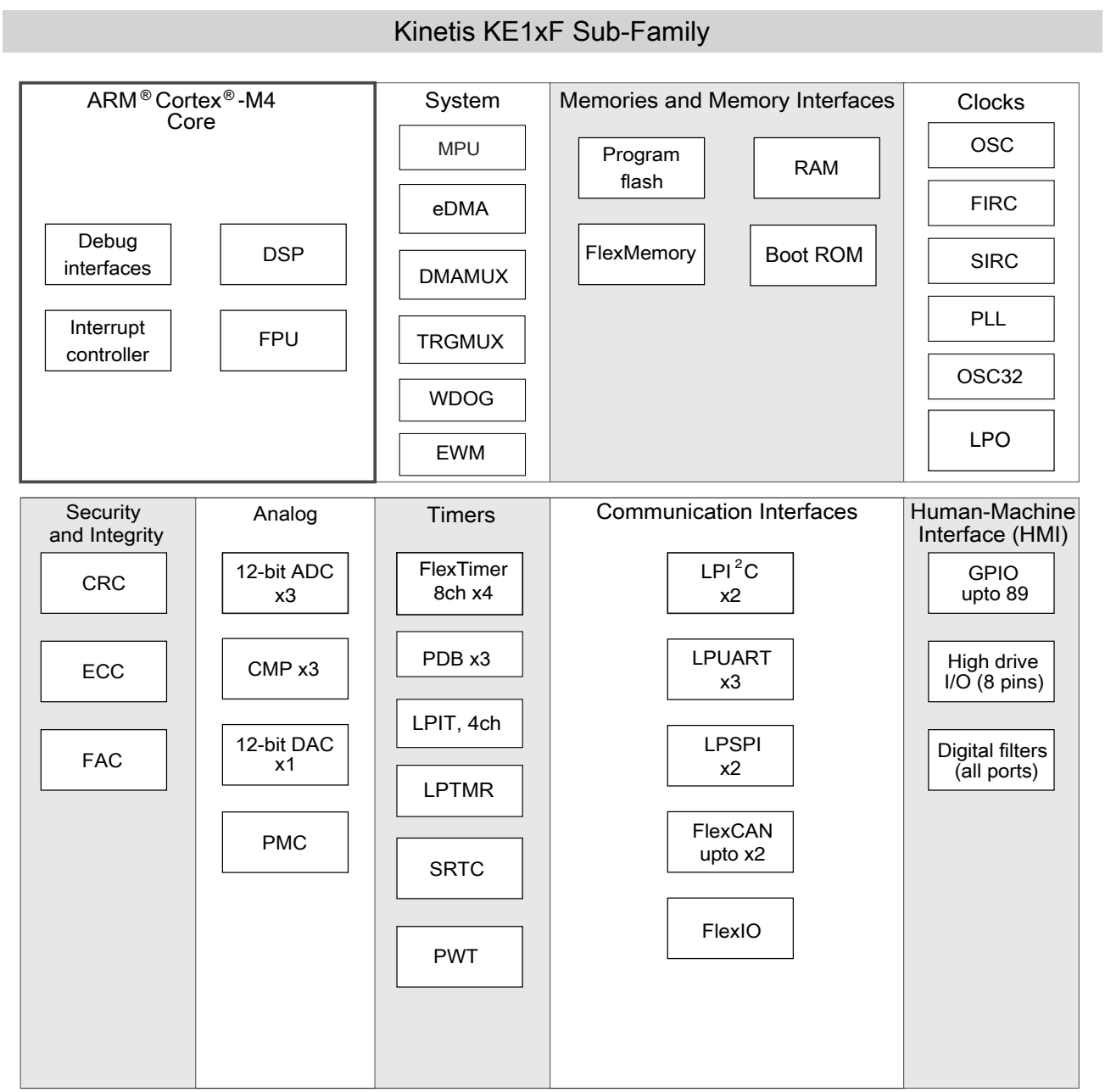


Figure 1. Functional block diagram

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1 Ordering information

The following chips are available for ordering.

Table 1. Ordering information

Product		Memory			Package		IO and ADC channel			Communication
Part number	Marking (Line1/Line2)	Flash (KB)	SRAM (KB)	FlexNVM/ FlexRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD)[1]	ADC channels	FlexCAN
MKE18F512VLL16	MKE18F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	2
MKE18F512VLH16	MKE18F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	2
MKE18F256VLL16	MKE18F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	2
MKE18F256VLH16	MKE18F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	2
MKE16F512VLL16	MKE16F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	1
MKE16F512VLH16	MKE16F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	1
MKE16F256VLL16	MKE16F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	1
MKE16F256VLH16	MKE16F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	1
MKE14F512VLL16	MKE14F512 / VLL16	512	64	64/4	100	LQFP	89	89/8	16	0
MKE14F512VLH16	MKE14F512 / VLH16	512	64	64/4	64	LQFP	58	58/8	16	0
MKE14F256VLL16	MKE14F256 / VLL16	256	32	64/4	100	LQFP	89	89/8	16	0
MKE14F256VLH16	MKE14F256 / VLH16	256	32	64/4	64	LQFP	58	58/8	16	0

1. INT: interrupt pin numbers; HD: high drive pin numbers

2 Overview

The following figure shows the system diagram of this device.

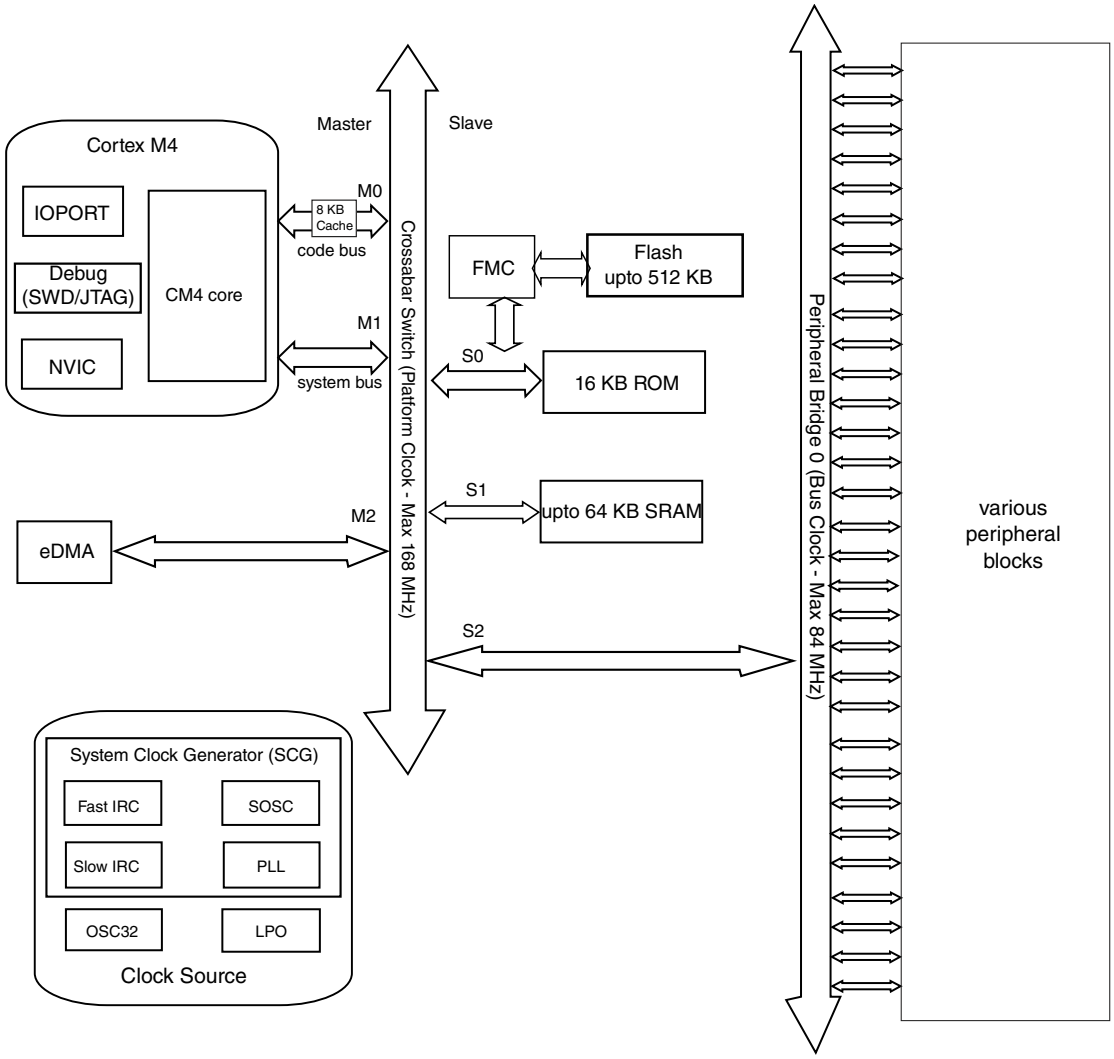


Figure 2. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

2.1.1 ARM Cortex-M4 core

The ARM Cortex-M4 is the member of the Cortex M Series of processors targeting microcontroller cores focused on very cost sensitive, deterministic, interrupt driven environments. The Cortex M4 processor is based on the ARMv7 Architecture and Thumb®-2 ISA and is upward compatible with the Cortex M3, Cortex M1, and Cortex M0 architectures. Cortex M4 improvements include an ARMv7 Thumb-2 DSP (ported from the ARMv7-A/R profile architectures) providing 32-bit instructions with SIMD (single instruction multiple data) DSP style multiply-accumulates and saturating arithmetic.

2.1.2 NVIC

The Nested Vectored Interrupt Controller supports nested interrupts and 16 priority levels for interrupts. In the NVIC, each source in the IPR registers contains 4 bits. It also differs in number of interrupt sources and supports 240 interrupt vectors.

The Cortex-M family uses a number of methods to improve interrupt latency . It also can be used to wake the MCU core from Wait and VLPW modes.

2.1.3 AWIC

The asynchronous wake-up interrupt controller (AWIC) is used to detect asynchronous wake-up events in Stop mode and signal to clock control logic to resume system clocking. After clock restarts, the NVIC observes the pending interrupt and performs the normal interrupt or event processing. The AWIC can be used to wake MCU core from Partial Stop, Stop and VLPS modes.

Wake-up sources for this SoC are listed as below:

Table 2. AWIC Stop and VLPS Wake-up Sources

Wake-up source	Description
Available system resets	RESET pin, WDOG, JTAG , loss of clock(LOC) reset and loss of lock (LOL) reset
Pin interrupts	Port Control Module - Any enabled pin interrupt is capable of waking the system
ADCx	ADCx is optional functional with clock source from SIRC or OSC
CMPx	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPI2C	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPUART	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPSPI	Functional in Stop/VLPS modes with clock source from SIRC or OSC

Table continues on the next page...

Table 2. AWIC Stop and VLPS Wake-up Sources (continued)

Wake-up source	Description
LPIT	Functional in Stop/VLPS modes with clock source from SIRC or OSC
FlexIO	Functional in Stop/VLPS modes with clock source from SIRC or OSC
LPTMR	Functional in Stop/VLPS modes
RTC	Functional in Stop/VLPS modes
SCG	Functional in Stop mode (Only SIRC)
CAN	CAN stop wakeup
NMI	Non-maskable interrupt

2.1.4 Memory

This device has the following features:

- Upto 512 KB of embedded program flash memory.
- Upto 64 KB of embedded SRAM accessible (read/write) at CPU clock speed with 0 wait states.
- The non-volatile memory is divided into several arrays:
  - 64 KB of embedded data flash memory
  - 4 KB of Emulated EEPROM
  - 16 KB ROM (built-in bootloader to support UART, I2C, and SPI interfaces)

The program flash memory contains a 16-byte flash configuration field that stores default protection settings and security information. The page size of program flash is 4 KB.

The protection setting can protect 32 regions of the program flash memory from unintended erase or program operations.

The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

2.1.5 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the

specific module is not reset by the corresponding Reset source.

Table 3. Reset source

Reset sources	Descriptions	Modules									
		PMC	SIM	SMC	RCM	Reset pin is negated	WDOG	SCG	RTC	LPTMR	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
System resets	Low-voltage detect (LVD)	Y[1]	Y	Y	Y	Y	Y	Y	N	Y	Y
	External pin reset ($\overline{\text{RESET}}$)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Watchdog (WDOG) reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Multipurpose clock generator loss of clock (LOC) reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Multipurpose clock generator loss of lock (LOL) reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Stop mode acknowledge error (SACKERR)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Software reset (SW)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	Lockup reset (LOCKUP)	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
	MDM DAP system reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y
Debug reset	Debug reset	Y[1]	Y[2]	Y[3]	Y[4]	Y	Y[5]	Y[6]	N	N	Y

1. Except PMC_LVDSC1[LVDV] and PMC_LVDSC2[LVWV]
2. Except SIM_SOPT1
3. Except SMC_PMPROT, SMC_PMCTRL_RUM, SMC_PMCTRL_STOPM, SMC_STOPCTRL, SMC_PMSTAT
4. Except RCM_RPC, RCM_MR, RCM_FM, RCM_SRIE, RCM_SRS, RCM_SSRS
5. Except WDOG_CS[TST]
6. Except SCG_CSR and SCG_FIRCSTAT

This device supports booting from:

- internal flash
- boot ROM

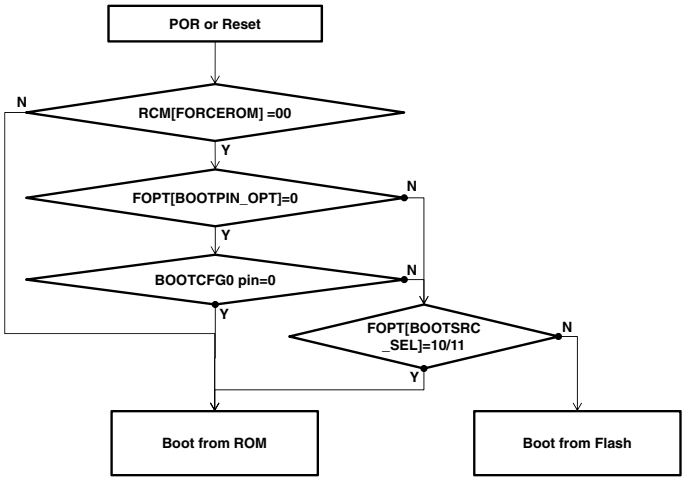


Figure 3. Boot flow chart

The blank chip is default to boot from ROM and remaps the vector table to ROM base address, otherwise, it remaps to flash address.

2.1.6 Clock options

The SCG module controls which clock source is used to derive the system clocks. The clock generation logic divides the selected clock source into a variety of clock domains, including the clocks for the system bus masters, system bus slaves, and flash memory . The clock generation logic also implements module-specific clock gating to allow granular shutoff of modules.

The following figure is a high level block diagram of the clock generation. For more details on the clock operation and configuration, see the Clocking chapter in the Reference Manual.

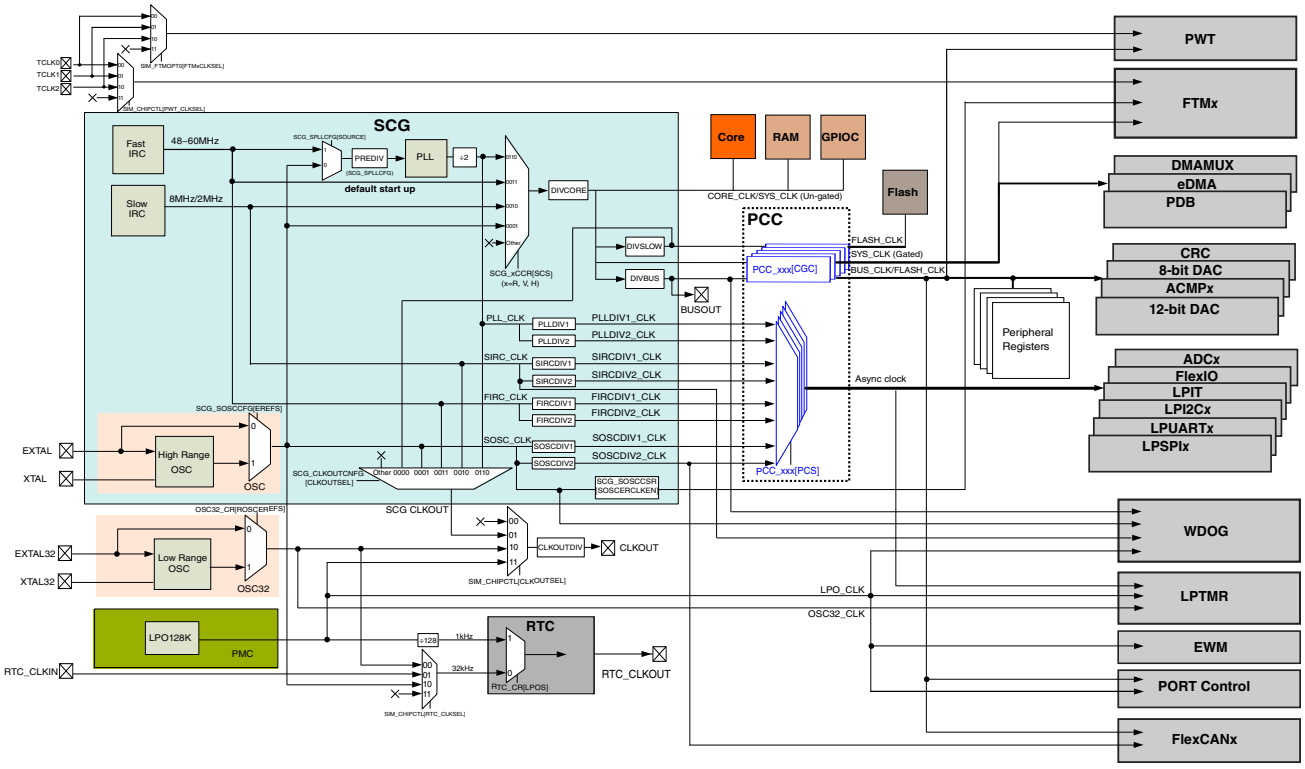


Figure 4. Clocking block diagram

2.1.7 Security

Security state can be enabled via programming flash configure field (0x40e). After enabling device security, the SWD/JTAG port cannot access the memory resources of the MCU.

External interface	Security	Unsecure
SWD/JTAG port	Can't access memory source by SWD/ JTAG interface	the debugger can write to the Flash Mass Erase in Progress field of the MDM-AP Control register to trigger a mass erase (Erase All Blocks) command

2.1.7.1 Flash Access Control (FAC)

The FAC is a native or third-party configurable memory protection scheme optimized to allow end users to utilize software libraries while offering programmable restrictions to these libraries. The flash memory is divided into equal size segments that provide protection to proprietary software libraries. The protection of these

segments is controlled as the FAC provides a cycle-by-cycle evaluation of the access rights for each transaction routed to the on-chip flash memory. Configurability allows an increasing number of protected segments while supporting two levels of vendors adding their proprietary software to a device.

2.1.7.2 Error-correcting code (ECC)

The ECC detection is also supported on Flash and SRAM memories. It supports auto correction of one-bit error and reporting more than one-bit error.

2.1.8 Power management

The Power Management Controller (PMC) expands upon ARM's operational modes of Run, Sleep, and Deep Sleep, to provide multiple configurable modes. These modes can be used to optimize current consumption for a wide range of applications. The WFI or WFE instruction invokes a Wait or a Stop mode, depending on the current configuration. For more information on ARM's operational modes, See the ARM® Cortex® User Guide.

The PMC provides High Speed Run (HSRUN), Normal Run (RUN), and Very Low Power Run (VLPR) configurations in ARM's Run operation mode. In these modes, the MCU core is active and can access all peripherals. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption. The configuration that matches the power versus performance requirements of the application can be selected.

The PMC provides Wait (Wait) and Very Low Power Wait (VLPW) configurations in ARM's Sleep operation mode. In these modes, even though the MCU core is inactive, all of the peripherals can be enabled and operate as programmed. The difference between the modes is the maximum clock frequency of the system and therefore the power consumption.

The PMC provides Stop (Stop), Very Low Power Stop (VLPS) configurations in ARM's Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, please refer to the Reference Manual.

The following table provides information about the state of the peripherals in the various operational modes and the modules that can wake MCU from low power modes.

Table 5. Peripherals states in different operational modes

Core mode	Device mode	Descriptions
Run mode	High Speed Run	In HSRun mode, MCU is able to operate at a faster frequency, and all device modules are operational.
	Run	In Run mode, all device modules are operational.
	Very Low Power Run	In VLPR mode, all device modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled.
Sleep mode	Wait	In Wait mode, all peripheral modules are operational. The MCU core is placed into Sleep mode.
	Very Low Power Wait	In VLPW mode, all peripheral modules are operational at a reduced frequency except the Low Voltage Detect (LVD) monitor, which is disabled. The MCU core is placed into Sleep mode.
Deep sleep	Stop	In Stop mode, most peripheral clocks are disabled and placed in a static state. Stop mode retains all registers and SRAMs while maintaining Low Voltage Detection protection. In Stop mode, the ADC, DAC, CMP, LPTMR, RTC, and pin interrupts are operational. The NVIC is disabled, but the AWIC can be used to wake up from an interrupt.
	Very Low Power Stop	In VLPS mode, the contents of the SRAM are retained. The CMP (low speed), ADC, OSC, RTC, LPTMR, LPIT, FlexIO, LPUART, LPI2C,LPSPI, and DMA are operational, LVD and NVIC are disabled, AWIC is used to wake up from interrupt.

2.1.9 Debug controller

This device has extensive debug capabilities including run control and tracing capabilities. The standard ARM debug port supports SWD/JTAG interface.

2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

2.2.1 eDMA and DMAMUX

The eDMA is a highly programmable data-transfer engine optimized to minimize any required intervention from the host processor. It is intended for use in applications where the data size to be transferred is statically known and not defined within the transferred data itself. The DMA controller in this device implements 16 channels which can be routed from up to 63 DMA request sources through DMA MUX module.

Main features of eDMA are listed below:

- All data movement via dual-address transfers: read from source, write to destination
- 16-channel implementation that performs complex data transfers with minimal intervention from a host processor
- Transfer control descriptor (TCD) organized to support two-deep, nested transfer operations
- Channel activation via one of three methods
- Fixed-priority and round-robin channel arbitration
- Channel completion reported via programmable interrupt requests
- Programmable support for scatter/gather DMA processing
- Support for complex data structures

2.2.2 FTM

This device contains four FlexTimer modules.

The FlexTimer module (FTM) is a two-to-eight channel timer that supports input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. The FTM time reference is a 16-bit counter that can be used as an unsigned or signed counter.

Several key enhancements of this module are made:

- Signed up counter
- Deadtime insertion hardware
- Fault control inputs
- Enhanced triggering functionality
- Initialization and polarity control

2.2.3 ADC

This device contains three 12-bit SAR ADC modules. The ADC module supports hardware triggers from FTM, LPTMR, PIT, RTC, external trigger pin and CMP output. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

- Linear successive approximation algorithm with up to 12-bit resolution
- Up to 16 single-ended external analog inputs
- Support 12-bit, 10-bit, and 8-bit single-ended output modes
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Input clock selectable from up to four sources
- Operation in low-power modes for lower noise
- Selectable hardware conversion trigger
- Automatic compare with interrupt for less-than, greater-than or equal-to, within range, or out-of-range, programmable value
- Temperature sensor
- Hardware average function
- Selectable Voltage reference: from external or alternate
- Self-Calibration mode

2.2.3.1 Temperature sensor

This device contains one temperature sensor internally connected to the input channel of AD26, see ADC electrical characteristics for details of the linearity factor.

The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

2.2.4 DAC

The 12-bit digital-to-analog converter (DAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator, or ADC.

DAC module has the following features:

- On-chip programmable reference generator output. The voltage output range is from 1⁄4096 Vin to V_{in}, and the step is 1⁄4096 V_{in}, where V_{in} is the input voltage.
- V_{in} can be selected from two reference sources

- Static operation in Normal Stop mode
- 16-word data buffer supported with multiple operation modes
- DMA support

2.2.5 CMP

There are three analog comparators on this device.

- Each CMP has its own independent 8-bit DAC.
- Each CMP supports up to 7 analog inputs from external pins.
- Each CMP is able to convert an internal reference from the bandgap.
- Each CMP supports internal reference from the on-chip 12-bit DAC out.
- Each CMP supports the round-robin sampling scheme. In summary, this allow the CMP to operate independently in VLPS and Stop modes, whilst being triggered periodically to sample up to 8 inputs. Only if an input changes state is a full wakeup generated.

The CMP has the following features:

- Inputs may range from rail to rail
- Programmable hysteresis control
- Selectable interrupt on rising-edge, falling-edge, or both rising and falling edges of the comparator output
- Selectable inversion on comparator output
- Capability to produce a wide range of outputs such as sampled, windowed, or digitally filtered
- External hysteresis can be used at the same time that the output filter is used for internal functions
- Two software selectable performance levels: Shorter propagation delay at the expense of higher power, and Low power with longer propagation delay
- DMA transfer support
- Functional in all power modes available on this MCU
- The window and filter functions are not available in STOP mode
- Integrated 8-bit DAC with selectable supply reference source and can be power down to conserve power

2.2.6 RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator, or clock directly from RTC_CLKIN pin.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers.

The RTC module has the following features

- 32-bit seconds counter with roll-over protection and 32-bit alarm
- 16-bit prescaler with compensation that can correct errors between 0.12 ppm and 3906 ppm
- Register write protection with register lock mechanism
- 1 Hz square wave or second pulse output with optional interrupt

2.2.7 LPIT

The Low Power Periodic Interrupt Timer (LPIT) is a multi-channel timer module generating independent pre-trigger and trigger outputs. These timer channels can operate individually or can be chained together. The LPIT can operate in low power modes if configured to do so. The pre-trigger and trigger outputs can be used to trigger other modules on the device.

This device contains one LPIT module with four channels. The LPIT generates periodic trigger events to the DMAMUX.

2.2.8 PDB

The Programmable Delay Block (PDB) provides controllable delays from either an internal or an external trigger, or a programmable interval tick, to the hardware trigger inputs of ADCs and/or generates the interval triggers to DACs, so that the precise timing between ADC conversions and/or DAC updates can be achieved. The PDB can optionally provide pulse outputs (Pulse-Out's) that are used as the sample window in the CMP block.

The PDB module has the following capabilities:

- trigger input sources and one software trigger source
- 1 DAC refresh trigger output, for this device
- configurable PDB channels for ADC hardware trigger
- 1 pulse output, for this device

2.2.9 LPTMR

The low-power timer (LPTMR) can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter

2.2.10 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial, WAS, and other parameters required to implement a 16-bit or 32-bit CRC standard.

The CRC module has the following features:

- Hardware CRC generator circuit using a 16-bit or 32-bit programmable shift register
- Programmable initial seed value and polynomial
- Option to transpose input data or output data (the CRC result) bitwise or bytewise.
- Option for inversion of final CRC result
- 32-bit CPU register programming interface

2.2.11 LPUART

This product contains three Low-Power UART modules, and can work in Stop and VLPS modes. The module also supports 4× to 32× data oversampling rate to meet different applications.

The LPUART module has the following features:

- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4× to 32×

- Transmit and receive baud rate can operate asynchronous to the bus clock and can be configured independently of the bus clock frequency, support operation in Stop mode
- Interrupt, DMA or polled operation
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

2.2.12 LPSPI

This device contains two LPSPI modules. The LPSPI is a low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave. The LPSPI can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses.

The LPSPI modules have the following features:

- Command/transmit FIFO of 4 words
- Receive FIFO of 4 words
- Host request input can be used to control the start time of an SPI bus transfer

2.2.13 FlexCAN

This device contains two FlexCAN modules. The FlexCAN module is a communication controller implementing the CAN protocol according to the ISO 11898-1 standard and CAN 2.0 B protocol specifications.

Each FlexCAN module contains 16 message buffers. Each message buffer is 16 bytes.

The FlexCAN module has the following features:

- Flexible mailboxes of zero to eight bytes data length
- Each mailbox configurable as receive or transmit, all supporting standard and extended messages
- Individual Rx Mask registers per mailbox
- Full-featured Rx FIFO with storage capacity for up to six frames and automatic internal pointer handling with DMA support
- Transmission abort capability
- Programmable clock source to the CAN Protocol Interface, either peripheral clock or oscillator clock
- RAM not used by reception or transmission structures can be used as general purpose RAM space
- Listen-Only mode capability
- Programmable Loop-Back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number, or highest priority
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independence from the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low power modes, with programmable wake up on bus activity
- Remote request frames may be handled automatically or by software
- CAN bit time settings and configuration bits can only be written in Freeze mode
- Tx mailbox status (Lowest priority buffer or empty buffer)
- Identifier Acceptance Filter Hit Indicator (IDHIT) register for received frames
- SYNCH bit available in Error in Status 1 register to inform that the module is synchronous with CAN bus
- CRC status for transmitted message
- Rx FIFO Global Mask register
- Selectable priority between mailboxes and Rx FIFO during matching process
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either 128 extended, 256 standard, or 512 partial (8 bit) IDs, with up to 32 individual masking capability

2.2.14 LPI2C

This device contains two LPI2C modules. The LPI2C is a low power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a master and/or a slave. The LPI2C can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses. The LPI2C implements logic support for standard-mode, fast-mode, fast-mode plus and ultra-fast modes of operation. The LPI2C module also complies with the *System Management Bus (SMBus) Specification, version 2*.

The LPI2C modules have the following features:

- Standard, Fast, Fast+ and Ultra Fast modes are supported
- HS-mode supported in slave mode
- Multi-master support including synchronization and arbitration
- Clock stretching
- General call, 7-bit and 10-bit addressing
- Software reset, START byte and Device ID require software support
- For master mode:
  - command/transmit FIFO of 4 words
  - receive FIFO of 4 words
- For slave mode:
  - separate I2C slave registers to minimize software overhead due to master/slave switching
  - support for 7-bit or 10-bit addressing, address range, SMBus alert and general call address
  - transmit/receive data register supporting interrupt or DMA requests

2.2.15 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to UART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation.

The FlexIO module has the following features:

- Functional in VLPR/VLPW/Stop/VLPS mode provided the clock it is using remains enabled
- Four 32-bit double buffered shift registers with transmit, receive, and data match modes, and continuous data transfer

- The timing of the shifter's shift, load and store events are controlled by the highly flexible 16-bit timer assigned to the shifter
- Two or more shifters can be concatenated to support large data transfer sizes
- Each 16-bit timers operates independently, supports for reset, enable and disable on a variety of internal or external trigger conditions with programmable trigger polarity
- Flexible pin configuration supporting output disabled, open drain, bidirectional output data and output mode
- Supports interrupt, DMA or polled transmit/receive operation

2.2.16 Port control and GPIO

The Port Control and Interrupt (PORT) module provides support for port control, digital filtering, and external interrupt functions. The GPIO data direction and output data registers control the direction and output data of each pin when the pin is configured for the GPIO function. The GPIO input data register displays the logic value on each pin when the pin is configured for any digital function, provided the corresponding Port Control and Interrupt module for that pin is enabled.

The following figure shows the basic I/O pad structure. Pseudo open-drain pins have the p-channel output driver disabled when configured for open-drain operation. None of the I/O pins, including open-drain and pseudo open-drain pins, are allowed to go above VDD.

NOTE

The RESET_b pin is also a normal I/O pad with pseudo open-drain.

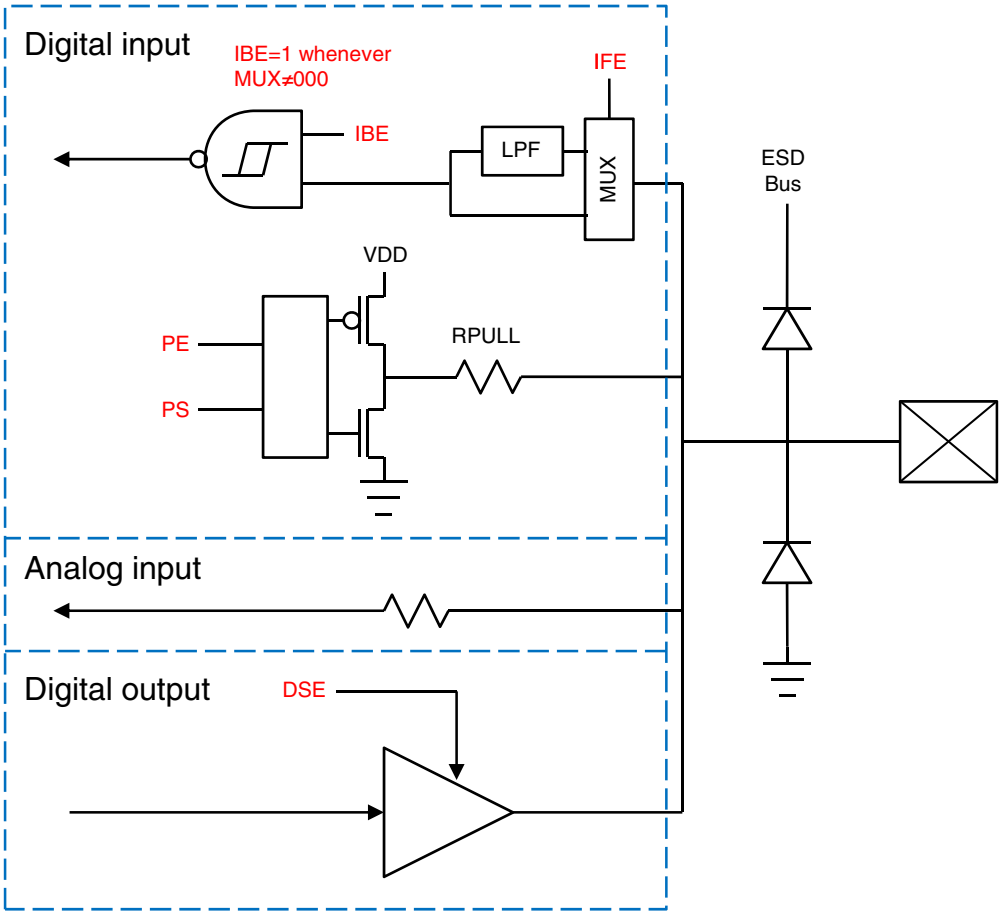


Figure 5. I/O simplified block diagram

The PORT module has the following features:

- all PIN support interrupt enable
- Configurable edge (rising, falling, or both) or level sensitive interrupt type
- Support DMA request
- Asynchronous wake-up in low-power modes
- Configurable pullup, pulldown, and pull-disable on select pins
- Configurable high and low drive strength on selected pins
- Configurable passive filter on selected pins
- Individual mux control field supporting analog or pin disabled, GPIO, and up to chip-specific digital functions
- Pad configuration fields are functional in all digital pin muxing modes.

The GPIO module has the following features:

- Port Data Input register visible in all digital pin-multiplexing modes
- Port Data Output register with corresponding set/clear/toggle registers
- Port Data Direction register
- GPIO support single-cycle access via fast GPIO.

3 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. For more details of the system memory and peripheral locations, see the Memory Map chapter in the Reference Manual.

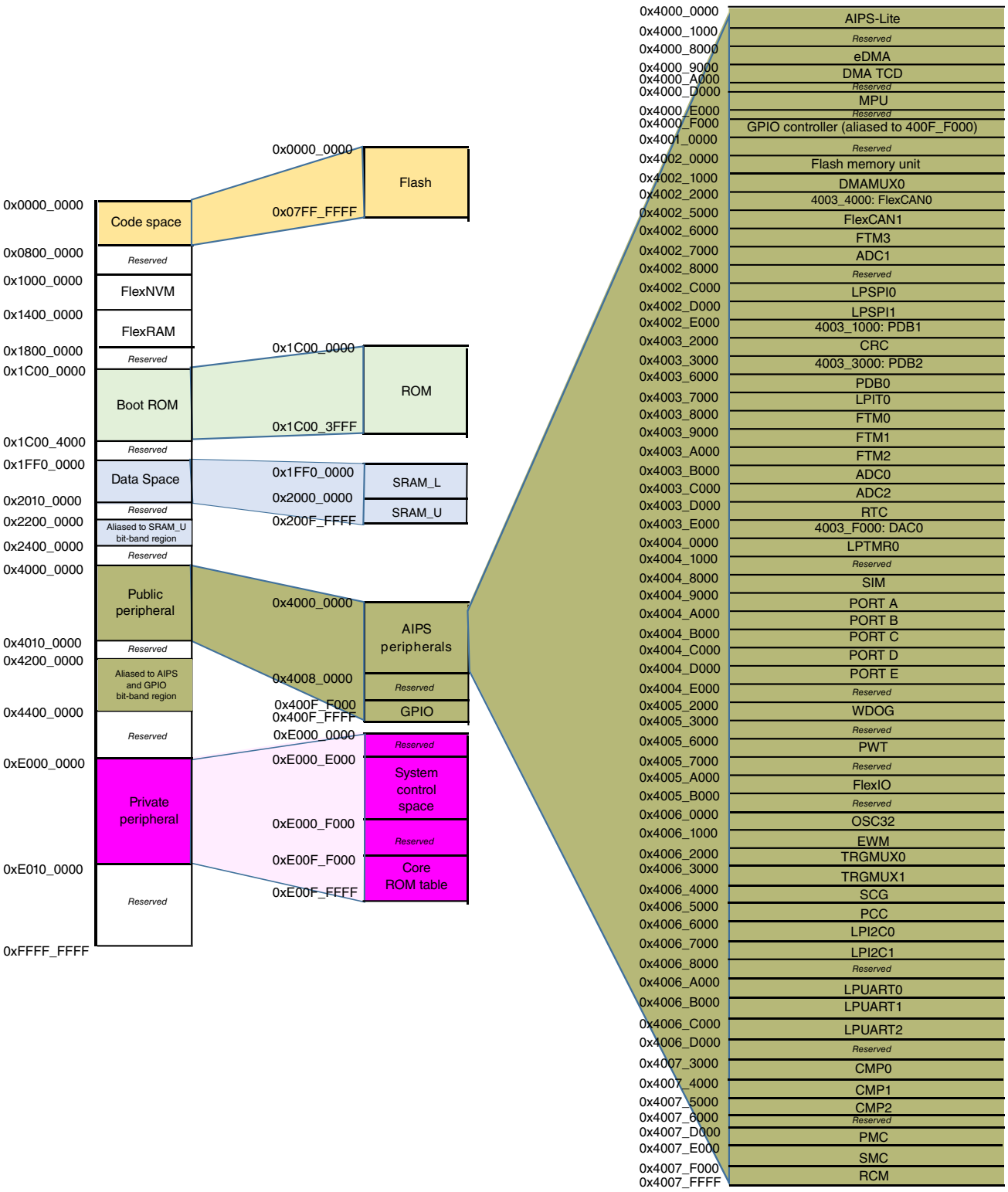


Figure 6. Memory map

4 Pinouts

4.1 KE1xF Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

NOTE

On this device, there are several special ADC channels which support hardware interleave between multiple ADCs. Taking ADC0_SE4 and ADC1_SE14 channels as an example, these two channels can work independently, but they can also be hardware interleaved. In the hardware interleaved mode, a signal on the pin PTB0 can be sampled by both ADC0 and ADC1. The interleaved mode is enabled by SIM_CHIPCTL[ADC_INTERLEAVE_EN] bits. For more information, see "ADC Hardware Interleaved Channels" in the ADC chapter of Reference Manual.

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
—	10	VREFL/ VSS	VREFL/ VSS	VREFL/ VSS							
1	—	PTE16	DISABLED		PTE16			FTM2_CH7		FXIO_D3	TRGMUX_ OUT7
2	—	PTE15	DISABLED		PTE15			FTM2_CH6		FXIO_D2	TRGMUX_ OUT6
3	1	PTD1	ADC2_SE1	ADC2_SE1	PTD1	FTM0_CH3	LPSPI1_SIN	FTM2_CH1		FXIO_D1	TRGMUX_ OUT2
4	2	PTD0	ADC2_SE0	ADC2_SE0	PTD0	FTM0_CH2	LPSPI1_SCK	FTM2_CH0		FXIO_D0	TRGMUX_ OUT1
5	3	PTE11	ADC2_SE13	ADC2_SE13	PTE11	PWT_IN1	LPTMR0_ ALT1	FTM2_CH5		FXIO_D5	TRGMUX_ OUT5
6	4	PTE10	ADC2_SE12	ADC2_SE12	PTE10	CLKOUT		FTM2_CH4		FXIO_D4	TRGMUX_ OUT4
7	—	PTE13	DISABLED		PTE13			FTM2_FLT0			
8	5	PTE5	DISABLED		PTE5	TCLK2	FTM2_QD_ PHA	FTM2_CH3	CAN0_TX	FXIO_D7	EWM_IN
9	6	PTE4	DISABLED		PTE4	BUSOUT	FTM2_QD_ PHB	FTM2_CH2	CAN0_RX	FXIO_D6	EWM_OUT_b

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
10	7	VDD	VDD	VDD							
11	8	VDDA	VDDA	VDDA							
12	9	VREFH	VREFH	VREFH							
13	—	VREFL	VREFL	VREFL							
14	—	VSS	VSS	VSS							
15	11	PTB7	EXTAL	EXTAL	PTB7	LPI2C0_SCL					
16	12	PTB6	XTAL	XTAL	PTB6	LPI2C0_SDA					
17	—	PTE14	ACMP2_IN3	ACMP2_IN3	PTE14	FTM0_FLT1		FTM2_FLT1			
18	13	PTE3	DISABLED		PTE3	FTM0_FLT0	LPUART2_ RTS	FTM2_FLT0		TRGMUX_IN6	ACMP2_OUT
19	—	PTE12	DISABLED		PTE12	FTM0_FLT3	LPUART2_TX				
20	—	PTD17	DISABLED		PTD17	FTM0_FLT2	LPUART2_RX				
21	14	PTD16	ACMP2_IN0	ACMP2_IN0	PTD16	FTM0_CH1					
22	15	PTD15	ACMP2_IN1	ACMP2_IN1	PTD15	FTM0_CH0					
23	16	PTE9	ACMP2_IN2/ DAC0_OUT	ACMP2_IN2/ DAC0_OUT	PTE9	FTM0_CH7	LPUART2_ CTS				
24	—	PTD14	DISABLED		PTD14	FTM2_CH5					CLKOUT
25	—	PTD13	DISABLED		PTD13	FTM2_CH4					RTC_CLKOUT
26	17	PTE8	ACMP0_IN3	ACMP0_IN3	PTE8	FTM0_CH6					
27	18	PTB5	DISABLED		PTB5	FTM0_CH5	LPSPI0_PCS1			TRGMUX_IN0	ACMP1_OUT
28	19	PTB4	ACMP1_IN2	ACMP1_IN2	PTB4	FTM0_CH4	LPSPI0_SOUT			TRGMUX_IN1	
29	20	PTC3	ADC0_SE11/ ACMP0_IN4/ EXTAL32	ADC0_SE11/ ACMP0_IN4/ EXTAL32	PTC3	FTM0_CH3	CAN0_TX				
30	21	PTC2	ADC0_SE10/ ACMP0_IN5/ XTAL32	ADC0_SE10/ ACMP0_IN5/ XTAL32	PTC2	FTM0_CH2	CAN0_RX				
31	22	PTD7	DISABLED		PTD7	LPUART2_TX		FTM2_FLT3			
32	23	PTD6	DISABLED		PTD6	LPUART2_RX		FTM2_FLT2			
33	24	PTD5	DISABLED		PTD5	FTM2_CH3	LPTMR0_ ALT2	FTM2_FLT1	PWT_IN2	TRGMUX_IN7	
34	—	PTD12	DISABLED		PTD12	FTM2_CH2	LPI2C1_HREQ			LPUART2_ RTS	
35	—	PTD11	DISABLED		PTD11	FTM2_CH1	FTM2_QD_ PHA			LPUART2_ CTS	
36	—	PTD10	DISABLED		PTD10	FTM2_CH0	FTM2_QD_ PHB				
37	—	VSS	VSS	VSS							
38	—	VDD	VDD	VDD							
39	25	PTC1	ADC0_SE9/ ACMP1_IN3	ADC0_SE9/ ACMP1_IN3	PTC1	FTM0_CH1				FTM1_CH7	
40	26	PTC0	ADC0_SE8/ ACMP1_IN4	ADC0_SE8/ ACMP1_IN4	PTC0	FTM0_CH0				FTM1_CH6	

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
41	—	PTD9	ACMP1_IN5	ACMP1_IN5	PTD9	LPI2C1_SCL		FTM2_FLT3		FTM1_CH5	
42	—	PTD8	DISABLED		PTD8	LPI2C1_SDA		FTM2_FLT2		FTM1_CH4	
43	27	PTC17	ADC0_SE15	ADC0_SE15	PTC17	FTM1_FLT3		LPI2C1_SCLS			
44	28	PTC16	ADC0_SE14	ADC0_SE14	PTC16	FTM1_FLT2		LPI2C1_SDAS			
45	29	PTC15	ADC0_SE13/ ACMP2_IN4	ADC0_SE13/ ACMP2_IN4	PTC15	FTM1_CH3					
46	30	PTC14	ADC0_SE12/ ACMP2_IN5	ADC0_SE12/ ACMP2_IN5	PTC14	FTM1_CH2					
47	31	PTB3	ADC0_SE7	ADC0_SE7	PTB3	FTM1_CH1	LPSPI0_SIN	FTM1_QD_ PHA		TRGMUX_IN2	
48	32	PTB2	ADC0_SE6	ADC0_SE6	PTB2	FTM1_CH0	LPSPI0_SCK	FTM1_QD_ PHB		TRGMUX_IN3	
49	—	PTC13	DISABLED		PTC13	FTM3_CH7	FTM2_CH7				
50	—	PTC12	DISABLED		PTC12	FTM3_CH6	FTM2_CH6				
51	—	PTC11	DISABLED		PTC11	FTM3_CH5					
52	—	PTC10	DISABLED		PTC10	FTM3_CH4					
53	33	PTB1	ADC0_SE5	ADC0_SE5	PTB1	LPUART0_TX	LPSPI0_SOUT	TCLK0			
54	34	PTB0	ADC0_SE4	ADC0_SE4	PTB0	LPUART0_RX	LPSPI0_PCS0	LPTMR0_ ALT3	PWT_IN3		
55	35	PTC9	ADC2_SE15	ADC2_SE15	PTC9	LPUART1_TX	FTM1_FLT1			LPUART0_ RTS	
56	36	PTC8	ADC2_SE14	ADC2_SE14	PTC8	LPUART1_RX	FTM1_FLT0			LPUART0_ CTS	
57	37	PTA7	ADC0_SE3/ ACMP1_IN1	ADC0_SE3/ ACMP1_IN1	PTA7	FTM0_FLT2		RTC_CLKIN		LPUART1_ RTS	
58	38	PTA6	ADC0_SE2/ ACMP1_IN0	ADC0_SE2/ ACMP1_IN0	PTA6	FTM0_FLT1	LPSPI1_PCS1			LPUART1_ CTS	
59	39	PTE7	ADC2_SE2/ ACMP2_IN6	ADC2_SE2/ ACMP2_IN6	PTE7	FTM0_CH7	FTM3_FLT0				
60	40	VSS	VSS	VSS							
61	41	VDD	VDD	VDD							
62	—	PTA17	DISABLED		PTA17	FTM0_CH6	FTM3_FLT0	EWM_OUT_b			
63	—	PTB17	ADC2_SE3	ADC2_SE3	PTB17	FTM0_CH5	LPSPI1_PCS3				
64	—	PTB16	ADC1_SE15	ADC1_SE15	PTB16	FTM0_CH4	LPSPI1_SOUT				
65	—	PTB15	ADC1_SE14	ADC1_SE14	PTB15	FTM0_CH3	LPSPI1_SIN				
66	—	PTB14	ADC1_SE9	ADC1_SE9	PTB14	FTM0_CH2	LPSPI1_SCK				
67	42	PTB13	ADC1_SE8	ADC1_SE8	PTB13	FTM0_CH1	FTM3_FLT1				
68	43	PTB12	ADC1_SE7	ADC1_SE7	PTB12	FTM0_CH0	FTM3_FLT2				
69	44	PTD4	ADC1_SE6/ ACMP1_IN6	ADC1_SE6/ ACMP1_IN6	PTD4	FTM0_FLT3	FTM3_FLT3				
70	45	PTD3	NMI_b	ADC1_SE3	PTD3	FTM3_CH5	LPSPI1_PCS0	FXIO_D5		TRGMUX_IN4	NMI_b
71	46	PTD2	ADC1_SE2	ADC1_SE2	PTD2	FTM3_CH4	LPSPI1_SOUT	FXIO_D4		TRGMUX_IN5	
72	47	PTA3	ADC1_SE1	ADC1_SE1	PTA3	FTM3_CH1	LPI2C0_SCL	EWM_IN		LPUART0_TX	

100 LQFP	64 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
73	48	PTA2	ADC1_SE0	ADC1_SE0	PTA2	FTM3_CH0	LPI2C0_SDA	EWM_OUT_b		LPUART0_RX	
74	—	PTB11	ADC2_SE8	ADC2_SE8	PTB11	FTM3_CH3	LPI2C0_HREQ				
75	—	PTB10	ADC2_SE9	ADC2_SE9	PTB10	FTM3_CH2	LPI2C0_SDAS				
76	—	PTB9	ADC2_SE10	ADC2_SE10	PTB9	FTM3_CH1	LPI2C0_SCLS				
77	—	PTB8	ADC2_SE11	ADC2_SE11	PTB8	FTM3_CH0					
78	49	PTA1	ADC0_SE1/ ACMP0_IN1	ADC0_SE1/ ACMP0_IN1	PTA1	FTM1_CH1	LPI2C0_SDAS	FXIO_D3	FTM1_QD_ PHA	LPUART0_ RTS	TRGMUX_ OUT0
79	50	PTA0	ADC0_SE0/ ACMP0_IN0	ADC0_SE0/ ACMP0_IN0	PTA0	FTM2_CH1	LPI2C0_SCLS	FXIO_D2	FTM2_QD_ PHA	LPUART0_ CTS	TRGMUX_ OUT3
80	51	PTC7	ADC1_SE5	ADC1_SE5	PTC7	LPUART1_TX	CAN1_TX	FTM3_CH3			
81	52	PTC6	ADC1_SE4	ADC1_SE4	PTC6	LPUART1_RX	CAN1_RX	FTM3_CH2			
82	—	PTA16	ADC1_SE13	ADC1_SE13	PTA16	FTM1_CH3	LPSPI1_PCS2				
83	—	PTA15	ADC1_SE12	ADC1_SE12	PTA15	FTM1_CH2	LPSPI0_PCS3				
84	53	PTE6	ADC1_SE11/ ACMP0_IN6	ADC1_SE11/ ACMP0_IN6	PTE6	LPSPI0_PCS2		FTM3_CH7		LPUART1_ RTS	
85	54	PTE2	ADC1_SE10	ADC1_SE10	PTE2	LPSPI0_SOUT	LPTMR0_ ALT3	FTM3_CH6	PWT_IN3	LPUART1_ CTS	
86	—	VSS	VSS	VSS							
87	—	VDD	VDD	VDD							
88	—	PTA14	DISABLED		PTA14	FTM0_FLT0	FTM3_FLT1	EWM_IN		FTM1_FLT0	BUSOUT
89	55	PTA13	ADC2_SE4	ADC2_SE4	PTA13	FTM1_CH7	CAN1_TX	LPI2C1_SCLS			
90	56	PTA12	ADC2_SE5	ADC2_SE5	PTA12	FTM1_CH6	CAN1_RX	LPI2C1_SDAS			
91	57	PTA11	DISABLED		PTA11	FTM1_CH5	LPUART0_RX	FXIO_D1			
92	58	PTA10	JTAG_TDO/ noetm_Trace_ SWO		PTA10	FTM1_CH4	LPUART0_TX	FXIO_D0			JTAG_TDO/ noetm_Trace_ SWO
93	59	PTE1	ADC2_SE6	ADC2_SE6	PTE1	LPSPI0_SIN	LPI2C0_HREQ	LPI2C1_SCL		FTM1_FLT1	
94	60	PTE0	ADC2_SE7	ADC2_SE7	PTE0	LPSPI0_SCK	TCLK1	LPI2C1_SDA		FTM1_FLT2	
95	61	PTC5	JTAG_TDI		PTC5	FTM2_CH0	RTC_CLKOUT	LPI2C1_HREQ		FTM2_QD_ PHB	JTAG_TDI
96	62	PTC4	JTAG_TCLK/ SWD_CLK	ACMP0_IN2	PTC4	FTM1_CH0	RTC_CLKOUT		EWM_IN	FTM1_QD_ PHB	JTAG_TCLK/ SWD_CLK
97	63	PTA5	RESET_b		PTA5		TCLK1			JTAG_TRST_b	RESET_b
98	64	PTA4	JTAG_TMS/ SWD_DIO		PTA4			ACMP0_OUT	EWM_OUT_b		JTAG_TMS/ SWD_DIO
99	—	PTA9	DISABLED		PTA9			FXIO_D7	FTM3_FLT2	FTM1_FLT3	
100	—	PTA8	DISABLED		PTA8			FXIO_D6	FTM3_FLT3		

4.2 Port control and interrupt summary

The following table provides more information regarding the Port Control and Interrupt configurations.

Table 6. Ports summary

Feature	Port A	Port B	Port C	Port D	Port E
Pull select control	Yes	Yes	Yes	Yes	Yes
Pull select at reset	PTA4/PTA5=Pull up, Others=No	No	PTC5=Pull up, Others=No	PTD3=Pull up, Others=No	No
Pull enable control	Yes	Yes	Yes	Yes	Yes
Pull enable at reset	PTA4/ PTA5=Enabled; Others=Disabled	Disabled	PTC4/ PTC5=Enabled; Others=Disabled	PTD3=Enabled; Others=Disabled	Disabled
Passive filter enable control	PTA5=Yes; Others=No	No	No	PTD3=Yes; Others=No	No
Passive filter enable at reset	PTA5=Enabled; Others=Disabled	Disabled	Disabled	Disabled	Disabled
Open drain enable control	Disabled	Disabled	Disabled	Disabled	Disabled
Open drain enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Drive strength enable control	No	PTB4/PTB5 only	No	PTD0/PTD1/ PTD15/PTD16 only	PTE0/PTE1 only
Drive strength enable at reset	Disabled	Disabled	Disabled	Disabled	Disabled
Pin mux control	Yes	Yes	Yes	Yes	Yes
Pin mux at reset	PTA4/PTA5/ PTA10=ALT7; Others=ALT0	ALT0	PTC4/PTC5=ALT7; Others=ALT0	PTD3=ALT7; Others=ALT0	ALT0
Lock bit	Yes	Yes	Yes	Yes	Yes
Interrupt and DMA request	Yes	Yes	Yes	Yes	Yes
Digital glitch filter	Yes	Yes	Yes	Yes	Yes

4.3 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

4.3.1 Core Modules

Table 7. JTAG Signal Descriptions

Chip signal name	Module signal name	Description	I/O
JTAG_TMS	JTAG_TMS/ SWD_DIO	JTAG Test Mode Selection	I/O
JTAG_TCLK	JTAG_TCLK/ SWD_CLK	JTAG Test Clock	I
JTAG_TDI	JTAG_TDI	JTAG Test Data Input	I
JTAG_TDO	JTAG_TDO/ TRACE_SWO	JTAG Test Data Output	O
JTAG_TRST_b	JTAG_TRST_b	JTAG Reset	I

Table 8. SWD Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SWD_CLK	JTAG_TCLK/ SWD_CLK	Serial Wire Clock	I
SWD_DIO	JTAG_TMS/ SWD_DIO	Serial Wire Data	I/O

Table 9. TPIU Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TRACE_SWO	JTAG_TDO/ TRACE_SWO	Trace output data from the ARM CoreSight debug block over a single pin	O

4.3.2 System Modules

Table 10. System Signal Descriptions

Chip signal name	Module signal name	Description	I/O
NMI_b	—	Non-maskable interrupt NOTE: Driving the NMI signal low forces a non-maskable interrupt, if the NMI function is selected on the corresponding pin.	I
RESET_b	—	Reset bidirectional signal	I/O
VDD	—	MCU power	I
VSS	—	MCU ground	I

Table 11. EWM Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EWM_IN	EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_IN is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
EWM_OUT_b	$\overline{\text{EWM\_out}}$	EWM reset out signal	O

4.3.3 Clock Modules

Table 12. OSC (in SCG) Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL	EXTAL	External clock/Oscillator input	I
XTAL	XTAL	Oscillator output	O

Table 13. RTC Oscillator (OSC32) Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL32	EXTAL32	32.768 kHz oscillator input	I
XTAL32	XTAL32	32.768 kHz oscillator output	O

4.3.4 Analog

Table 14. ADC*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ADC*n*_SE[15:0]	AD[15:0]	Single-Ended Analog Channel Inputs	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VREFL	V_{REFSL}	Voltage Reference Select Low	I
VDDA	V_{DDA}	Analog Power Supply	I

Table 15. DAC0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
DAC0_OUT	—	DAC output	O

Table 16. ACMP*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
ACMP*n*_IN[6:0]	IN[6:0]	Analog voltage inputs	I
ACMP*n*_OUT	CMPO	Comparator output	O

4.3.5 Timer Modules

Table 17. LPTMR0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[3:1]	LPTMR_ALT*n*	Pulse Counter Input pin	I

Table 18. RTC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
RTC_CLKOUT	RTC_CLKOUT	1 Hz square-wave output or 32 kHz clock	O

Table 19. FTM*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FTM*n*_CH[7:0]	CHn	FTM channel (n), where n can be 7-0	I/O
FTM*n*_FLT[3:0]	FAULTj	Fault input (j), where j can be 3-0	I
TCLK[2:0]	EXTCLK	External clock. FTM external clock can be selected to drive the FTM counter.	I

4.3.6 Communication Interfaces

Table 20. CAN*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
CAN*n*_RX	CAN Rx	CAN Receive Pin	I
CAN*n*_TX	CAN Tx	CAN Transmit Pin	O

Table 21. LPSPI*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPSPI*n*_SOUT	SOUT	Serial Data Out	O
LPSPI*n*_SIN	SIN	Serial Data In	I
LPSPI*n*_SCK	SCK	Serial Clock	I/O
LPSPI*n*_PCS[3:0]	PCS[3:0]	Peripheral Chip Select 0-3	I/O

Table 22. LPI2C*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPI2C*n*_SCL	SCL	Bidirectional serial clock line of the I2C system.	I/O
LPI2C*n*_SDA	SDA	Bidirectional serial data line of the I2C system.	I/O
LPI2C*n*_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C*n*_SCLS	SCLS	Secondary I2C clock line.	I/O
LPI2C*n*_SDAS	SDAS	Secondary I2C data line.	I/O

Table 23. LPUART*n* Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART*n*_TX	LPUART_TX	Transmit data	O
LPUART*n*_RX	LPUART_RX	Receive data	I
LPUART*n*_CTS	LPUART_CTS	Clear to send	I
LPUART*n*_RTS	LPUART_RTS	Request to send	O

Table 24. FlexIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FXIO_D[7:0]	FXIO_D[7:0]	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O

4.3.7 Human-Machine Interfaces (HMI)

Table 25. GPIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
PTA[17:0]	PORTA17–PORTA0	General-purpose input/output	I/O
PTB[17:0]	PORTB17–PORTB0	General-purpose input/output	I/O
PTC[17:0]	PORTC17–PORTC0	General-purpose input/output	I/O
PTD[17:0]	PORTD17–PORTD0	General-purpose input/output	I/O
PTE[16:0]	PORTE16–PORTE0	General-purpose input/output	I/O

4.4 Pinout diagram

The following figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous table of Pin Assignments.

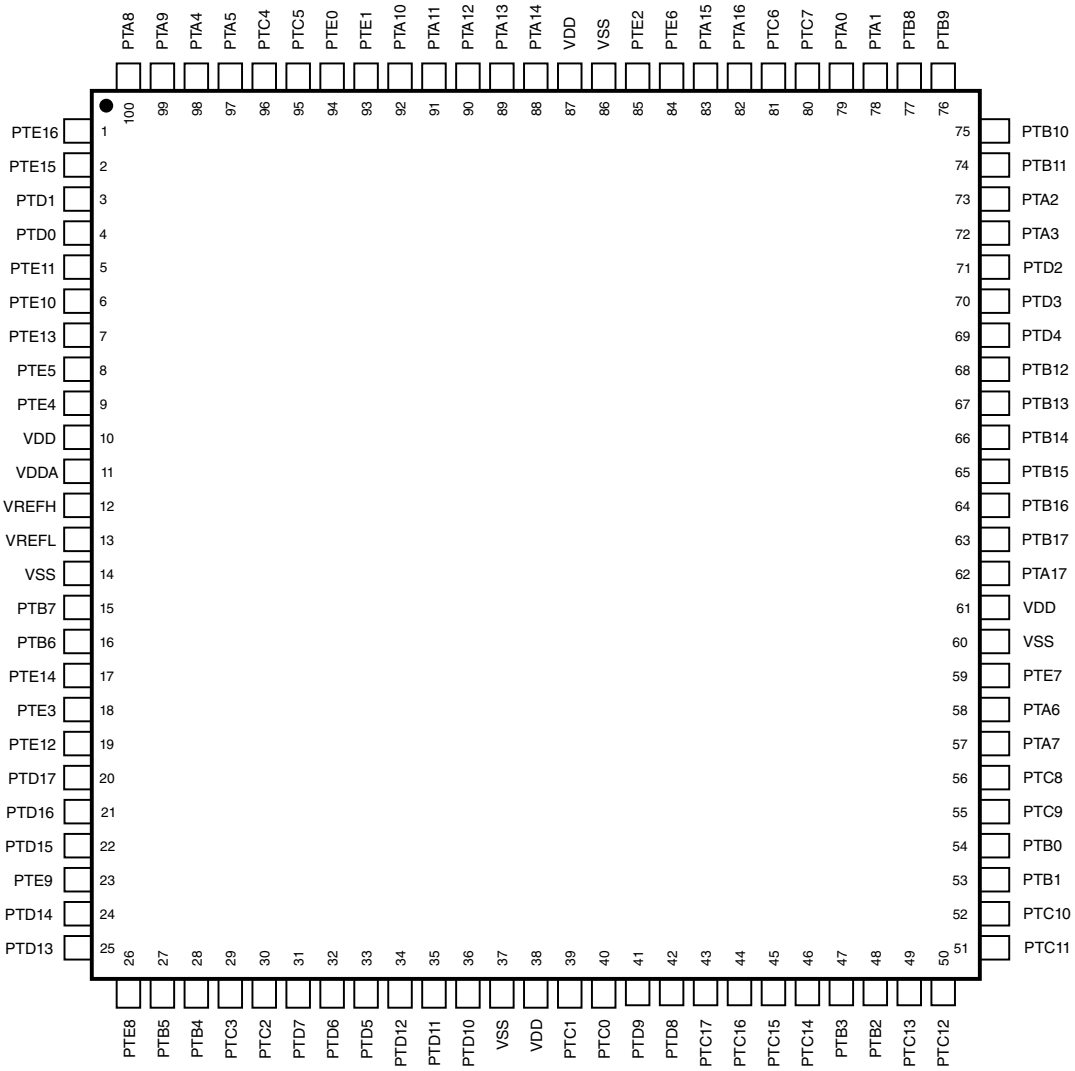


Figure 7. 100 LQFP Pinout Diagram

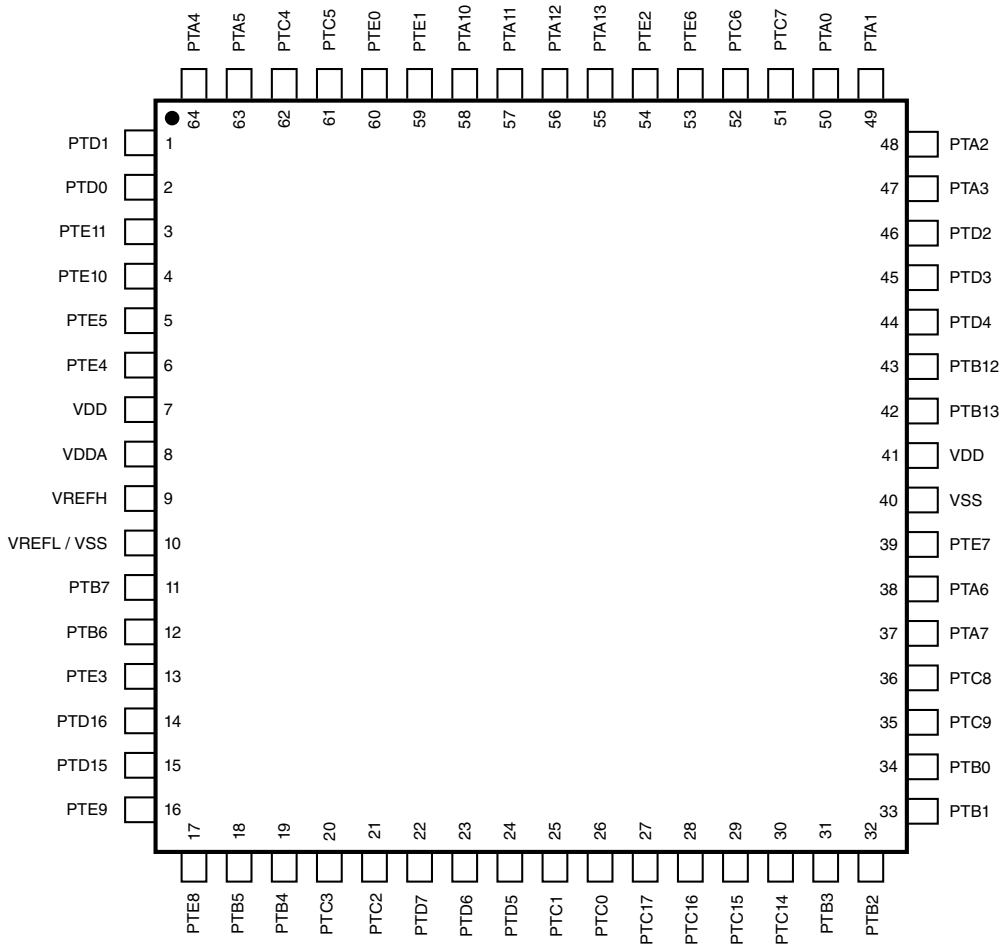


Figure 8. 64 LQFP Pinout Diagram

4.5 Package dimensions

The following figures show the dimensions of the package options for the devices supported by this document.

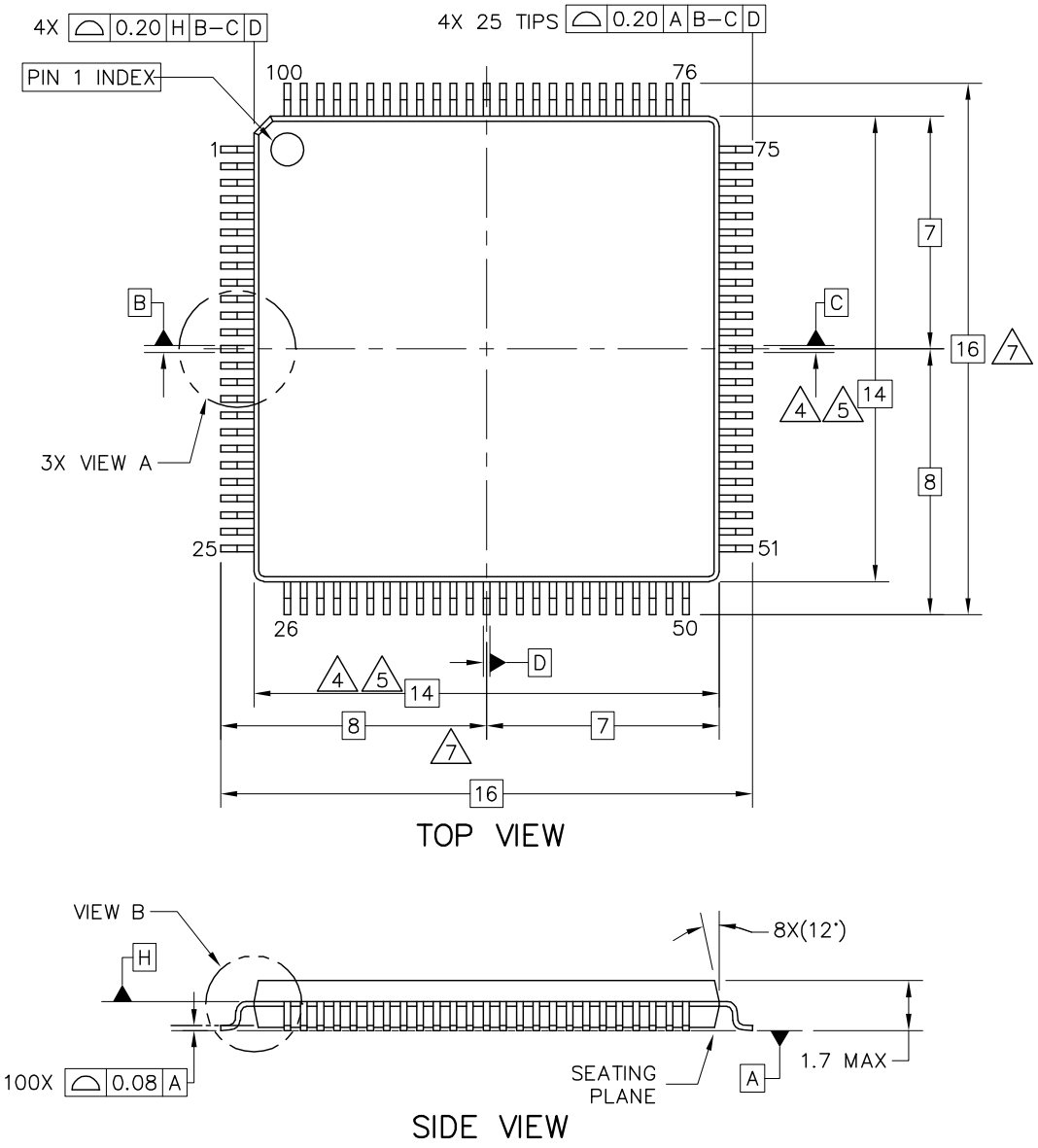
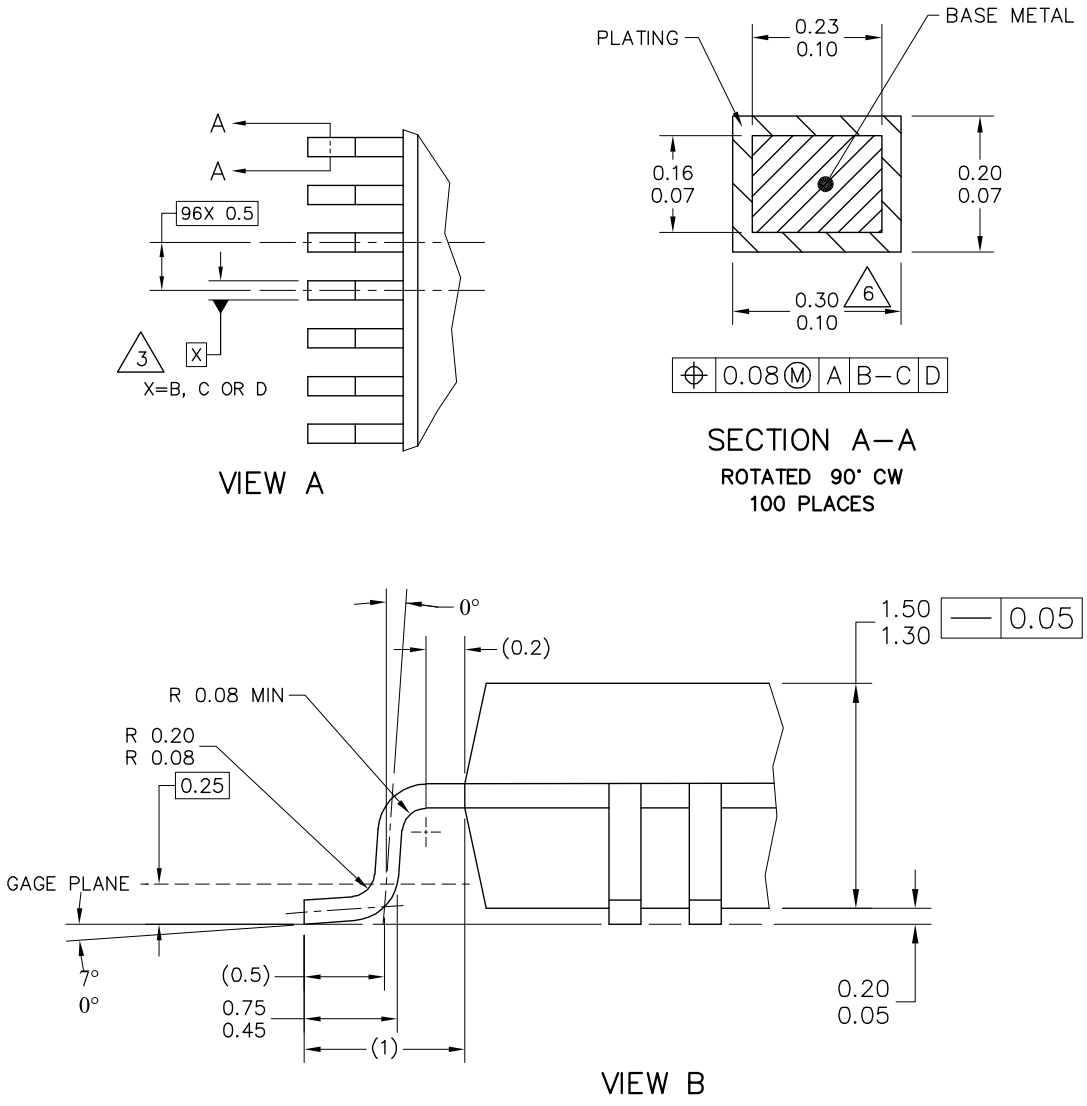


Figure 9. 100-pin LQFP package dimensions 1



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.
4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.
5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.
7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.

Figure 10. 100-pin LQFP package dimensions 2

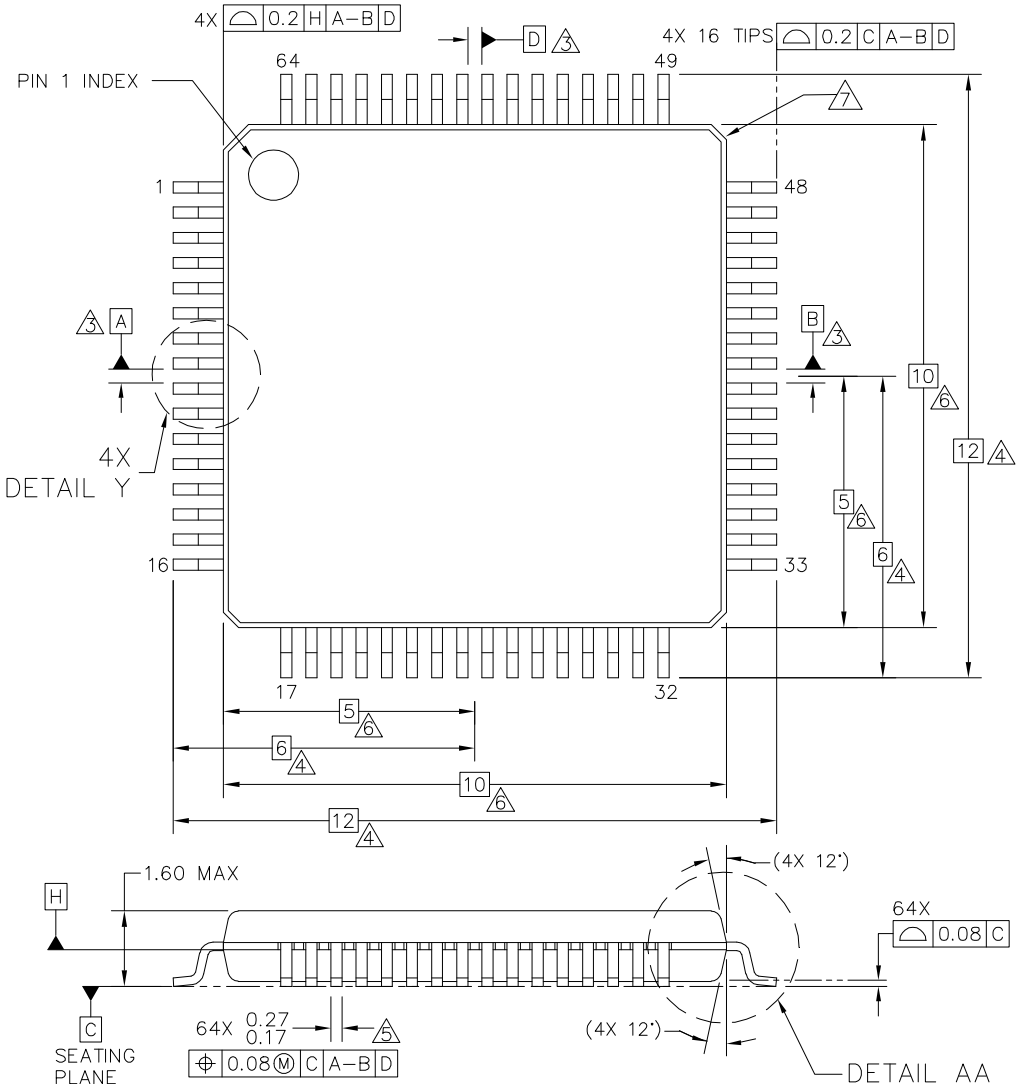
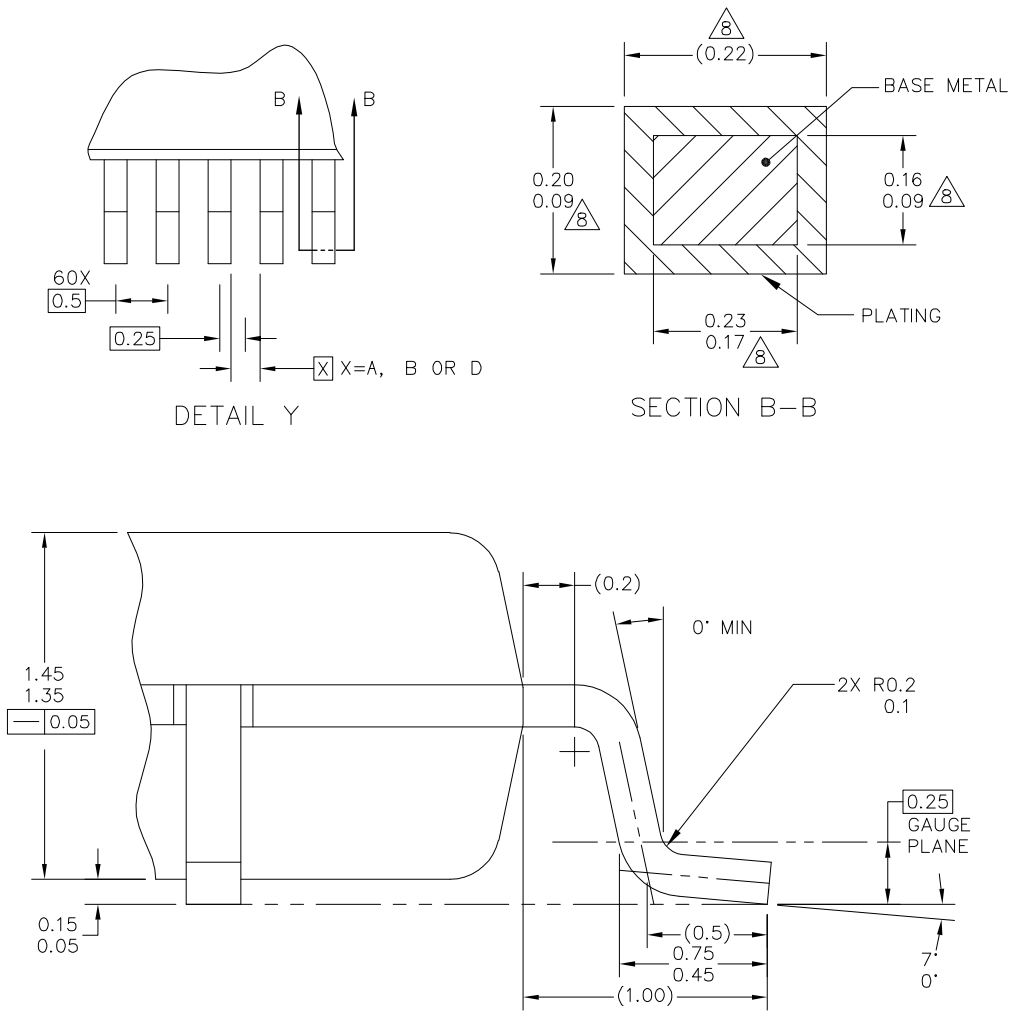


Figure 11. 64-pin LQFP package dimensions 1



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 MM AND 0.25 MM FROM THE LEAD TIP.

Figure 12. 64-pin LQFP package dimensions 2

5 Electrical characteristics

5.1 Terminology and guidelines

5.1.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

5.1.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

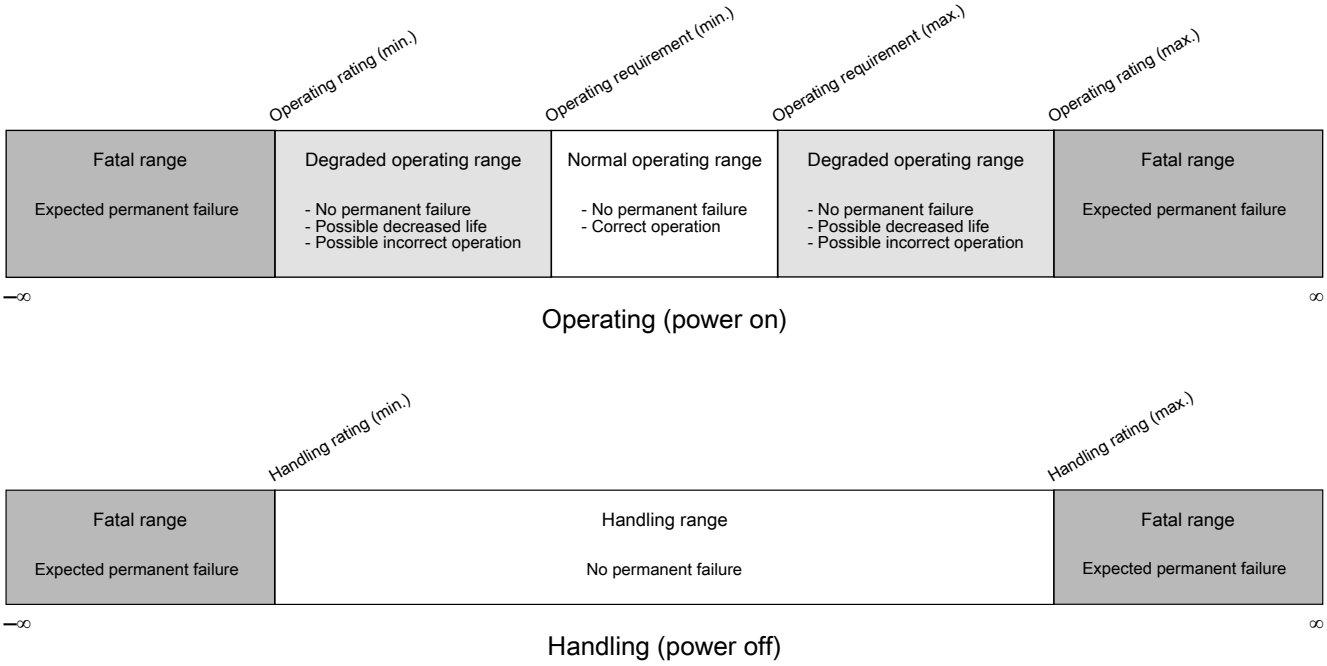
Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

5.1.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	Supply voltage	5.0	V

5.1.4 Relationship between ratings and operating requirements



5.1.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

5.2 Ratings

5.2.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5.2.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	– 6000	6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I_{LAT}	Latch-up current at ambient temperature upper limit	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

5.2.4 Voltage and current operating ratings

Table 26. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Supply voltage	2.7	5.5	V
I_{DD}	Digital supply current	—	80	mA
V_{IO}	IO pin input voltage	V_{SS} – 0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.1	V_{DD} + 0.1	V

5.3 General

5.3.1 Nonswitching electrical specifications

5.3.1.1 Voltage and current operating requirements

Table 27. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	5.5	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	– 0.1	0.1	V	
I_{ICIO}	Analog DC injection current — single pin				
	$V_{IN} < V_{SS}$ - 0.3 V (Negative current injection)	– 5	—	mA	1, 2
	$V_{IN} > V_{DD}$ + 0.3 V (Positive current injection)	—	+ 5	mA	
I_{ICcont}	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins	– 25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	3

1. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is less than V_{AIO_MIN} or greater than V_{AIO_MAX}, a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{ICIO}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO\_MAX})/|I_{ICIO}|$. Select the larger of these two calculated resistances if the pin is exposed to positive and negative injection currents.
2. Max voltage levels that I/O pins can withstand while keeping the injection current (maximum) at 5mA:
   - Max supply V_{DD} = 6.0 V for 60 s lifetime (with no switching restrictions) or for 10 hours (if device is in reset or no switching state)
   - Max I/O pin voltage = 6.5 V (at injection current ≤ 5 mA) or 7.0 V (at injection current > 5 mA)
3. Open drain outputs must be pulled to V_{DD}.

5.3.1.2 DC electrical specifications at 3.3 V Range and 5.0 V Range

Table 28. DC electrical specifications

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
V_{DD}	I/O Supply Voltage [1] @ V_{DD} = 3.3 V	2.7	3.3	4	V	
	@ V_{DD} = 5.0 V	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage @ V_{DD} = 3.3 V	0.7 × V_{DD}	—	V_{DD} + 0.3	V	
	@ V_{DD} = 5.0 V	0.65 × V_{DD}	—	V_{DD} + 0.3	V	

Table continues on the next page...

Table 28. DC electrical specifications (continued)

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
V_{il}	Input Buffer Low Voltage @ V_{DD} = 3.3 V	V_{SS} – 0.3	—	0.3 × V_{DD}	V	
	@ V_{DD} = 5.0 V	V_{SS} – 0.3	—	0.35 × V_{DD}	V	
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_5	Normal drive I/O current source capability measured when pad = (V_{DDE} – 0.8 V) @ V_{DD} = 3.3 V	2.8	—	—	mA	
	@ V_{DD} = 5.0 V	4.8	—	—	mA	
Iol_5	Normal drive I/O current sink capability measured when pad = 0.8 V @ V_{DD} = 3.3 V	2.4	—	—	mA	
	@ V_{DD} = 5.0 V	4.4	—	—	mA	
Ioh_20	High drive I/O current source capability measured when pad = (V_{DDE} – 0.8 V)[2] @ V_{DD} = 3.3 V	10.8	—	—	mA	
	@ V_{DD} = 5.0 V	18.5	—	—	mA [3]	
Iol_20	High drive I/O current sink capability measured when pad = 0.8 V[4] @ V_{DD} = 3.3 V	10.1	—	—	mA	
	@ V_{DD} = 5.0 V	18.5	—	—	mA [3]	
I_leak	Hi-Z (Off state) leakage current (per pin)	—	—	300	nA	5, 6
V_{OH}	Output high voltage					7
	Normal drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –2.8 mA)	V_{DD} – 0.8	—	—	V	
	Normal drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –4.8 mA)	V_{DD} – 0.8	—	—	V	
	High drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –10.8 mA)	V_{DD} – 0.8	—	—	V	
	High drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –18.5 mA)	V_{DD} – 0.8	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage					7
	Normal drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –2.8 mA)	—	—	0.8	V	
	Normal drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –4.8 mA)	—	—	0.8	V	
	High drive pad (2.7 V ≤ V_{DD} ≤ 4.0 V, I_{OH} = –10.8 mA)	—	—	0.8	V	
	High drive pad (4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH} = –18.5 mA)	—	—	0.8	V	

Table continues on the next page...

Table 28. DC electrical specifications (continued)

Symbol	Parameter	Value			Unit	Notes
		Min	Typ	Max		
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range @ V_{DD} = 3.3 V					8, 7
	All pins other than high drive port pins	—	0.002	0.5	µA	
	High drive port pins	—	0.004	0.5	µA	
	Input leakage current (per pin) for full temperature range @ V_{DD} = 5.5 V					
	All pins other than high drive port pins	—	0.005	0.5	µA	
	High drive port pins	—	0.010	0.5	µA	
R_{PU}	Internal pull-up resistors @ V_{DD} = 3.3 V	20	—	65	kΩ	9
	@ V_{DD} = 5.0 V	20	—	50	kΩ	
R_{PD}	Internal pull-down resistors @ V_{DD} = 3.3 V	20	—	65	kΩ	10
	@ V_{DD} = 5.0 V	20	—	50	kΩ	

1. Max power supply ramp rate is 500 V/ms.
2. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_5 value given above.
3. The 20 mA I/O pin is capable of switching a 50 pF load at up to 40 MHz.
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_5 value given above.
5. Refers to the current that leaks into the core when the pad is in Hi-Z (Off state).
6. Maximum pin leakage current at the ambient temperature upper limit.
7. PTD0, PTD1, PTD15, PTD16, PTB4, PTB5, PTE0 and PTE1 I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only.
8. Refers to the pin leakage on the GPIOs when they are OFF.
9. Measured at V_{DD} supply voltage = V_{DD} min and input V = V_{SS}
10. Measured at V_{DD} supply voltage = V_{DD} min and input V = V_{DD}

5.3.1.3 Voltage regulator electrical characteristics

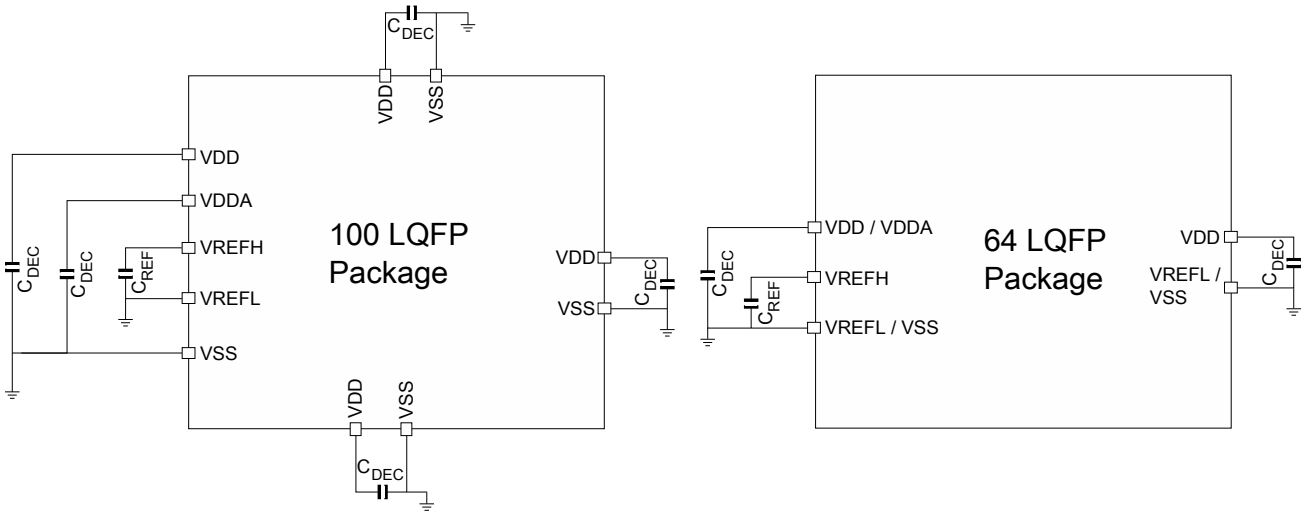


Figure 13. Pinout decoupling

Table 29. Voltage regulator electrical characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
C_{REF} [1, 2]	ADC reference high decoupling capacitance	—	100	—	nF
C_{DEC} [2, 3]	Recommended decoupling capacitance	—	100	—	nF

1. For improved ADC performance it is recommended to use 1 nF X7R/C0G and 10 nF X7R ceramics in parallel.
2. The capacitors should be placed as close as possible to the VREFH/VREFL pins or corresponding V_{DD}/V_{SS} pins.
3. The requirement and value of of C_{DEC} will be decided by the device application requirement.

NOTE

For 64 LQFP, the external decoupling capacitor C_{DEC} must be added, and the minimum value is 100 nF.

5.3.1.4 LVR, LVD and POR operating requirements

Table 30. V_{DD} supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and Falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVRX}	LVRX falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVRX_HYST}	LVRX hysteresis	—	45	—	mV	1
V_{LVRX_LP}	LVRX falling threshold (VLPS/VLPR modes)	1.97	2.12	2.44	V	
$V_{LVRX\_LP\_HYST}$	LVRX hysteresis (VLPS/VLPR modes)	—	40	—	mV	
V_{LVD}	Falling low-voltage detect threshold	2.8	2.88	3	V	

Table continues on the next page...

Table 30. V_{DD} supply LVR, LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVD_HYST}	LVD hysteresis	—	50	—	mV	1
V_{LVW}	Falling low-voltage warning threshold	4.19	4.31	4.5	V	
V_{LVW_HYST}	LVW hysteresis		68		mV	1
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

5.3.1.5 Power mode transition operating behaviors

Table 31. Power mode transition operating behaviors

Description	System Clock	Core, Bus, Flash frequency (MHz)	Min.	Typ. (µs)[1]	Max. (µs)[2]
STOP→RUN	FIRC	48, 48, 24	—	7.32	12.8
STOP→RUN	SPLL	120, 60, 24	—	7.04	12.6
VLPS→RUN	FIRC	48, 48, 24	—	7.32	12.9
VLPS→RUN	SPLL	120, 60, 24	—	142	149
RUN→HSRUN	SPLL	120, 60, 24→120, 60, 24	—	3.96	6.74
HSRUN→RUN	SPLL	120, 60, 24→120, 60, 24	—	0.704	1.155
RUN→VLPR	SPLL→SIRC	120, 60, 24→4, 4, 1	—	7.62	8.54
VLPR→RUN	SIRC→FIRC	4, 4, 1→48, 48, 24	—	19.4	31.8
VLPR→RUN	SIRC→SPLL	4, 4, 1→120, 60, 24	—	157	168
WAIT→RUN	FIRC	48, 48, 24	—	0.476	0.554
WAIT→RUN	SPLL	120, 60, 24	—	0.260	0.310
VLPW→VLPR	SIRC	4, 4, 1	—	10.3	16.2
VLPS→VLPR	SIRC	4, 4, 1	—	10.8	15.7
VLPW→RUN	FIRC (reset value)	48, 48, 24 (reset value)	—	128	143
t_{POR}[3]	FIRC (reset value)	48, 48, 24 (reset value)	—	112	122

1. Typical value is the average of values tested at Temperature=25 °C and V_{DD}=3.3 V.
2. Max value is mean+6×sigma of tested values at the worst case of ambient temperature range and V_{DD} 2.7 V to 5.5 V.
3. After a POR event, the amount of time from the point V_{DD} reaches the reference voltage 2.7 V to execution of the first instruction, across the operating temperature range of the chip.

5.3.1.6 Power consumption

The following table shows the power consumption targets for the device in various mode of operations.

NOTE

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

Table 32. Power consumption operating behaviors

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Units
HSRUN	I_{DD_HSRUN}	PLL	Running CoreMark in Flash in **Compute Operation** mode. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	44.50	46.36	mA
				105 °C	—	51.88	59.46	
		PLL	Running CoreMark in Flash all peripheral clock disabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	50.49	52.35	
				105 °C	—	58.31	65.89	
		PLL	Running CoreMark in Flash, all peripheral clock enabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	60.51	62.37	
				105 °C	—	68.62	76.20	
		PLL	Running While(1) loop in Flash, all peripheral clock disabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	52.74	54.60	
				105 °C	—	60.76	68.34	
		PLL	Running While(1) loop in Flash all peripheral clock enabled. Core@168MHz, bus @84MHz,flash @24MHz VDD=5V	25 °C	—	62.48	64.34	
				105 °C	—	70.75	78.33	
RUN	I_{DD_RUN}	PLL	Running CoreMark in Flash in **Compute Operation** mode. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	29.04	29.67	mA
				105 °C	—	34.82	40.43	
		PLL	Running CoreMark in Flash all peripheral clock disabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	33.29	33.92	
				105 °C	—	39.08	44.69	
		PLL	Running CoreMark in Flash, all peripheral clock enabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	41.00	41.63	
				105 °C	—	47.00	52.61	
		PLL	Running While(1) loop in Flash, all peripheral clock disabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 °C	—	34.59	35.22	
				105 °C	—	40.68	46.29	

Table continues on the next page...

Table 32. Power consumption operating behaviors (continued)

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Units
		PLL	Running While(1) loop in Flash all peripheral clock enabled. Core@120MHz, bus @60MHz,flash @24MHz VDD=5V	25 ℃	—	39.87	40.50	
				105 ℃	—	46.03	51.64	
		IRC48M	Running CoreMark in Flash in **Compute Operation** mode. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	14.02	14.65	
				105 ℃	—	19.76	25.37	
		IRC48M	Running CoreMark in Flash all peripheral clock disabled. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	16.83	17.46	
				105 ℃	—	22.64	28.25	
		IRC48M	Running CoreMark in Flash, all peripheral clock enabled. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	19.70	20.33	
				105 ℃	—	25.59	31.20	
		IRC48M	Running While(1) loop in Flash, all peripheral clock disabled. Core@48MHz, bus @48MHz, flash @24MHz , VDD=5V	25 ℃	—	17.22	17.85	
				105 ℃	—	23.23	28.84	
VLPR	I_{DD_VLPR}	IRC8M	Very Low Power Run Core Mark in Flash in **Compute Operation** mode. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.52	1.63	mA
		IRC8M	Very Low Power Run Core Mark in Flash all peripheral clock disabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.73	1.84	
		IRC8M	Very Low Power Run Core Mark in Flash all peripheral clock enabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.95	2.06	
		IRC8M	Very Low Power Run While(1) loop in Flash all peripheral clock disabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.77	1.88	
		IRC8M	Very Low Power Run While(1) loop in Flash all peripheral clock enabled. Core@4MHz, bus @4MHz, flash @1MHz, VDD=5V	25 ℃	—	1.96	2.07	
		IRC2M	Very Low Power Run While(1) loop in Flash all peripheral clock disabled.	25 ℃	—	1.19	1.30	

Table continues on the next page...

Table 32. Power consumption operating behaviors (continued)

Mode	Symbol	Clock Configuration	Description	Temperature	Min	Typ	Max[1]	Units
			Core@2MHz, bus @2MHz, flash @1MHz, VDD=5V					
		IRC2M	Very Low Power Run While(1) loop in Flash all peripheral clock enabled. Core@2MHz, bus @2MHz, flash @1MHz, VDD=5V	25 °C	—	1.28	1.39	
WAIT	I_{DD_WAIT}	PLL	core disabled, system@120MHz, bus @60MHz, flash disabled (**flash doze enabled**), VDD=5 V, all peripheral clocks disabled	25 °C	—	14.13	14.78	mA
		IRC48M	core disabled, system@48 MHz, bus @48MHz, flash disabled (**flash doze enabled**), VDD=5 V, all peripheral clocks disabled	25 °C	—	8.50	9.15	
VLPW	I_{DD_VLPW}	IRC8M	Very Low Power Wait current, core disabled system@4MHz, bus@4Mhz and flash@1MHz, all peripheral clocks disabled, VDD=5V	25 °C	—	0.84	0.94	mA
		IRC2M	Very Low Power Wait current, core disabled system@2MHz, bus@2Mhz and flash@1MHz, all peripheral clocks disabled, VDD=5V	25 °C	—	1.08	1.18	
STOP	I_{DD_STOP}	-	Stop mode current, VDD=5V, bias disabled [2]	25 °C and blew	—	175	484	µA
				50 °C	—	438	1014	
				85 °C	—	1433	2864	
				105 °C	—	2860	5263	
STOP	I_{DD_STOP}	-	Stop mode current, VDD=5V, bias enabled [2]	25 °C and blew	—	92	299	µA
				50 °C	—	211	530	
				85 °C	—	671	1397	
				105 °C	—	1287	2502	
VLPS	I_{DD_VLPS}	-	Very Low Power Stop current, VDD=5V, bias disabled [2]	25 °C and blew	—	175	483	µA
				50 °C	—	424	998	
				85 °C	—	1367	2792	
				105 °C	—	2864	5258	
VLPS	I_{DD_VLPS}	-	Very Low Power Stop current, VDD=5V, bias enabled [2]	25 °C and blew	—	91	298	µA
				50 °C	—	208	525	
				85 °C	—	656	1378	
				105 °C	—	1305	2514	

1. These values are based on characterization but not covered by test limits in production.
2. PMC_REGSC[CLKBIASDIS] is the control bit to enable or disable bias under STOP/VLPS mode.

NOTE

CoreMark benchmark compiled using IAR 7.40 with optimization level high, optimized for balanced.

5.3.1.6.1 Low power mode peripheral current adder — typical value

Symbol	Description	Typical
I_{LPTMR}	LPTMR peripheral adder measured by placing the device in VLPS mode with LPTMR enabled using LPO. Includes LPO power consumption.	366 nA
I_{CMP}	CMP peripheral adder measured by placing the device in VLPS mode with CMP enabled using the 8-bit DAC and a single external input for compare. 8-bit DAC enabled with half VDDA voltage, low speed mode. Includes 8-bit DAC power consumption.	16 µA
I_{RTC}	RTC peripheral adder measured by placing the device in VLPS mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC counter enabled. Includes EXTAL32 (32 kHz external crystal) power consumption.	312 nA
I_{LPUART}	LPUART peripheral adder measured by placing the device in VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. (SIRC 8 MHz)	79 µA
I_{FTM}	FTM peripheral adder measured by placing the device in VLPW mode with selected clock source, outputting the edge aligned PWM of 100 Hz frequency.	45 µA
I_{ADC}	ADC peripheral adder combining the measured values at VDD and VDDA by placing the device in VLPS mode. ADC is configured for low power mode using SIRC clock source, 8-bit resolution and continuous conversions.	484 µA
I_{LPI2C}	LPI2C peripheral adder measured by placing the device in VLPS mode with selected clock source sending START and Slave address, waiting for RX data. Includes the DMA power consumption.	179 µA
I_{LPIT}	LPIT peripheral adder measured by placing the device in VLPS mode with internal SIRC 8 MHz enabled in Stop mode. Includes selected clock source power consumption.	18 µA
I_{LPSPI}	LPSPI peripheral adder measured by placing the device in VLPS mode with selected clock source, output data on SOUT pin with SCK 500 kbit/s. Includes the DMA power consumption.	565 µA

5.3.1.6.2 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- SCG in SOSC for both Run and VLPR modes
- No GPIOs toggled

- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFE

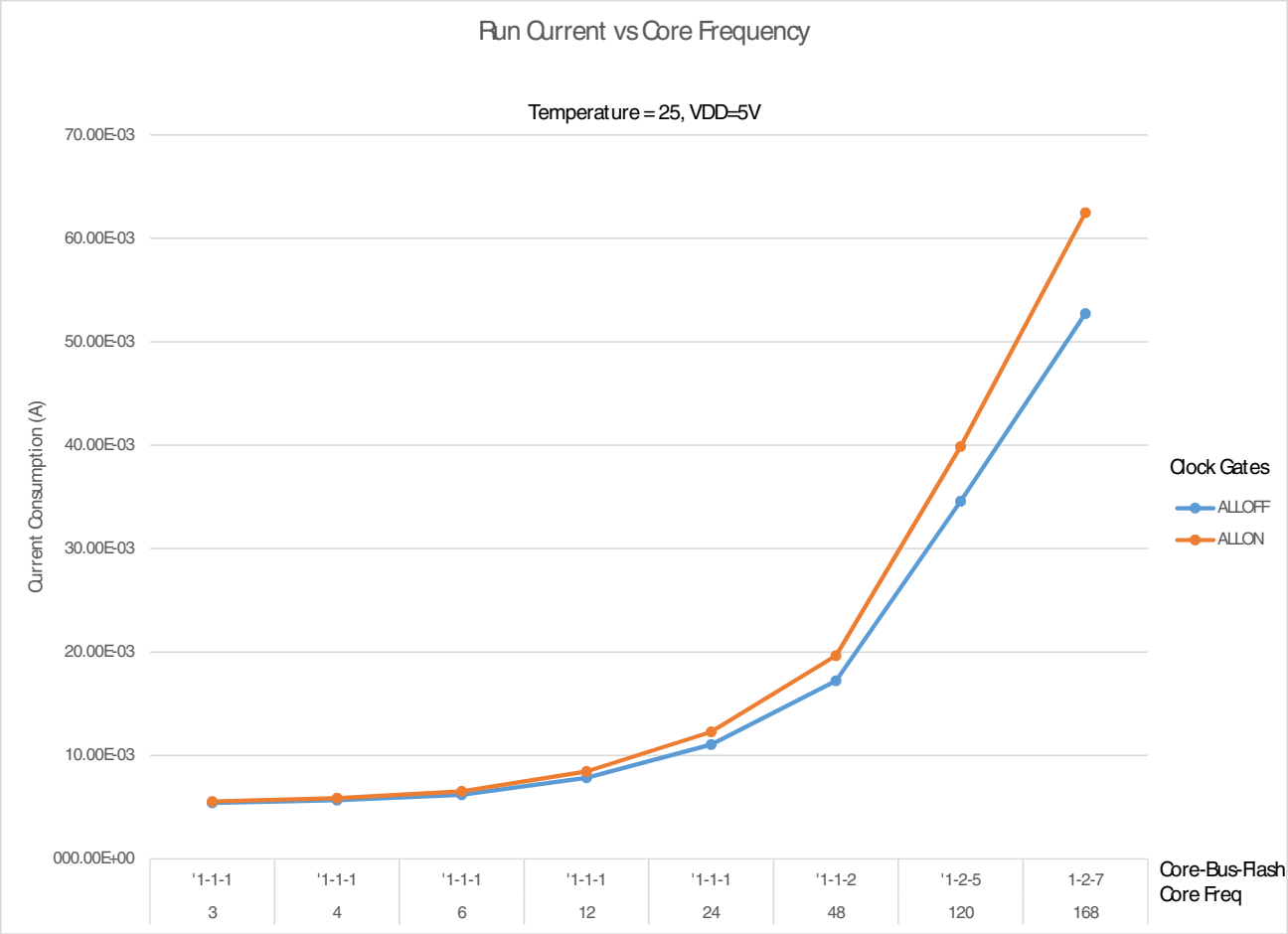


Figure 14. Run mode supply current vs. core frequency

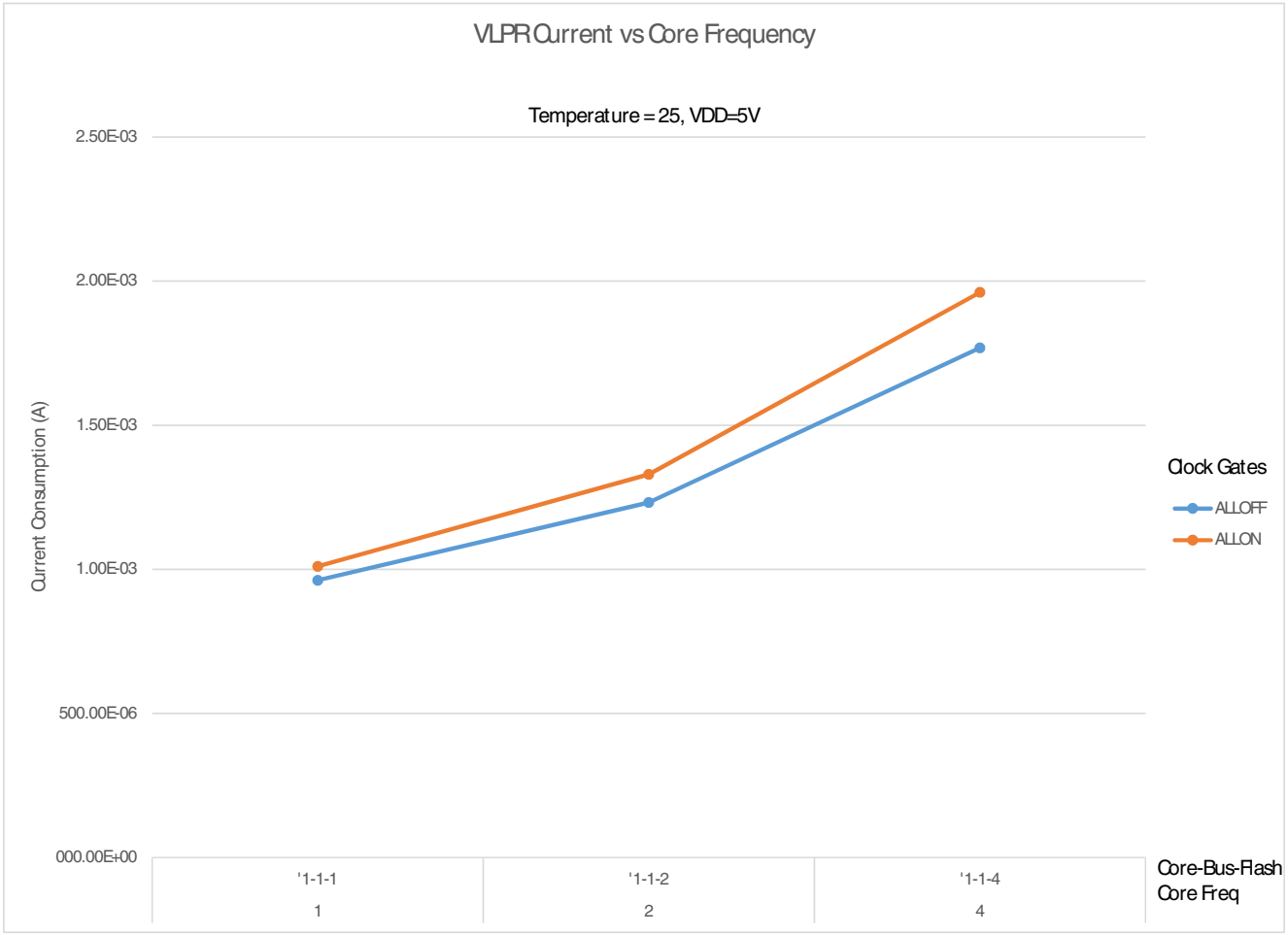


Figure 15. VLPR mode supply current vs. core frequency

5.3.1.7 EMC performance

Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components, and MCU software operation play a significant role in the EMC performance. The system designer can consult the following applications notes, available on http://www.nxp.com for advice and guidance specifically targeted at optimizing EMC performance.

- AN2321: Designing for Board Level Electromagnetic Compatibility
- AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers
- AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers

- AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications
- AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems

5.3.1.7.1 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5.3.1.7.2 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions.

1. Go to http://www.nxp.com.
2. Perform a keyword search for “EMC design”.
3. Select the "Documents" category and find the application notes.

5.3.1.8 Capacitance attributes

Table 33. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External Oscillator electrical specifications for EXTAL/XTAL pins.

5.3.2 Switching specifications

5.3.2.1 Device clock specifications

Table 34. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed RUN mode					
f_{SYS}	System and core clock	—	168	MHz	
f_{BUS}	Bus clock	—	84	MHz	

Table continues on the next page...

Table 34. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{FLASH}	Flash clock	—	25	MHz	
Normal RUN mode					
f_{SYS}	System and core clock	—	120	MHz	
f_{BUS}	Bus clock	—	60	MHz	
f_{FLASH}	Flash clock	—	25	MHz	
f_{LPTMR}	LPTMR clock	—	50	MHz	
VLPR / VLPW mode[1]					
f_{SYS}	System and core clock	—	4	MHz	
f_{BUS}	Bus clock	—	4	MHz	
f_{FLASH}	Flash clock	—	1	MHz	
f_{ERCLK}	External reference clock	—	16	MHz	
f_{LPTMR}	LPTMR clock	—	13	MHz	
$f_{FlexCAN}$	FlexCAN clock	—	4	MHz	

1. The frequency limitations in VLPR / VLPW mode here override any frequency specification listed in the timing specification for any other module.

5.3.2.2 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

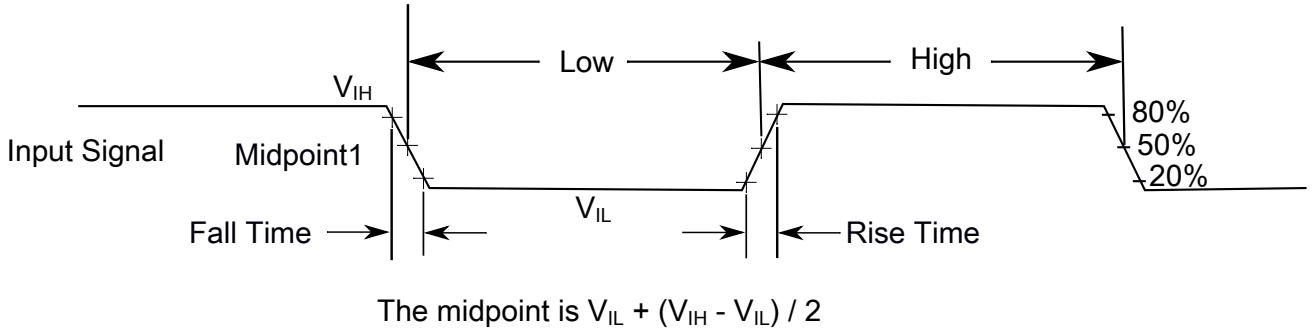


Figure 16. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Normal drive strength

5.3.2.3 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 35. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	4

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins have a passive filter enabled on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.

5.3.2.4 AC specifications at 3.3 V range

Table 36. Functional pad AC specifications

Characteristic	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage	Vdd [1]	2.7		4	V

1. Max power supply ramp rate is 500 V/ms.

Name	Prop Delay (ns) [1]	Rise/Fall Edge (ns) [2]		Drive Load (pF)
	Max	Min	Max	
Normal drive I/O pad	17.5	5	17	25
	28	9	32	50
High drive I/O pad	19	5	17	25
	26	9	33	50
CMOS Input [3]	4	1.2	3	0.5

1. Propagation delay measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

NOTE

All measurements were taken accounting for 150 mV drop across VDD and VSS.

5.3.2.5 AC specifications at 5 V range

Table 37. Functional pad AC specifications

Characteristic	Symbol	Min	Typ	Max	Unit
I/O Supply Voltage	Vdd [1]	4		5.5	V

1. Max power supply ramp rate is 500 V/ms.

Name	Prop Delay (ns) [1]	Rise/Fall Edge (ns) [2]		Drive Load (pF)
	Max	Min	Max	
Normal drive I/O pad	12	3.6	10	25
	18	8	17	50
High drive I/O pad	13	3.6	10	25
	19	8	19	50
CMOS Input [3]	3	1.2	2.8	0.5

1. As measured from 50% of core side input to 50% of the output.
2. Edges measured using 20% and 80% of the VDD supply.
3. Input slope = 2 ns.

NOTE

All measurements were taken accounting for 150 mV drop across VDD and VSS.

5.3.3 Thermal specifications

5.3.3.1 Thermal operating requirements

Table 38. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed maximum T_J. The simplest method to determine T_J is: $T_J = T_A + R_{\Theta JA} \times$ chip power dissipation.

5.3.3.2 Thermal attributes

5.3.3.2.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

5.3.3.2.2 Thermal characteristics for the 64-pin LQFP package

Table 39. Thermal characteristics for the 64-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	60	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	42	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	49	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	36	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	24	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	12	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	Ψ_{JT}	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.3 Thermal characteristics for the 100-pin LQFP package

Table 40. Thermal characteristics for the 100-pin LQFP package

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	57	°C/W

Table continues on the next page...

Table 40. Thermal characteristics for the 100-pin LQFP package (continued)

Rating	Conditions	Symbol	Value	Unit
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	44	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	47	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	38	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	30	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	14	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	ψ_{JT}	2	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

5.3.3.2.4 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

5.4 Peripheral operating requirements and behaviors

5.4.1 System modules

There are no specifications necessary for the device's system modules.

5.4.2 Clock interface modules

5.4.2.1 Oscillator electrical specifications

5.4.2.1.1 External Oscillator electrical specifications

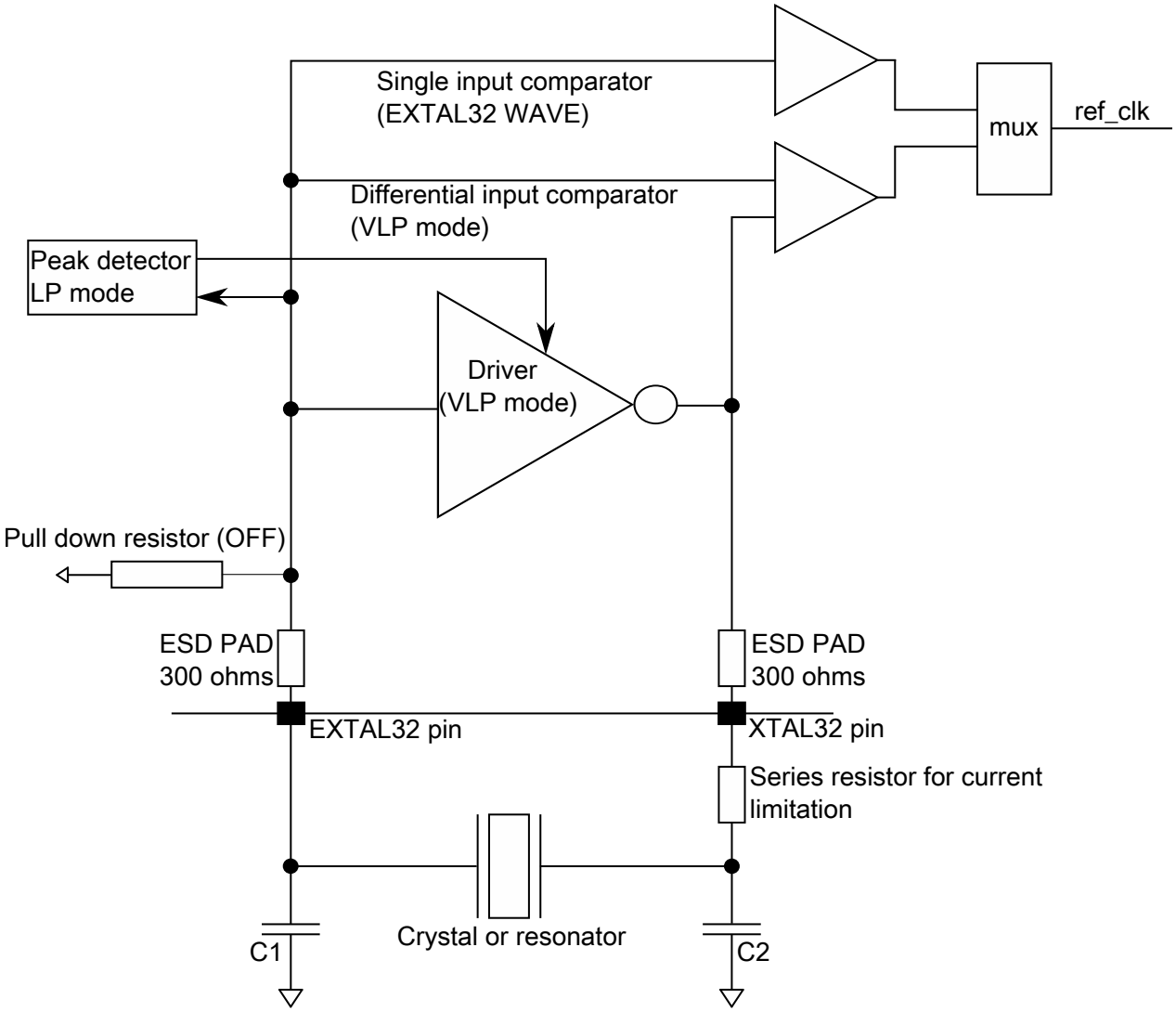
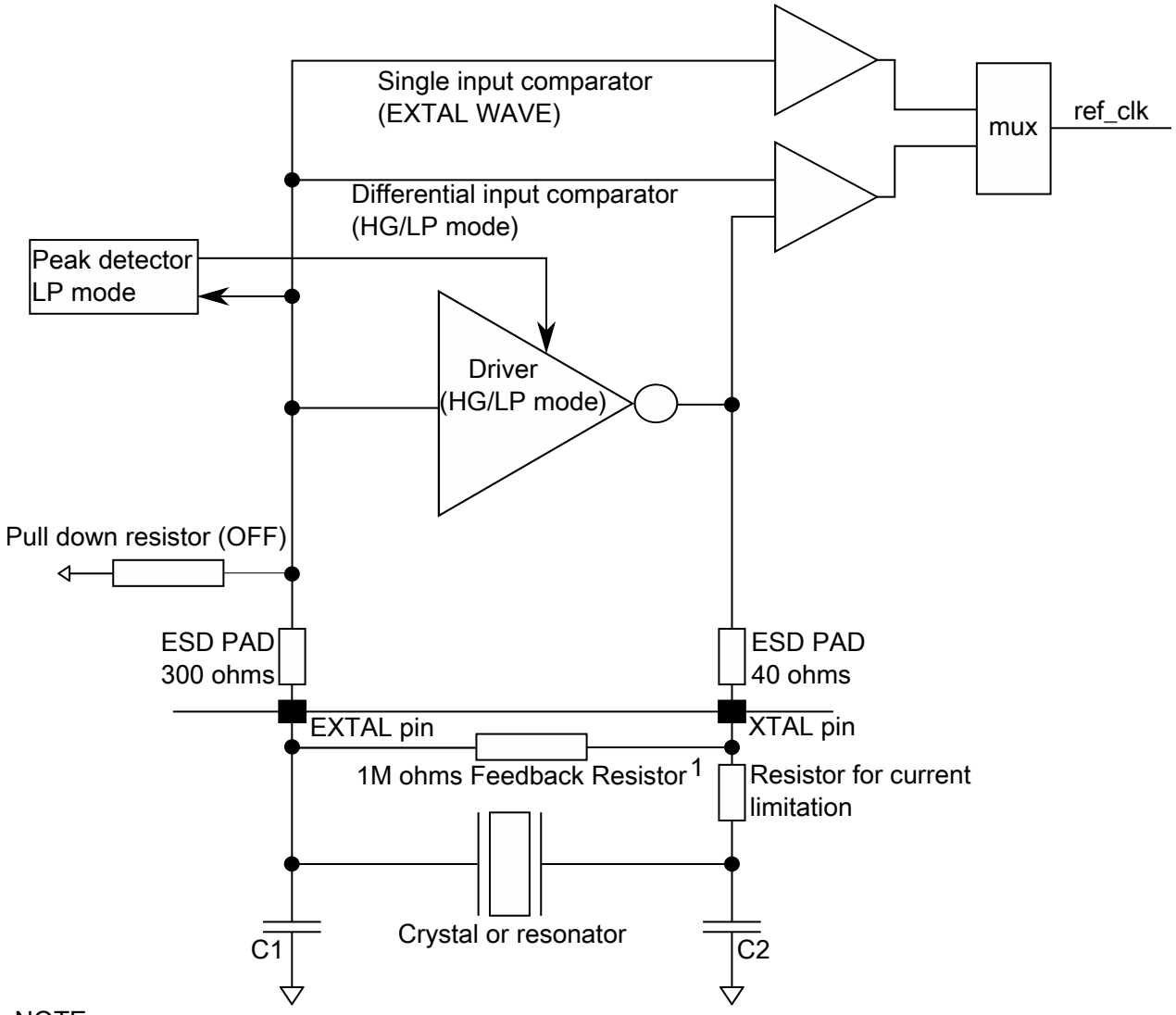


Figure 17. Oscillator connections scheme (OSC32)



NOTE:

1. 1M Feedback resistor is needed only for HG mode.

Figure 18. Oscillator connections scheme (OSC)

NOTE

Data values in the following "External Oscillator electrical specifications" tables are from simulation.

Table 41. External Oscillator electrical specifications (OSC32)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	—	5.5	V	
I_{DDOSC}	Supply current	—	25	—	µA	1
g_{mXOSC}	Oscillator transconductance	6	—	9	µA/V	
V_{EXTAL}	EXTAL32 input voltage — external clock mode	0	—	3.6	V	

Table continues on the next page...

Table 41. External Oscillator electrical specifications (OSC32) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{IH}	Input high voltage — EXTAL32 pin in external clock mode	0.7 x V_{DD}	—	V_{DD}	V	
V_{IL}	Input low voltage — EXTAL32 pin in external clock mode	V_{SS}	—	0.35 x V_{DD}	V	
C_1	EXTAL32 load capacitance	—	—	—		2
C_2	XTAL32 load capacitance	—	—	—		2
R_F	Feedback resistor	—	—	—	MΩ	
R_S	Series resistor	—	—	—	MΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)	—	0.6	—	V	3

1. Measured at V_{DD} = 5 V, Temperature = 25 °C. The current consumption is according to the crystal or resonator, loading capacitance.
2. C1 and C2 must be provided by external capacitors and their load capacitance depends on the crystal or resonator manufacturers' recommendation. Please check the crystal datasheet for the recommended values.
3. The EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

Table 42. External Oscillator electrical specifications (OSC)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	—	5.5	V	
I_{DDOSC}	Supply current — low-gain mode (low-power mode) (HGO=0)					1
	4 MHz	—	200	—	µA	
	8 MHz	—	300	—	µA	
	16 MHz	—	1.2	—	mA	
	24 MHz	—	1.6	—	mA	
	32 MHz	—	2	—	mA	
	40 MHz	—	2.6	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	4 MHz	—	1	—	mA	
	8 MHz	—	1.2	—	mA	
	16 MHz	—	3.5	—	mA	
	24 MHz	—	5	—	mA	
	32 MHz	—	5.5	—	mA	
	40 MHz	—	6	—	mA	
g_{mXOSC}	Fast external crystal oscillator transconductance					
	32 kHz, Low Frequency Range, High Gain (32 kHz)	15	—	45	µA / V	
	High Frequency Range 1 (4-8 MHz)	2.2	—	9.7	mA / V	
	High Frequency Range 2 (8-40 MHz)	16		37	mA / V	
V_{EXTAL}	EXTAL input voltage — external clock mode	0	—	V_{DD}	V	

Table continues on the next page...

Table 42. External Oscillator electrical specifications (OSC) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 x V_{DD}	—	V_{DD}	V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	0.35 x V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		2
C_2	XTAL load capacitance	—	—	—		2
R_F	Feedback resistor					3
	Low-frequency, high-gain mode (32 kHz)	—	10	—	MΩ	
	High-frequency, low-gain mode (low-power mode) (4-8 MHz, 8-40 MHz)	—	—	—	MΩ	
	High-frequency, high-gain mode (4-8 MHz, 8-40 MHz)	—	1	—	MΩ	
R_S	Series resistor					
	Low-frequency, high-gain mode (32 kHz)	—	200	—		
	High-frequency, low-gain mode (low-power mode) (4-8 MHz, 8-40 MHz)	—	0	—	kΩ	
	High-frequency, high-gain mode (4-8 MHz, 8-40 MHz)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					4
	Low-frequency, high-gain mode	—	3.3	—	V	
	High-frequency, low-gain mode	—	1.0	—	V	
	High-frequency, high-gain mode	—	3.3	—	V	

1. Measured at V_{DD} = 5 V, Temperature = 25 °C
2. C1 and C2 must be provided by external capacitors and their load capacitance depends on the crystal or resonator manufacturers' recommendation. Please check the crystal datasheet for the recommended values.
3. When low power mode is selected, R_F is integrated and must not be attached externally.
4. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

5.4.2.1.2 External Oscillator frequency specifications

Table 43. External Oscillator frequency specifications (OSC32)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode	30	—	40	kHz	
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	2000	—	ms	1

1. The start-up measured after 4096 cycles. Proper PC board layout procedures must be followed to achieve specifications.

Table 44. External Oscillator frequency specifications (OSC)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — Low Frequency, High Gain Mode	32	—	40	kHz	
f_{osc_me}	Oscillator crystal or resonator frequency — Medium Frequency	1	—	8	MHz	
f_{osc_hi}	Oscillator crystal or resonator frequency — High Frequency	8	—	32		
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz Low Frequency, High-Gain Mode	—	500	—	ms	1
	Crystal startup time — 8 MHz High Frequency, Low-Power Mode	—	1.5	—		
	Crystal startup time — 8 MHz High Frequency, High-Gain Mode	—	2.5	—		
	Crystal startup time — 40 MHz High Frequency, Low-Power Mode	—	2	—		
	Crystal startup time — 40 MHz High Frequency, High-Gain Mode	—	2.5	—		

1. The start-up measured after 4096 cycles. Proper PC board layout procedures must be followed to achieve specifications.

5.4.2.2 System Clock Generation (SCG) specifications

5.4.2.2.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 45. Fast internal RC Oscillator electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	Fast internal reference frequency Trim range = 00 range = 01 (Note: 52/56 MHz are not trimmed) range = 10 (Note: 52/56 MHz are not trimmed) Trim range = 11	—	48 52 56 60	—	MHz
I_{VDD}	Supply current	—	400	500	µA
$F_{Untrimmed}$	IRC frequency (untrimmed)	F_{IRC}× (1-0.3)	—	F_{IRC}× (1+0.3)	MHz
ΔF_{OL}	Open loop total deviation of IRC frequency over voltage and temperature[1]				
	Regulator enable	—	±0.5	±1	$\%F_{FIRC}$
$T_{Startup}$	Startup time		—	3	µs[2]
T_{JIT}	Period jitter (RMS)	—	35	150	ps

1. The limit is respected across process, voltage and full temperature range.
2. Startup time is defined as the time between clock enablement and clock availability for system use.

NOTE

Fast internal RC Oscillator is compliant with CAN and LIN standards.

5.4.2.2.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 46. Slow internal RC oscillator (SIRC) electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	Slow internal reference frequency	—	2 8	—	MHz
I_{VDD}	Supply current	—	23	—	µA
$F_{Untrimmed}$	IRC frequency (untrimmed)	—	—	—	MHz
ΔF_{OL}	Open loop total deviation of IRC frequency over voltage and temperature[1]				
	Regulator enable	—	—	±3	$\%F_{SIRC}$
$T_{Startup}$	Startup time	—	6	—	µs[2]

1. The limit is respected across process, voltage and full temperature range.
2. Startup time is defined as the time between clock enablement and clock availability for system use.

5.4.2.2.3 Low Power Oscillator (LPO) electrical specifications

Table 47. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{LPO}	Internal low power oscillator frequency	113	128	139	kHz
I_{LPO}	Current consumption	1	3	7	µA
$T_{startup}$	Startup Time	—	—	20	µs

5.4.2.2.4 PLL electrical specifications

Table 48. PLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{pll_ref}	PLL Reference Frequency Range	8	—	50	MHz
F_{vcoclk_2x}	VCO output frequency	180	—	360	MHz
F_{vcoclk}	PLL output frequency	90	—	180	MHz
F_{vcoclk_90}	PLL output frequency	90	—	180	MHz
I_{pll}	PLL operating current[1]				

Table continues on the next page...

Table 48. PLL electrical specifications (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	VCO @ 150 MHz (F_{pll_ref} = 12 MHz, VDIV multiplier = 25, PRDIV divide = 2)	—	2.8	—	mA
	VCO @ 300 MHz (F_{pll_ref} = 12 MHz, VDIV multiplier = 50, PRDIV divide = 2)	—	3.6	—	mA
J_{cyc_pll}	PLL Period Jitter (RMS)[2]				
	at F_{vco} 180 MHz	—	120	—	ps
	at F_{vco} 360 MHz	—	75	—	ps
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS)[2]				
	at F_{vco} 180 MHz	—	1350	—	ps
	at F_{vco} 360 MHz	—	600	—	ps
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%
T_{pll_lock}	Lock detector detection time[3]	—	—	100×10^{-6} + 1075(1/F_{pll_ref})	s

1. Excludes any oscillator currents that are also consuming power while PLL is in operation.
2. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary
3. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, thisspecification assumes it is already running.

5.4.3 Memories and memory interfaces

5.4.3.1 Flash memory module (FTFE) electrical specifications

This section describes the electrical characteristics of the flash memory module (FTFE).

5.4.3.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 49. NVM program/erase timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{hvpgm8}	Program Phrase high-voltage time	—	7.5	18	µs	
$t_{hversscr}$	Erase Flash Sector high-voltage time	—	13	113	ms	1
$t_{hversblk64k}$	Erase Flash Block high-voltage time for 64 KB	—	52	452	ms	1
$t_{hversblk512k}$	Erase Flash Block high-voltage time for 512 KB	—	416	3616	ms	1

1. Maximum time based on expectations at cycling end-of-life.

5.4.3.1.2 Flash timing specifications — commands

Table 50. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk64k}$	• 64 KB data flash	—	—	0.5	ms	
$t_{rd1blk512k}$	• 512 KB program flash	—	—	1.8	ms	
$t_{rd1sec2k}$	Read 1s Section execution time (2 KB flash)	—	—	75	µs	1
$t_{rd1sec4k}$	Read 1s Section execution time (4 KB flash)	—	—	100	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{rdrsrc}	Read Resource execution time	—	—	40	µs	1
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
	Erase Flash Block execution time					2
$t_{ersblk64k}$	• 64 KB data flash	—	55	475	ms	
$t_{ersblk512k}$	• 512 KB program flash	—	435	3700	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	2.2	ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	1
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	500	4200	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	µs	1
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	500	4200	ms	2
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB EEPROM backup	—	70	—	ms	
$t_{pgmpart64k}$	• 64 KB EEPROM backup	—	71	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	70	—	µs	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.8	1.2	ms	
$t_{setram48k}$	• 48 KB EEPROM backup	—	1.0	1.5	ms	
$t_{setram64k}$	• 64 KB EEPROM backup	—	1.3	1.9	ms	
	Byte-write to FlexRAM execution time:					
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
$t_{eewr8b48k}$	• 48 KB EEPROM backup	—	430	1850	µs	
$t_{eewr8b64k}$	• 64 KB EEPROM backup	—	475	2000	µs	
	16-bit write to FlexRAM execution time:					

Table continues on the next page...

Table 50. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{eewr16b32k}$	• 32 KB EEPROM backup	—	385	1700	µs	
$t_{eewr16b48k}$	• 48 KB EEPROM backup	—	430	1850	µs	
$t_{eewr16b64k}$	• 64 KB EEPROM backup	—	475	2000	µs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	1500	µs	
	32-bit write to FlexRAM execution time:					
$t_{eewr32b32k}$	• 32 KB EEPROM backup	—	630	2000	µs	
$t_{eewr32b48k}$	• 48 KB EEPROM backup	—	720	2125	µs	
$t_{eewr32b64k}$	• 64 KB EEPROM backup	—	810	2250	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

5.4.3.1.3 Flash high voltage current behaviors

Table 51. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

5.4.3.1.4 Reliability specifications

Table 52. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2
Data Flash						
$t_{nvmretd10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
$n_{nvmcycee}$	Cycling endurance for EEPROM backup	20 K	50 K	—	cycles	2

Table continues on the next page...

Table 52. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	140 K	400 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	1.26 M	3.2 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	5 M	12.8 M	—	writes	
$n_{nvmwree2k}$	• EEPROM backup to FlexRAM ratio = 2,048	20 M	50 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.
3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM and the allocated EEPROM backup. Minimum and typical values assume all 16-bit or 32-bit writes to FlexRAM; all 8-bit writes result in 50% less endurance.

5.4.4 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

5.4.5 Analog

5.4.5.1 ADC electrical specifications

5.4.5.1.1 12-bit ADC operating conditions

Table 53. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	2.7	—	5.5	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high		2.5	V_{DDA}	V_{DDA} + 100m	V	3
V_{REFL}	ADC reference voltage low		– 100	0	100	mV	3
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
C_{ADIN}	Input capacitance		—	4	5	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	

Table continues on the next page...

Table 53. 12-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
R_{AS}	Analog source resistance (external)		—	—	5	kΩ	4
f_{ADCK}	ADC conversion clock frequency		2	40	50	MHz	5, 6
C_{rate}	ADC conversion rate	No ADC hardware averaging[7] Continuous conversions enabled, subsequent conversion time	20	—	1200	Ksps	8

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SSA}.
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
5. Clock and compare cycle need to be set according the guidelines in the block guide.
6. ADC conversion will become less reliable above maximum frequency.
7. When using ADC hardware averaging, refer to the device *Reference Manual* to determine the most appropriate setting for AVGS.
8. Max ADC conversion rate of 1200 Ksps is with 10-bit mode

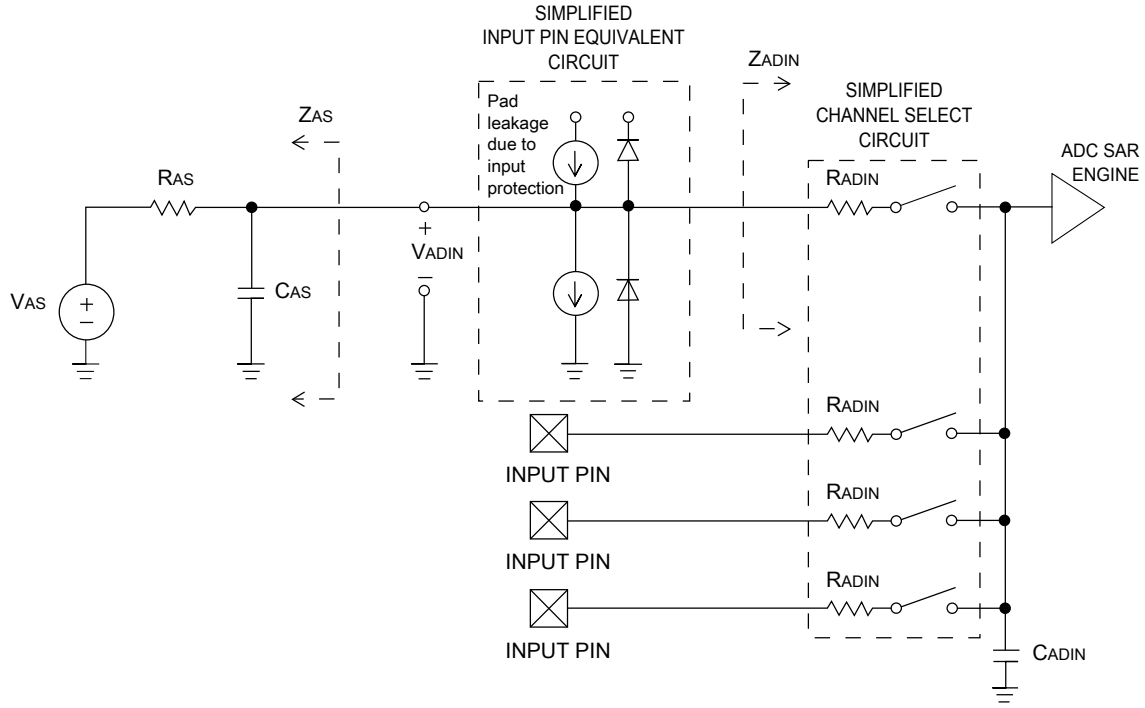


Figure 19. ADC input impedance equivalency diagram

5.4.5.1.2 12-bit ADC electrical characteristics

NOTE

All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

For ADC signals adjacent to VDD/VSS or the XTAL pins some degradation in the ADC performance may be observed.

NOTE

All values guarantee the performance of the ADC for the multiple ADC input channel pins. When using the ADC to monitor the internal analogue parameters, please assume minor degradation.

Table 54. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max. [3]	Unit	Notes
I_{DDA_ADC}	Supply current at 2.7 to 5.5 V		621	658 µA @ 5 V	696	mA	4

Table continues on the next page...

Table 54. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max. [3]	Unit	Notes
	Sample Time		275	—	Refer to the device's *Reference Manual*	ns	
TUE	Total unadjusted error at 2.7 to 5.5 V		—	±4.5	±6.56	LSB[5]	6
DNL	Differential non-linearity at 2.7 to 5.5 V		—	±0.8	±1.07	LSB[5]	6
INL	Integral non-linearity at 2.7 to 5.5 V		—	±1.4	±3.95	LSB[5]	6
E_{FS}	Full-scale error at 2.7 to 5.5 V		—	–2	-3.40	LSB[5]	V_{ADIN} = V_{DDA}[6]
E_{ZS}	Zero-scale error at 2.7 to 5.5 V		—	–2.7	-4.14	LSB[5]	
E_Q	Quantization error at 2.7 to 5.5 V		—	—	±0.5	LSB[5]	
ENOB	Effective number of bits at 2.7 to 5.5 V		—	11.3	—	bits	7
SINAD	Signal-to-noise plus distortion at 2.7 to 5.5 V	See ENOB	—	70	—	dB	SINAD = 6.02 × ENOB + 1.76
E_{IL}	Input leakage error at 2.7 to 5.5 V		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
V_{TEMP_S}	Temperature sensor slope at 2.7 to 5.5 V	Across the full temperature range of the device	1.492	1.564	1.636	mV/°C	8, 9
V_{TEMP25}	Temperatue sensor voltage at 2.7 to 5.5 V	25 °C	730	740.5	751	mV	8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 48 MHz unless otherwise stated.
3. These values are based on characterization but not covered by test limits in production.
4. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
7. Input data is 100 Hz sine wave. ADC conversion clock < 40 MHz.
8. ADC conversion clock < 3 MHz
9. The sensor must be calibrated to gain good accuracy, so as to provide good linearity, see also AN3031 for more detailed application information of the temperature sensor.

5.4.5.2 CMP with 8-bit DAC electrical specifications

Table 55. Comparator with 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ. [1]	Max.	Unit
V_{DD}	Supply voltage	2.7	—	5.5	V
I_{DDHS}	Supply current, High-speed mode[2]				µA
	within ambient temperature range	—	145	200	
I_{DDLS}	Supply current, Low-speed mode[2]				µA
	within ambient temperature range	—	5	10	
V_{AIN}	Analog input voltage	0	0 - V_{DDX}	V_{DDX}	V
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	within ambient temperature range	-25	±1	25	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	within ambient temperature range	-40	±4	40	
t_{DHSB}	Propagation delay, High-speed mode[3]				ns
	within ambient temperature range	—	30	200	
t_{DLSB}	Propagation delay, Low-speed mode[3]				µs
	within ambient temperature range	—	0.5	2	
t_{DHSS}	Propagation delay, High-speed mode[4]				ns
	within ambient temperature range	—	70	400	
t_{DLSS}	Propagation delay, Low-speed mode[4]				µs
	within ambient temperature range	—	1	5	
t_{IDHS}	Initialization delay, High-speed mode [3]				µs
	within ambient temperature range	—	1.5	3	
t_{IDLS}	Initialization delay, Low-speed mode[3]				µs
	within ambient temperature range	—	10	30	
V_{HYST0}	Analog comparator hysteresis, Hyst0 (V_{AIO})				mV
	within ambient temperature range	—	0	—	
V_{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	within ambient temperature range	—	16	53	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	within ambient temperature range	—	11	30	
V_{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	within ambient temperature range	—	32	90	
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	within ambient temperature range	—	22	53	
V_{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV

Table continues on the next page...

Table 55. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ. [1]	Max.	Unit
	within ambient temperature range	—	48	133	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	within ambient temperature range	—	33	80	
I_{DAC8b}	8-bit DAC current adder (enabled)	—	10	16	µA
INL	8-bit DAC integral non-linearity	–0.6	—	0.5	LSB[5]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB

1. Typical values assumed at VDDA = 5.0 V, Temp = 25 °C, unless otherwise stated.
2. Difference at input > 200mV
3. Applied ± (100 mV + Hyst) around switch point
4. Applied ± (30 mV + 2 × Hyst) around switch point
5. 1 LSB = $V_{reference}/256$

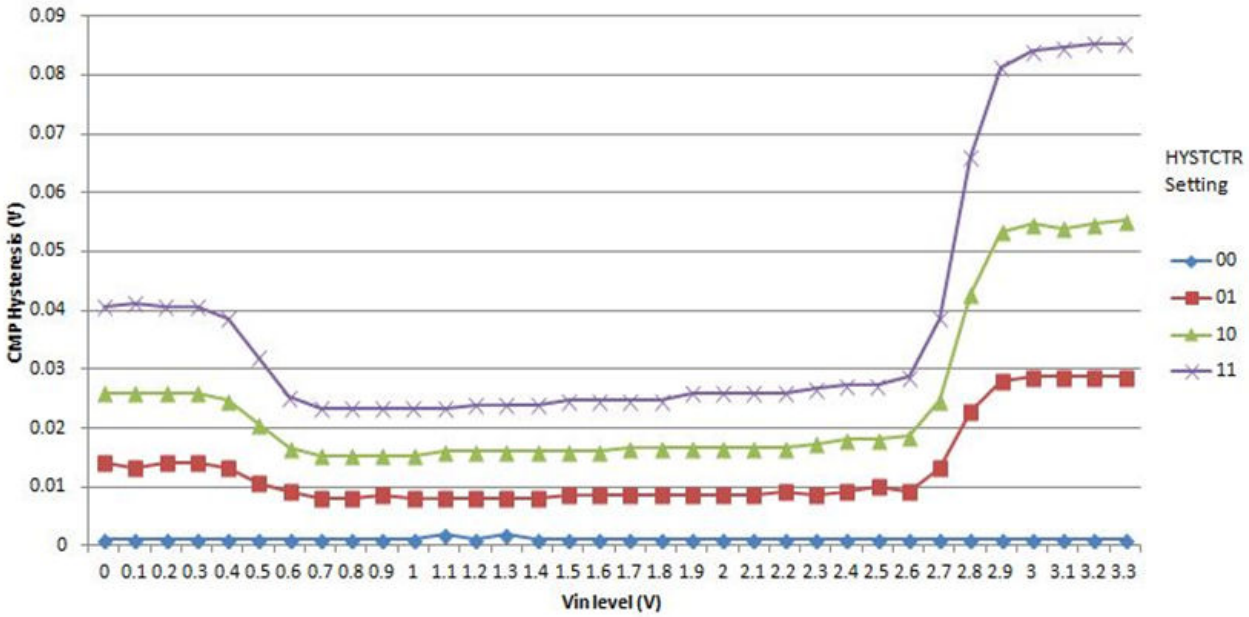


Figure 20. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

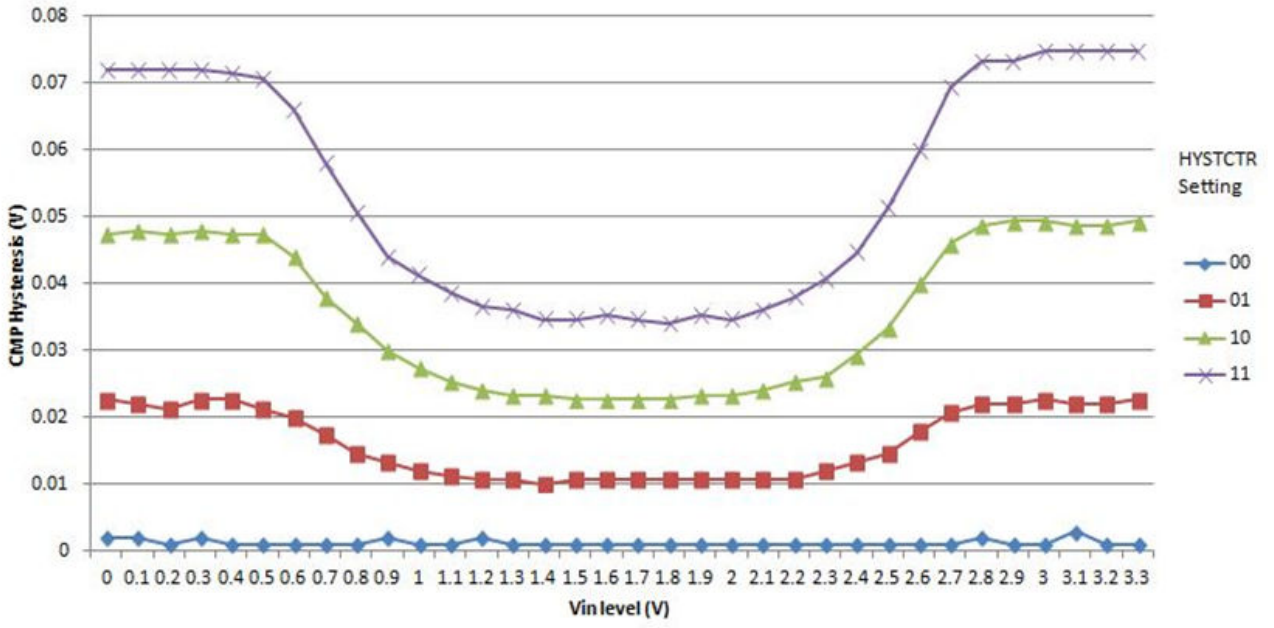


Figure 21. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

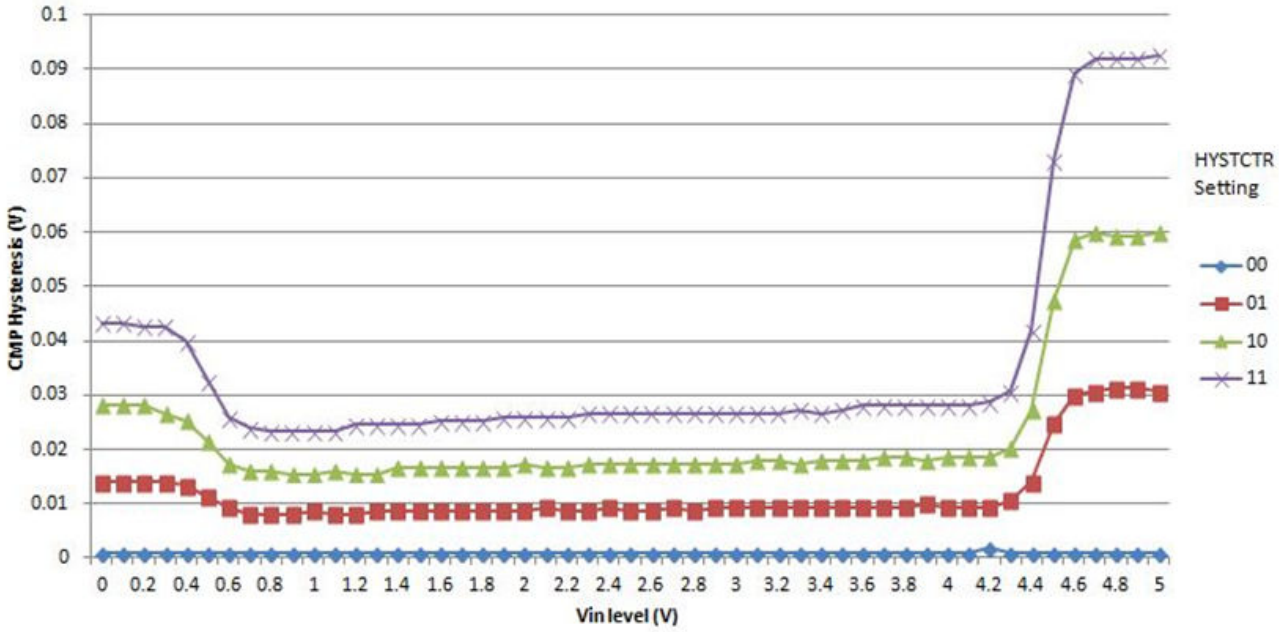


Figure 22. Typical hysteresis vs. Vin level (VDD = 5 V, PMODE = 0)

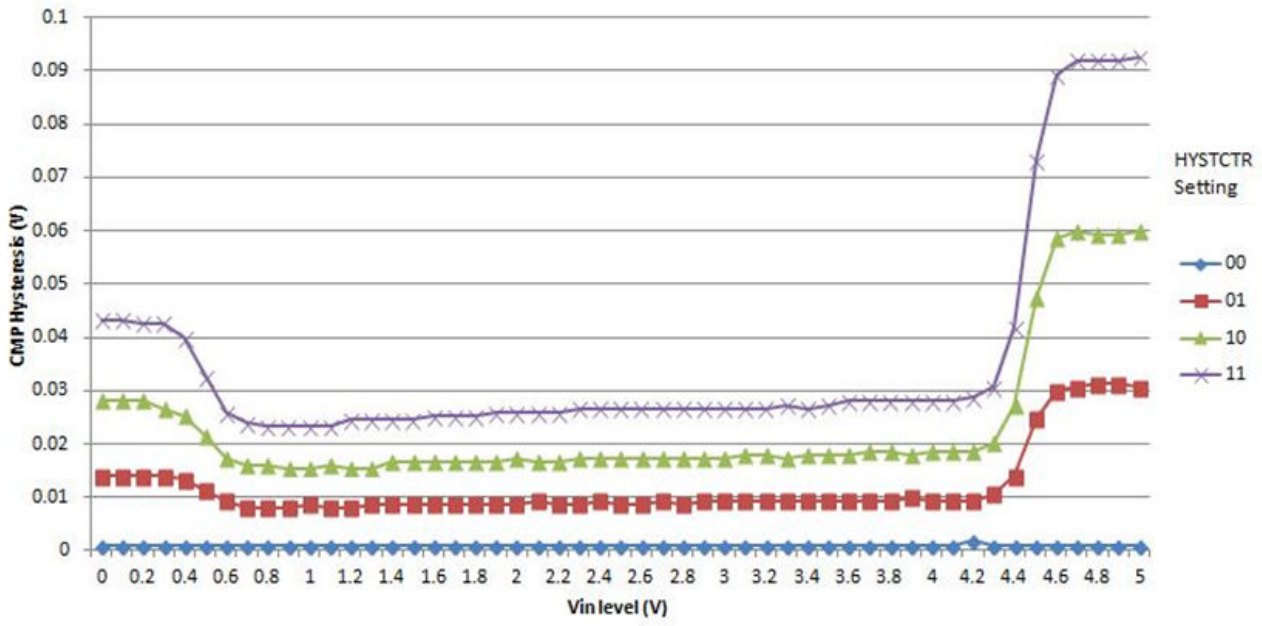


Figure 23. Typical hysteresis vs. Vin level (VDD = 5 V, PMODE = 1)

5.4.5.3 12-bit DAC electrical characteristics

5.4.5.3.1 12-bit DAC operating requirements

Table 56. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	2.7	5.5	V	
V_{DACR}	Reference voltage	2.7	5.5	V	1
C_L	Output load capacitance	20	100	pF	2
I_L	Output load current	—	1	mA	3

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance can improve the bandwidth performance of the DAC.
3. Output range is from ground + 0.2 to V_{DACR} - 0.2

5.4.5.3.2 12-bit DAC operating behaviors

Table 57. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	330	µA	
I_{DDA_DACHP}	Supply current — high-power mode	—	—	1200	µA	

Table continues on the next page...

Table 57. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode	—	—	5	µs	1
$t_{CCDACHP}$	Code-to-code settling time (0xBF8 to 0xC08) — high-power mode	—	0.7	—	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-power mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-power mode, no load, DAC set to 0xFFF	V_{DACR} – 100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high-power mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	3
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	4
E_G	Gain error	—	±0.1	±0.6	%FSR	4
PSRR	Power supply rejection ratio					
	High-power mode, code set to 3FF or BFF		68		dB	5
	Low-power mode, code set to 3FF or BFF		60			
T_{CO}	Temperature coefficient offset voltage	—	5	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	1 0.05	1.5 0.12	— —	V/µs	

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V
4. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} – 100 mV
5. DAC reference to VREFH (DACREF_1)
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

5.4.6 Communication interfaces

5.4.6.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

5.4.6.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

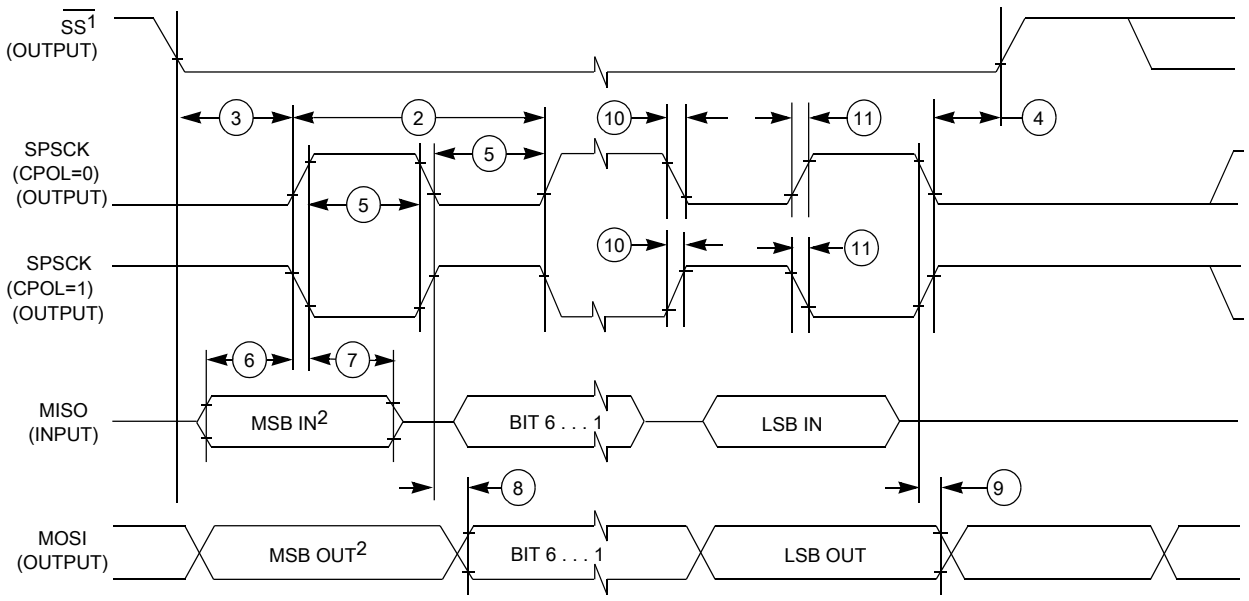
Table 58. LPSPI master mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} = LPSPI peripheral clock
2. $t_{periph} = 1/f_{periph}$

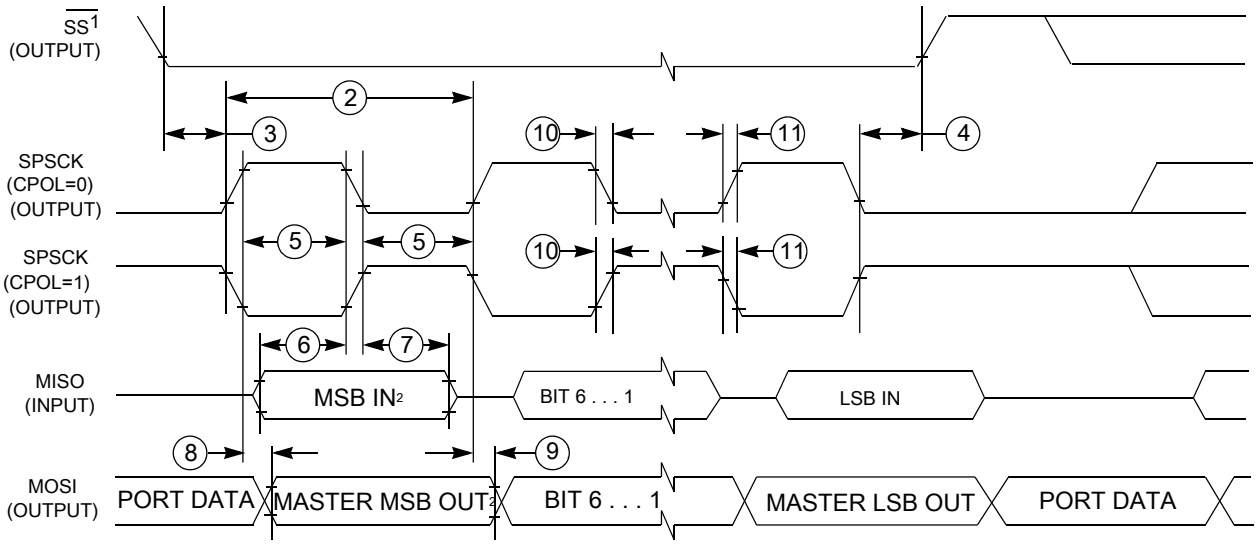
NOTE

High drive pin should be used for fast bit rate.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 24. LPSPI master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 25. LPSPI master mode timing (CPHA = 1)

Table 59. LPSPI slave mode timing

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—

Table continues on the next page...

Table 59. LPSPI slave mode timing (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} = LPSPI peripheral clock
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

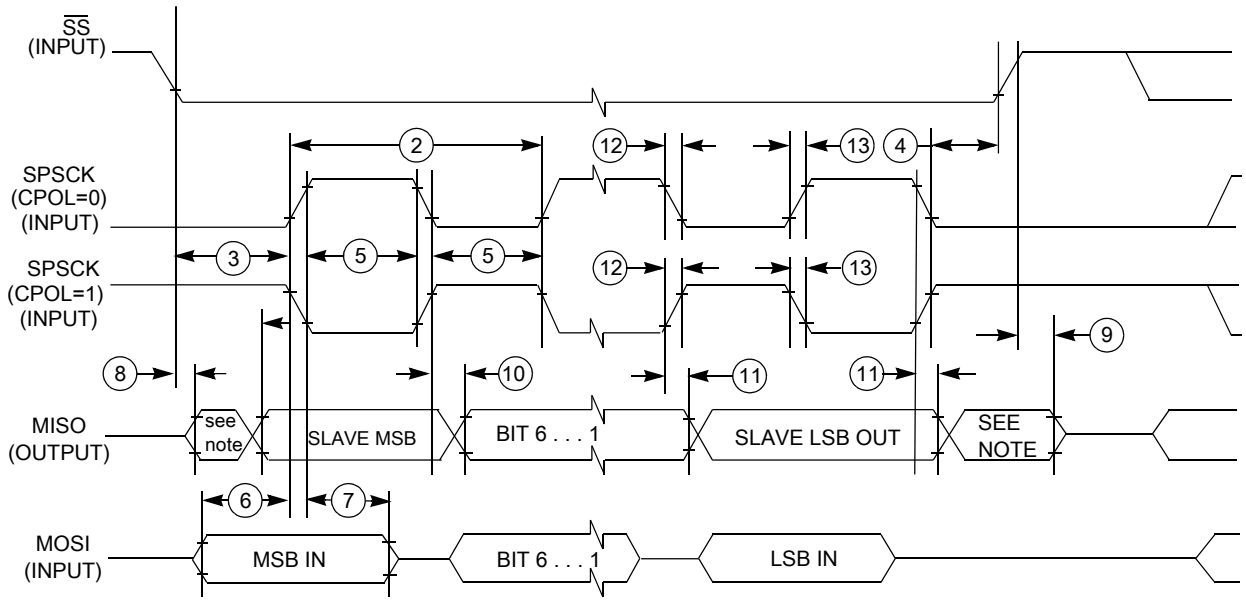


Figure 26. LPSPI slave mode timing (CPHA = 0)

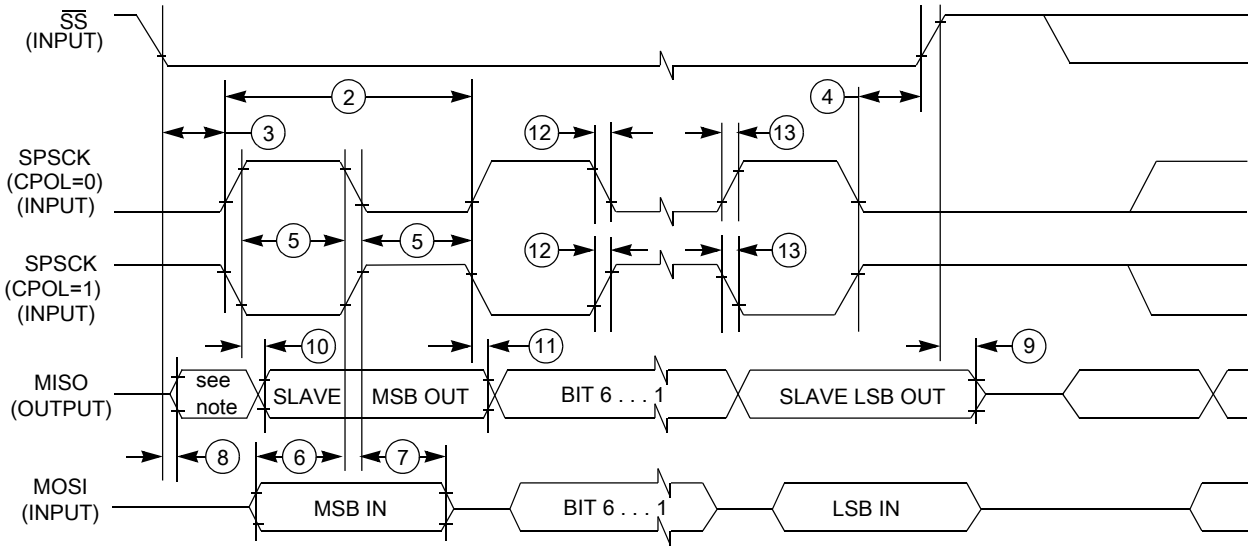


Figure 27. LPSPI slave mode timing (CPHA = 1)

5.4.6.3 LPI²C

Table 60. LPI²C specifications

Symbol	Description		Min.	Max.	Unit	Notes
f_{SCL}	SCL clock frequency	Standard mode (Sm)	0	100	kHz	1, 2, 3
		Fast mode (Fm)	0	400		
		Fast mode Plus (Fm+)	0	1000		
		Ultra Fast mode (UFm)	0	5000		
		High speed mode (Hs-mode)	0	3400		

1. Hs-mode is only supported in slave mode.
2. The maximum SCL clock frequency in Fast mode with maximum bus loading (400pF) can only be achieved with appropriate pull-up devices on the bus when using the high or normal drive pins across the full voltage range . The maximum SCL clock frequency in Fast mode Plus can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. The maximum SCL clock frequency in Ultra Fast mode can support maximum bus loading (400pF) when using the high drive pins. The maximum SCL clock frequency for slave in High speed mode can support maximum bus loading (400pF) with appropriate pull-up devices when using the high drive pins. For more information on the required pull-up devices, see I²C Bus Specification.
3. See General switching specifications

5.4.7 Debug modules

5.4.7.1 SWD electricals

Table 61. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
V_{DDA}	Operating voltage	2.7	5.5	V
S1	SWD_CLK frequency of operation	0	25	MHz
S2	SWD_CLK cycle period	1/S1	—	ns
S3	SWD_CLK clock pulse width	15	—	ns
S4	SWD_CLK rise and fall times	—	3	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	8	—	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	1.4	—	ns
S11	SWD_CLK high to SWD_DIO data valid	—	25	ns
S12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

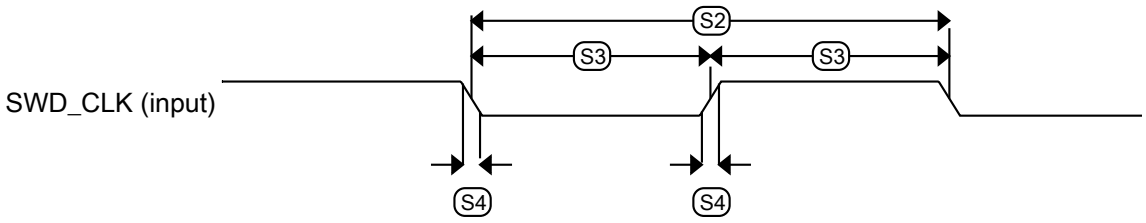


Figure 28. Serial wire clock input timing

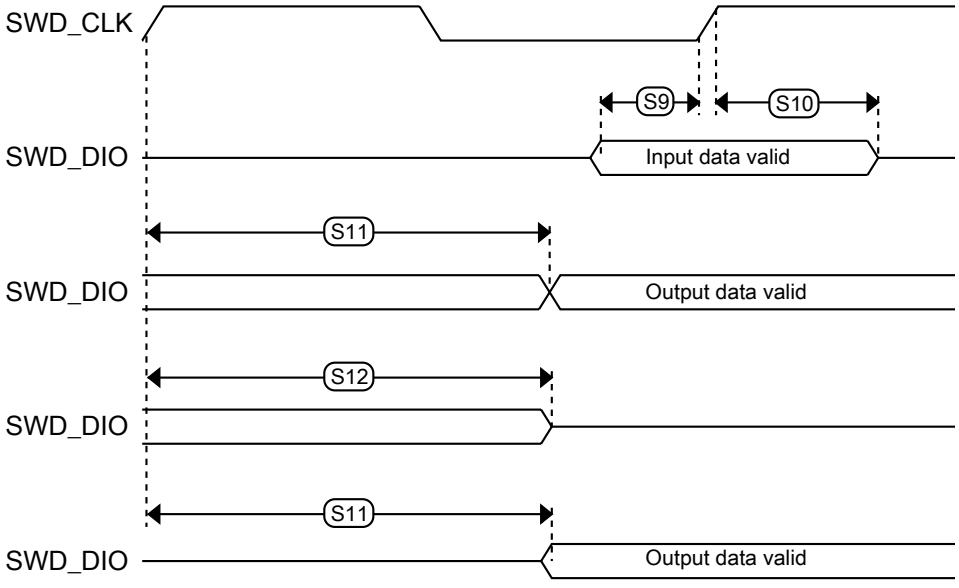


Figure 29. Serial wire data timing

5.4.7.2 JTAG electricals

Table 62. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	20	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			ns
	Boundary Scan	50	—	
	JTAG and CJTAG	25	—	
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	TRST assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

Table 63. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
V_{DDA}	Operating voltage	2.7	5.5	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	15	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			ns
	Boundary Scan	50	—	
	JTAG and CJTAG	33	—	
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	—	27	ns
J8	TCLK low to boundary scan output high-Z	—	27	ns

Table continues on the next page...

Table 63. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	—	26.2	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	TRST setup time (negation) to TCLK high	8	—	ns

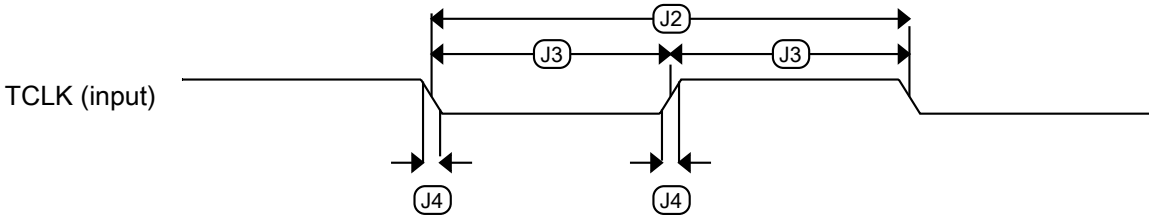


Figure 30. Test clock input timing

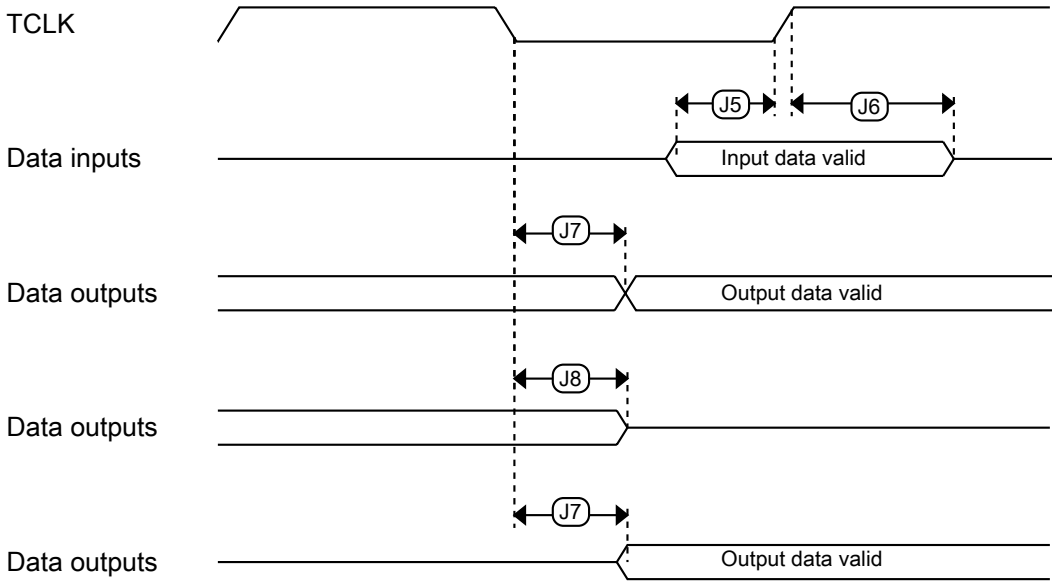


Figure 31. Boundary scan (JTAG) timing

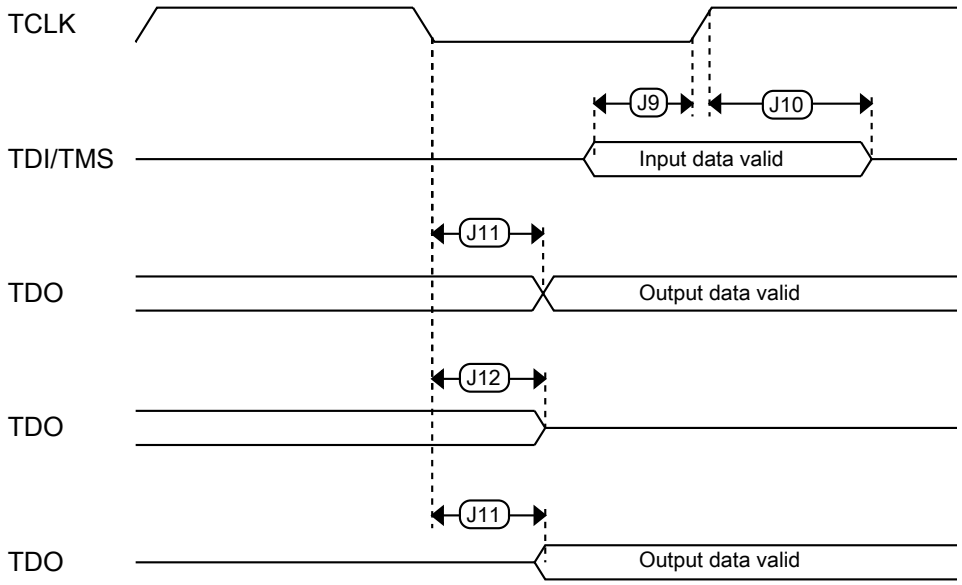


Figure 32. Test Access Port timing

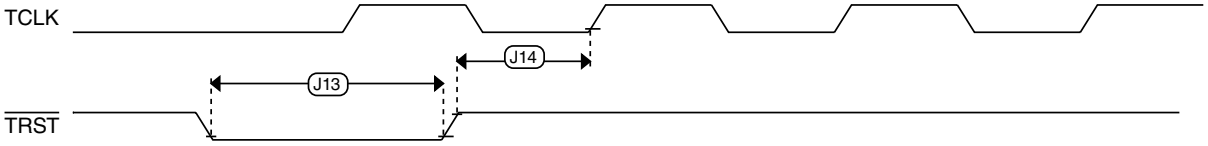


Figure 33. $\overline{\text{TRST}}$ timing

6 Design considerations

6.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

6.1.1 Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground. Consider to add ferrite bead or inductor to some sensitive lines.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP packages; and solder the exposed pad (EP) to ground directly under QFN packages.

6.1.2 Power delivery system

Consider the following items in the power delivery system:

- Use a plane for ground.
- Use a plane for MCU VDD supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Always route the power net as star topology, and make each power trace loop as minimum as possible.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10 μF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDD/VSS pair, including VDDA/VSSA and VREFH/VREFL.
- The minimum bypass requirement is to place 0.1 μF capacitors positioned as near as possible to the package supply pins.

6.1.3 Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be RAS max if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.

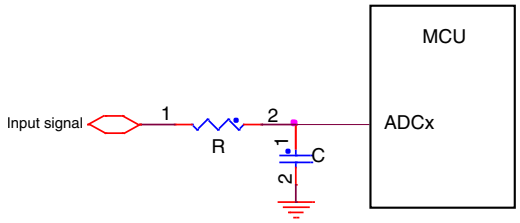


Figure 34. RC circuit for ADC input

High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. Since the ADC pins do not have diodes to VDD, external clamp diodes must be included to protect against transient over-voltages.

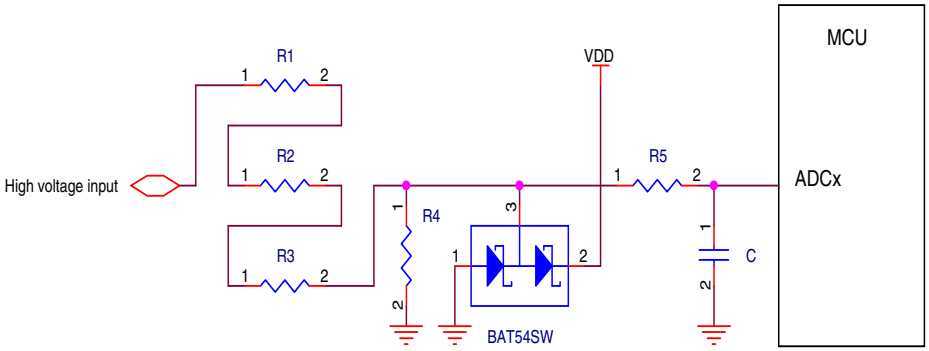


Figure 35. High voltage measurement with an ADC input

NOTE

For more details of ADC related usage, refer to AN5250: How to Increase the Analog-to-Digital Converter Accuracy in an Application.

6.1.4 Digital design

Ensure that all I/O pins cannot get pulled above VDD (Max I/O is VDD+0.3V).

CAUTION

Do not provide power to I/O pins prior to VDD, especially the RESET_b pin.

- RESET_b pin

The RESET_b pin is a pseudo open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

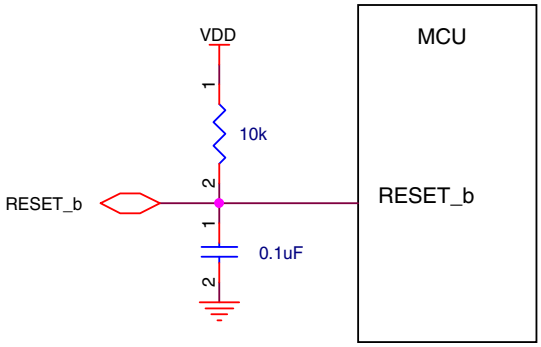


Figure 36. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. The supervisor chip must have an active high, open-drain output.

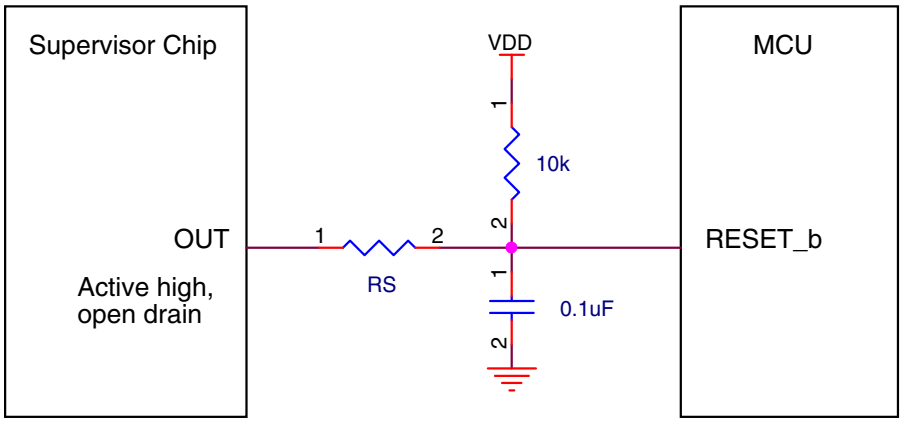


Figure 37. Reset signal connection to external reset chip

- NMI pin

Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

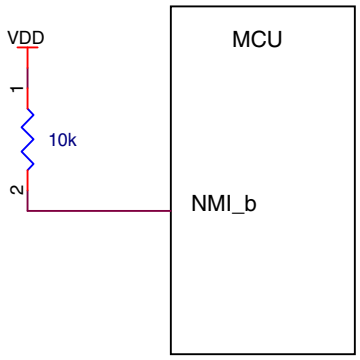


Figure 38. NMI pin biasing

- Debug interface

  This MCU uses the standard ARM SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

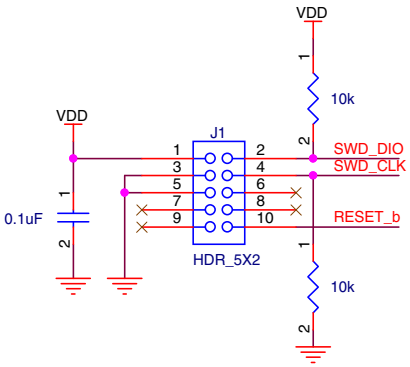


Figure 39. SWD debug interface

- Unused pin

Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

6.1.5 Crystal oscillator

When using an external crystal or ceramic resonator as the frequency reference for the MCU clock system, refer to the following table and diagrams.

The feedback resistor, RF, is incorporated internally with the low power oscillators. An external feedback is required when using high gain (HGO=1) mode.

The series resistor, RS, is required in high gain (HGO=1) mode when the crystal or resonator frequency is below 2 MHz. Otherwise, the low power oscillator (HGO=0) must not have any series resistance; and the high frequency, high gain oscillator with a frequency above 2 MHz does not require any series resistance.

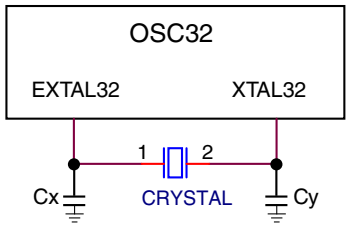


Figure 40. RTC Oscillator (OSC32) module connection – Diagram 1

Table 64. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768 kHz), high gain	Diagram 3
High frequency (1-32 MHz), low power	Diagram 2
High frequency (1-32 MHz), high gain	Diagram 3

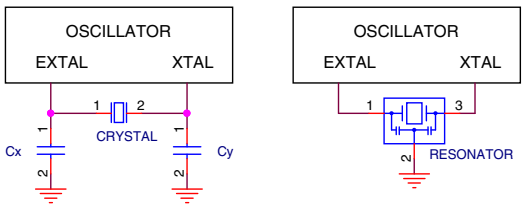


Figure 41. Crystal connection – Diagram 2

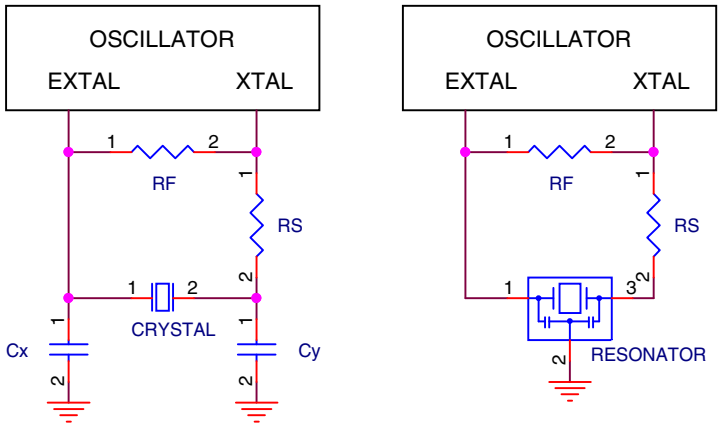


Figure 42. Crystal connection – Diagram 3

NOTE

For PCB layout, the user could consider to add the guard ring to the crystal oscillator circuit.

6.2 Software considerations

All Kinetis MCUs are supported by comprehensive NXP and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit http://www.nxp.com/kinetis/sw for more information and supporting collateral.

Evaluation and Prototyping Hardware

- Tower System Development Platform: http://www.nxp.com/tower

IDEs for Kinetis MCUs

- Kinetis Design Studio IDE: http://www.nxp.com/kds
- Partner IDEs: http://www.nxp.com/kide

Run-time Software

- Kinetis SDK: http://www.nxp.com/ksdk
- Kinetis Bootloader: http://www.nxp.com/kboot
- ARM mbed Development Platform: http://www.nxp.com/mbed

For all other partner-developed software and tools, visit http://www.nxp.com/partners.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Table 65. Part number fields description

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KE##	Kinetis family	• KE18, KE16, KE14
A	Key attribute	• D = Cortex-M4 with DSP • F = Cortex-M4 with DSP and FPU
FFF	Program flash memory size	• 512 = 512 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 16 = 168 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKE18F512VLL16

8 Revision history

The following table provides a revision history for this document.

Table 66. Revision history

Rev. No.	Date	Substantial Changes
2	09/2016	Initial public release.

How to Reach Us:

Home Page:
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