MPC8640D Integrated Dual-Core Processor

Built on Power Architecture® technology

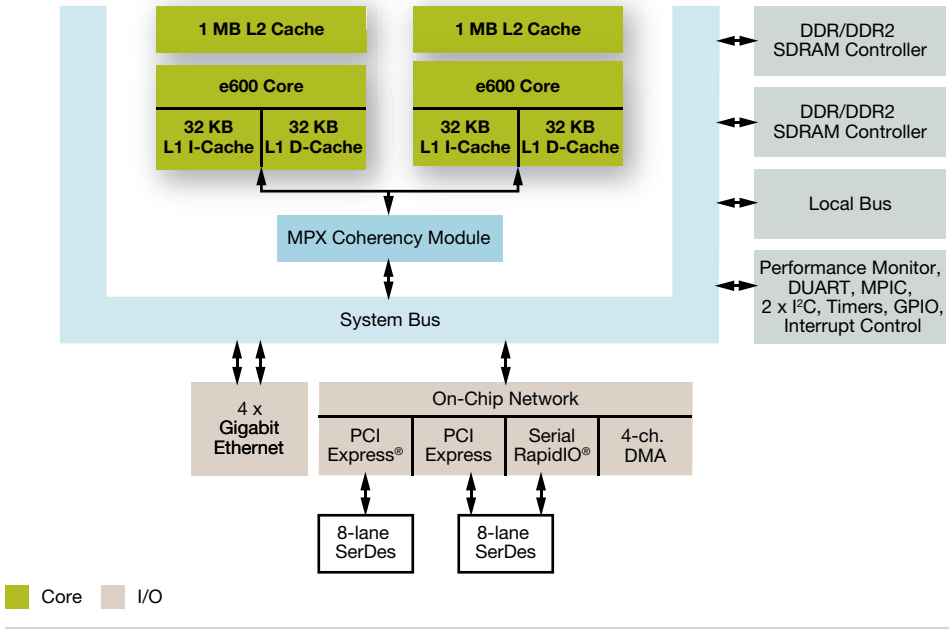
Freescale's MPC8640D dual-core processor is engineered to deliver breakthrough performance, connectivity and integration for embedded networking, telecom, aerospace and defense, storage, industrial and pervasive computing applications.

The MPC8640D's strength is its integration—the high-performance e600 core, built on Power Architecture® technology, combined with the PowerQUICC® system-on-chip (SoC) platform. With dual-core performance and integrated northbridge and southbridge functionality, this single chip can replace what could take up to four chips using other solutions. This translates into smaller boards or higher processing density. Additionally, all core-to-peripheral connections are internal in an integrated device, so the board designer is not exposed to the difficulties of laying out high-speed parallel buses.

The MPC8640D features two e600 cores operating at up to 1250 MHz. Each has its own ECC-protected 1 MB backside L2 caches for avoidance of "cache thrashing." The per-core AltiVec® 128-bit vector processing engines commonly achieve a 3x to 10x performance increase as shown by EEMBC benchmarks. The peripherals are derived from the field-proven PowerQUICC family, allowing for significant software reuse across Freescale product lines.

One of the significant advantages of the MPC8640D is the fully integrated MPX bus that can run three times faster than an external MPX bus. With MPX bus speed proportional to memory bandwidth and inversely related to memory latency, this integrated bus relieves system bottlenecks for applications limited by either condition. In addition, the MPC8640D features dual integrated memory controllers that provide support for both DDR and DDRII memories, thus increasing bandwidth and capacity while reducing latency. The memory controllers support error correction codes to ensure data integrity, a basic requirement for any application that needs reliability.

MPC8640D Block Diagram



In addition to its performance enhancements, the highly integrated MPC8640D can replace multiple devices, resulting in huge savings in board cost and space. With its on-chip, high-speed interfaces, including the standard RapidIO® fabric interface, PCI Express® interfaces and Gigabit Ethernet interfaces, the MPC8640D does not require system controllers or northbridges and southbridges.

The two cores can run in symmetric multiprocessing mode (SMP) where one operating system assigns tasks to each core, or asymmetric multiprocessing mode, where each core can run an entirely separate OS.

The MPC8640D processor provides extensive application flexibility for developers, offering various options for assigning distinct processing resources to tasks that need guaranteed performance.

Example 1: A **high-end line card** uses an ASIC or ASSP for the data path and MPC8640D for the control plane. The two cores can operate in SMP mode for straightforward performance scaling. Two separate operating systems may be used for separate control plane functions, such as off loading security, classification and quality-of-service (QoS) tasks from the core running the main OS.

Example 2: A **mid-range line card** uses the MPC8640D to implement both the control and data plane and can be organized in a variety of ways, including splitting functionality directionally (one core per direction) or splitting functionality vertically (one core for handling data plane, one for control plane).

Example 3: A **services card**, leveraging the MPC8640D, supports a new feature set in a centralized manner, receiving traffic from all line cards. The RapidIO port connects to the fabric and the Gigabit Ethernet ports implement a management interface.

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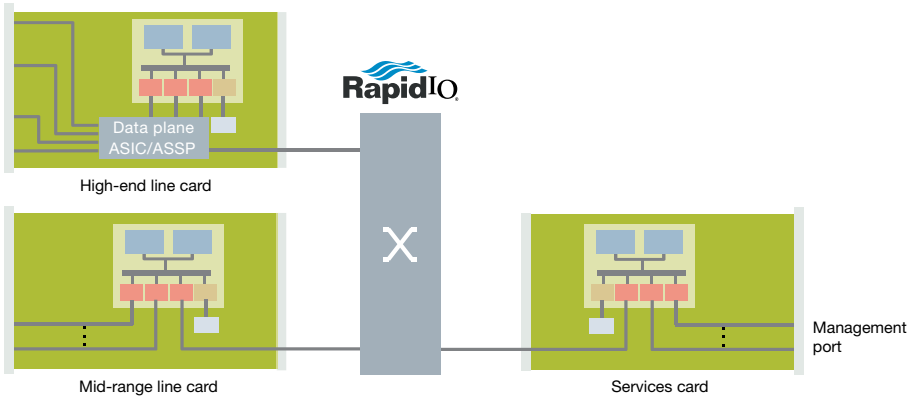
MPC8640D Processor Highlights

CPU Speeds (internal)	• 1,000/1,250 MHz
Typical Power	• 14 watts; 21 watts
MPX Bus (integrated)	• Up to 500 MHz, 64-bit
L1 Cache (integrated)	• 32 KB instruction, 32 KB data per core with parity protection
L2 Cache (integrated)	• 1 MB per core with optional ECC
Package	• 33 x 33 mm, 1023-pin, high-thermal coefficient of expansion (HCTE) ceramic package
Process Technology	• 90 nm silicon-on-insulator (SOI)
Execution Units	• Integer (4), floating-point, AltiVec (4), branch, load/store per core
RapidIO® Interface	• 1x/4x serial at Gbaud/lane intervals of 1.25, 2.5 and 3.125 • DMA and message-based programming models • Message unit supports SARing up to 4 KB messages into 256-byte packets • Hardware-based error recovery
PCI Express® Interface	• One or two 1x/4x/8x serial at 2.5 Gbaud/lane • Configurable as root complex or endpoint • Maximum supported packet payload size is 256 bytes
Ethernet Interface	• Four 10/100/1000 Ethernet controllers • Supports MII, RMII, GMII, RGMII, TBI and RTBI • Accelerates TCP and UPD checksum operations • 64 receive queues and eight transmit queues per Ethernet controller with QoS features • Classification and filtering capabilities • High-efficiency FIFO mode for ASIC/FPGA connectivity
Memory Controller	• Supports dual 64-bit DDR and DDRII with up to 500 MHz data rate with ECC
DMA Controller	• Four independent channels with bandwidth control per channel
Multiprocessor Interrupt Controller	• Four inter-core messaging interrupts • Steering of interrupts to either core
Local Bus	• 32-bit multiplexed address/data
Availability	• Samples: now • Production: now

System Example Using the MPC8640D Processor



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