

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
 - “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
 - “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
 - “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

μ PD70F3003A, 70F3025A, 70F3003A(A)

V853 32-BIT SINGLE-CHIP MICROCONTROLLERS

DESCRIPTION

The μ PD70F3003A, μ PD70F3025A, and μ PD70F3003A(A) have a flash memory instead of the internal mask ROM of the μ PD703003A/703004A, μ PD703025A, and μ PD703003A(A), respectively. This model is useful for small-scale production of a variety of application sets or early start of production since the program can be written and erased by the user even with the μ PD70F3003 mounted on the board.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

V853 Hardware User's Manual: U10913E
V850 Series Architecture User's Manual: U10243E

FEATURES

- Compatible with μ PD703003A, 703004A, 703025A, and 703003A(A)
 - Can be replaced with mask ROM model for mass production of application set
 - μ PD70F3003A \rightarrow μ PD703003A, 703004A
 - μ PD70F3025A \rightarrow μ PD703025A
 - μ PD70F3003A(A) \rightarrow μ PD703003A(A)
- Internal memory Flash memory: 128KB (μ PD70F3003A, 70F3003A(A))
256KB (μ PD70F3025A)

Remark For differences among the products, refer to 1. DIFFERENCES BETWEEN PRODUCT.

★ ORDERING INFORMATION

Part Number	Package	Quality Grade
μ PD70F3003AGC-33-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μ PD70F3003AGC-33-8EU-A	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μ PD70F3025AGC-33-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μ PD70F3025AGC-33-8EU-A	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μ PD70F3003AGC(A)-33-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special

- Remarks**
1. The μ PD70F3003A and μ PD70F3003A(A) differ in the quality grade only.
 2. Products with -A at the end of the part number are lead-free products.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

APPLICATIONS

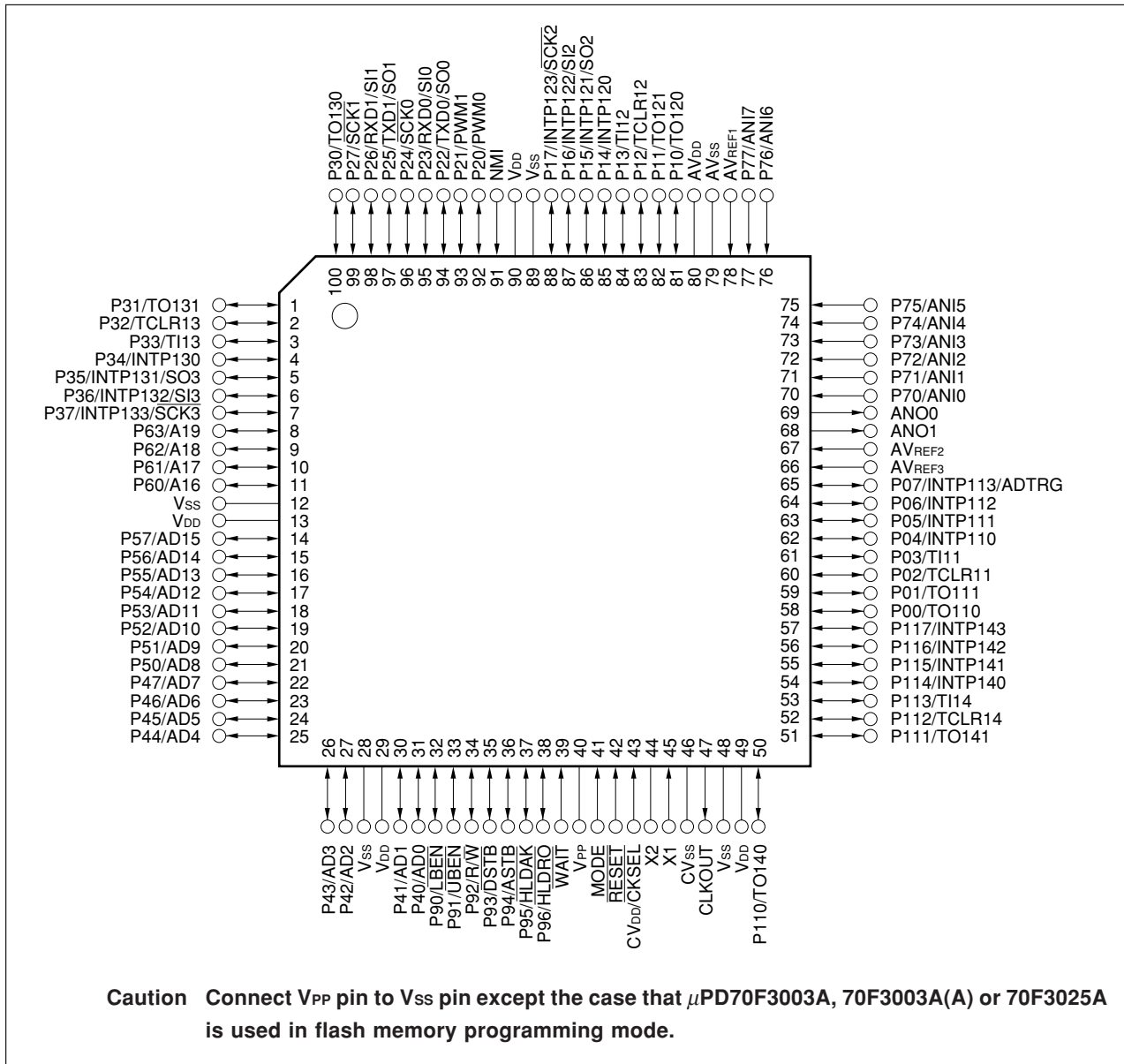
μPD70F3003A, 70F3025A: Camcorders, VCRs, PPCs, LBPs, printers, motor controllers, NC machine tools, mobile telephones, etc.

μPD70F3003A(A): Medical equipment, automotive appliances, etc.

★ PIN CONFIGURATION (Top View)

• 100-Pin Plastic LQFP (fine pitch) (14 × 14)

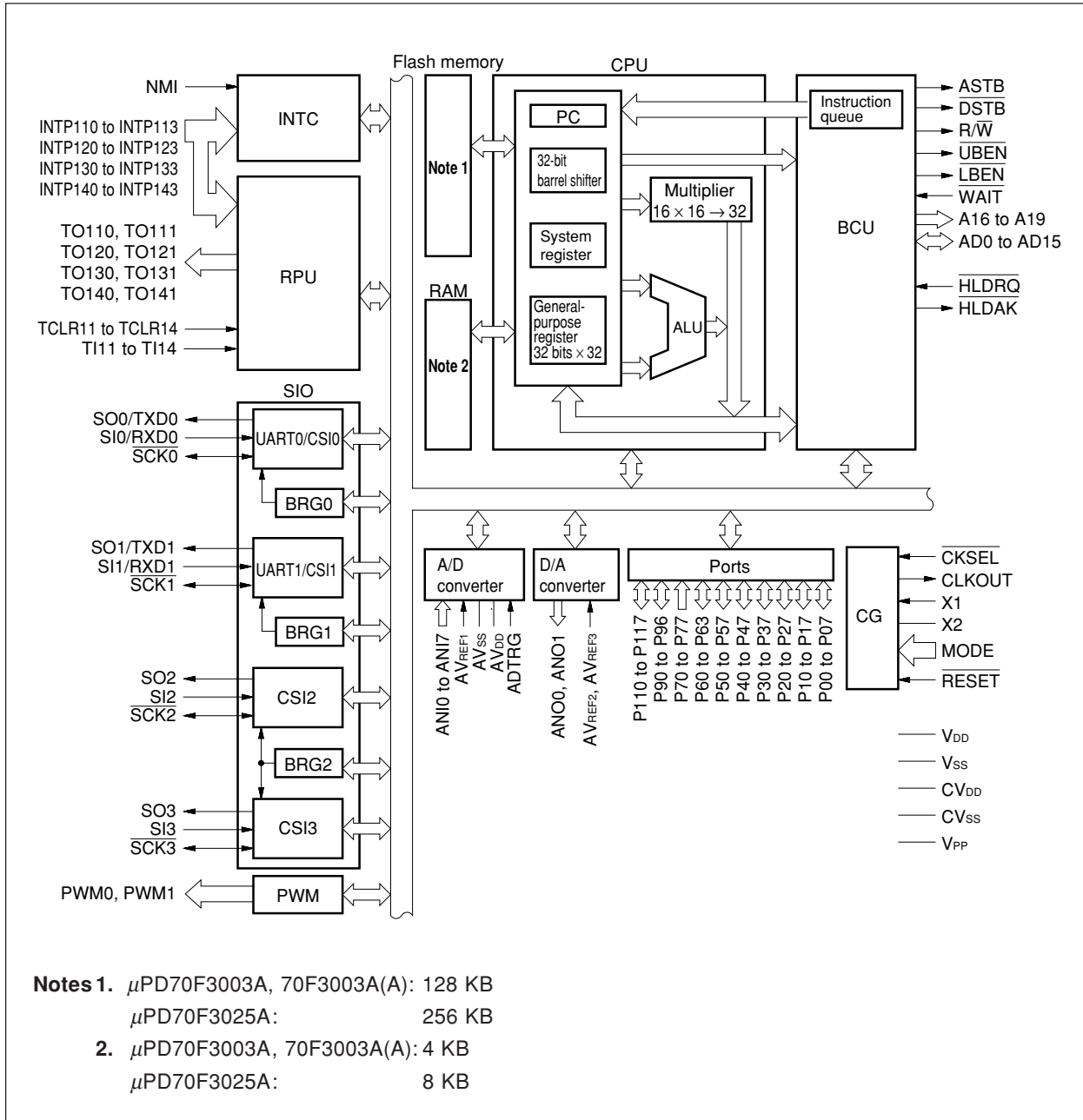
- μPD70F3003AGC-33-8EU μPD70F3025AGC-33-8EU
- μPD70F3003AGC-33-8EU-A μPD70F3025AGC-33-8EU-A
- μPD70F3003AGC(A)-33-8EU



PIN NAMES

A16 to A19:	Address bus	P40 to P47:	Port 4
AD0 to AD15:	Address/data bus	P50 to P57:	Port 5
ADTRG:	A/D Trigger input	P60 to P63:	Port 6
ANI0 to ANI7:	Analog input	P70 to P77:	Port 7
ANO0, ANO1:	Analog output	P90 to P96:	Port 9
ASTB:	Address strobe	P110 to P117:	Port 11
AV _{DD} :	Analog V _{DD}	PWM0, PWM1:	Pulse width modulation
AV _{REF1} to AV _{REF3} :	Analog reference voltage	$\overline{\text{RESET}}$:	Reset
AV _{SS} :	Analog V _{SS}	R/W:	Read/write status
CV _{DD} :	Power supply for clock generator	RXD0, PxD1:	Receive data
CV _{SS} :	Ground for clock generator	$\overline{\text{SCK0}}$ to $\overline{\text{SCK3}}$:	Serial clock
$\overline{\text{CKSEL}}$:	Clock select	SI0 to SI3:	Serial input
CLKOUT :	Clock output	SO0 to SO3:	Serial output
$\overline{\text{DSTB}}$:	Data strobe	TO110, TO111,	
$\overline{\text{HLD\!AK}}$:	Hold acknowledge	TO120, TO121,	
$\overline{\text{HLDRQ}}$:	Hold request	TO130, TO131,	
INTP110 to INTP113,		TO140, TO141:	Timer output
INTP120 to INTP123,		TCLR11 to TCLR14:	Timer clear
INTP130 to INTP133,		TI11 to TI14:	Timer input
INTP140 to INTP143:	Interrupt request from peripherals	TXD0, TXD1:	Transmit data
$\overline{\text{LBEN}}$:	Lower byte enable	$\overline{\text{UBEN}}$:	Upper byte enable
MODE:	Mode	$\overline{\text{WAIT}}$:	Wait
NMI:	Non-maskable interrupt request	X1, X2:	Crystal
P00 to P07:	Port 0	V _{DD} :	Power supply
P10 to P17:	Port 1	V _{PP} :	Programming power supply
P20 to P27:	Port 2	V _{SS} :	Ground
P30 to P37:	Port 3		

INTERNAL BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN PRODUCTS	6
2. PIN FUNCTIONS	7
2.1 Port Pins	7
2.2 Non-Port Pins	9
2.3 Pin I/O Circuits and Recommended Connection of Unused Pins	11
3. ELECTRICAL SPECIFICATIONS	14
3.1 Normal Operation Mode	14
3.2 Flash Memory Programming Mode	37
4. PACKAGE DRAWING	40
5. RECOMMENDED SOLDERING CONDITIONS	41
★ APPENDIX NOTES ON TARGET SYSTEM DESIGN	43

1. DIFFERENCES BETWEEN PRODUCTS

Item	μPD703003A	μPD703004A	μPD703025A	μPD703003A(A)	μPD703025A(A)	μPD70F3003A	μPD70F3025A	μPD70F3003A(A)
Internal ROM	Mask ROM					Flash memory		
	128 KB	96 KB	256 KB	128 KB	256 KB	128 KB	256 KB	128 KB
Internal RAM	4 KB		8 KB	4 KB	8 KB	4 KB	8 KB	4 KB
Flash memory programming mode	None					Provided		
V _{PP} pin	None					Provided		
Quality grade	Standard			Special		Standard		Special
Electrical specifications	Current consumption, etc. differs. (Refer to each product data sheets).							
Others	Noise immunity and noise radiation differ because circuit scale and mask layout differ.							

Caution There are differences in noise immunity and noise radiation between the flash memory version and mask ROM version. When pre-producing an application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluation for commercial samples (not engineering samples) of the mask ROM version.

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit I/O port. Input/output can be specified in 1-bit units.	TO110
P01			TO111
P02			TCLR11
P03			TI11
P04			INTP110
P05			INTP111
P06			INTP112
P07			INTP113/ADTRG
P10	I/O	Port 1 8-bit I/O port. Input/output can be specified in 1-bit units.	TO120
P11			TO121
P12			TCLR12
P13			TI12
P14			INTP120
P15			INTP121/SO2
P16			INTP122/SI2
P17			INTP123/SCK2
P20	I/O	Port 2 8-bit I/O port. Input/output can be specified in 1-bit units.	PWM0
P21			PWM1
P22			TXD0/SO0
P23			RXD0/SI0
P24			SCK0
P25			TXD1/SO1
P26			RXD1/SI1
P27			SCK1
P30	I/O	Port 3 8-bit I/O port. Input/output can be specified in 1-bit units.	TO130
P31			TO131
P32			TCLR13
P33			TI13
P34			INTP130
P35			INTP131/SO3
P36			INTP132/SI3
P37			INTP133/SCK3
P40 to P47	I/O	Port 4 8-bit I/O port. Input/output can be specified in 1-bit units.	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit I/O port. Input/output can be specified in 1-bit units.	AD8 to AD15

(2/2)

Pin Name	I/O	Function	Alternate Function
P60 to P63	I/O	Port 6 4-bit I/O port. Input/output can be specified in 1-bit units.	A16 to A19
P70 to P77	Input	Port 7 8-bit input port.	ANI0 to ANI7
P90	I/O	Port 9 7-bit I/O port. Input/output can be specified in 1-bit units.	$\overline{\text{LBEN}}$
P91			$\overline{\text{UBEN}}$
P92			R/ $\overline{\text{W}}$
P93			$\overline{\text{DSTB}}$
P94			ASTB
P95			$\overline{\text{HLD\text{A}K}}$
P96			H $\overline{\text{LDRQ}}$
P110	I/O	Port 11 8-bit I/O port. Input/output can be specified in 1-bit units.	TO140
P111			TO141
P112			TCLR14
P113			TI14
P114			INTP140
P115			INTP141
P116			INTP142
P117			INTP143

2.2 Non-Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
TO110	Output	Pulse signal output from timers 11 to 14	P00
TO111			P01
TO120			P10
TO121			P11
TO130			P30
TO131			P31
TO140			P110
TO141			P111
TCLR11	Input	External clear signal input for timers 11 to 14	P02
TCLR12			P12
TCLR13			P32
TCLR14			P112
TI11	Input	External count clock input for timers 11 to 14	P03
TI12			P13
TI13			P33
TI14			P113
INTP110	Input	External maskable interrupt request input and external capture trigger input for timer 11	P04
INTP111			P05
INTP112			P06
INTP113			P07/ADTRG
INTP120	Input	External maskable interrupt request input and external capture trigger input for timer 12	P14
INTP121			P15/SO2
INTP122			P16/S12
INTP123			P17/ $\overline{\text{SCK}}_2$
INTP130	Input	External maskable interrupt request input and external capture trigger input for timer 13	P34
INTP131			P35/SO3
INTP132			P36/SI3
INTP133			P37/ $\overline{\text{SCK}}_3$
INTP140	Input	External maskable interrupt request input and external capture trigger input for timer 14	P114
INTP141			P115
INTP142			P116
INTP143			P117
SO0	Output	Serial transmit data output for CSI0 to CSI3 (3-wire)	P22/TXD0
SO1			P25/TXD1
SO2			P15/INTP121
SO3			P35/INTP131
SI0	Input	Serial receive data output for CSI0 to CSI3 (3-wire)	P23/RXD0
SI1			P26/RXD1
SI2			P16/INTP122
SI3			P36/INTP132

(2/2)

Pin Name	I/O	Function	Alternate Function
$\overline{\text{SCK0}}$	I/O	Serial clock I/O for CSI0 to CSI3 (3-wire)	P24
$\overline{\text{SCK1}}$			P27
$\overline{\text{SCK2}}$			P17/INTP123
$\overline{\text{SCK3}}$			P37/INTP133
TXD0	Output	Serial transmit data output of UART0 to UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input of UART0 to UART1	P23/SI0
RXD1			P26/SI1
PWM0	Output	Pulse signal output of PWM	P20
PWM1			P21
AD0 to AD7	I/O	16-bit multiplexed address/data bus when external memory is connected	P40 to P47
AD8 to AD15			P50 to P57
A16 to A19	Output	Higher address bus when external memory is connected	P60 to P63
$\overline{\text{LBEN}}$	Output	Lower byte enable signal output of external data bus	P90
$\overline{\text{UBEN}}$		Higher byte enable signal output of external data bus	P91
$\text{R}/\overline{\text{W}}$	Output	External read/write status output	P92
$\overline{\text{DSTB}}$		External data strobe signal output	P93
ASTB		External address strobe signal output	P94
$\overline{\text{HLDAK}}$	Output	Bus hold acknowledge output	P95
$\overline{\text{HLDRQ}}$	Input	Bus hold request input	P96
ANI0 to ANI7	Input	Analog input to A/D converter	P70 to P77
ANO0, ANO1	Output	Analog output of D/A converter	—
NMI	Input	Non-maskable interrupt request input	—
CLKOUT	Output	System clock output	—
$\overline{\text{CKSEL}}$	Input	Input specifying operation mode of clock generator	CV _{DD}
$\overline{\text{WAIT}}$	Input	Control signal input inserting wait state in bus cycle	—
MODE	Input	Operation mode specification	—
$\overline{\text{RESET}}$	Input	System reset input	—
X1	Input	System clock resonator connection. Input external clock to X1 to supply external clock.	—
X2	—		—
ADTRG	Input	A/D converter external trigger input	P07/INTP113
AV _{REF1}	Input	Reference voltage input for A/D converter	—
AV _{REF2}	Input	Reference voltage input for D/A converter	—
AV _{REF3}			—
AV _{DD}	—	Positive power supply for A/D converter	—
AV _{SS}	—	Ground potential for A/D converter	—
CV _{DD}	—	Positive power supply for internal clock generator	$\overline{\text{CKSEL}}$
CV _{SS}	—	Ground potential for internal clock generator	—
V _{DD}	—	Positive power supply	—
V _{SS}	—	Ground potential	—
V _{PP}	—	High voltage application pin when program is written/verified	—

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

Table 2-1 shows the I/O circuit type of each pin, and the recommended connections of the unused pins. Figure 2-1 shows a partially simplified diagram of each circuit.

It is recommended that 1 to 10 kΩ resistors be used when connecting to V_{DD} or V_{SS} via a resistor.

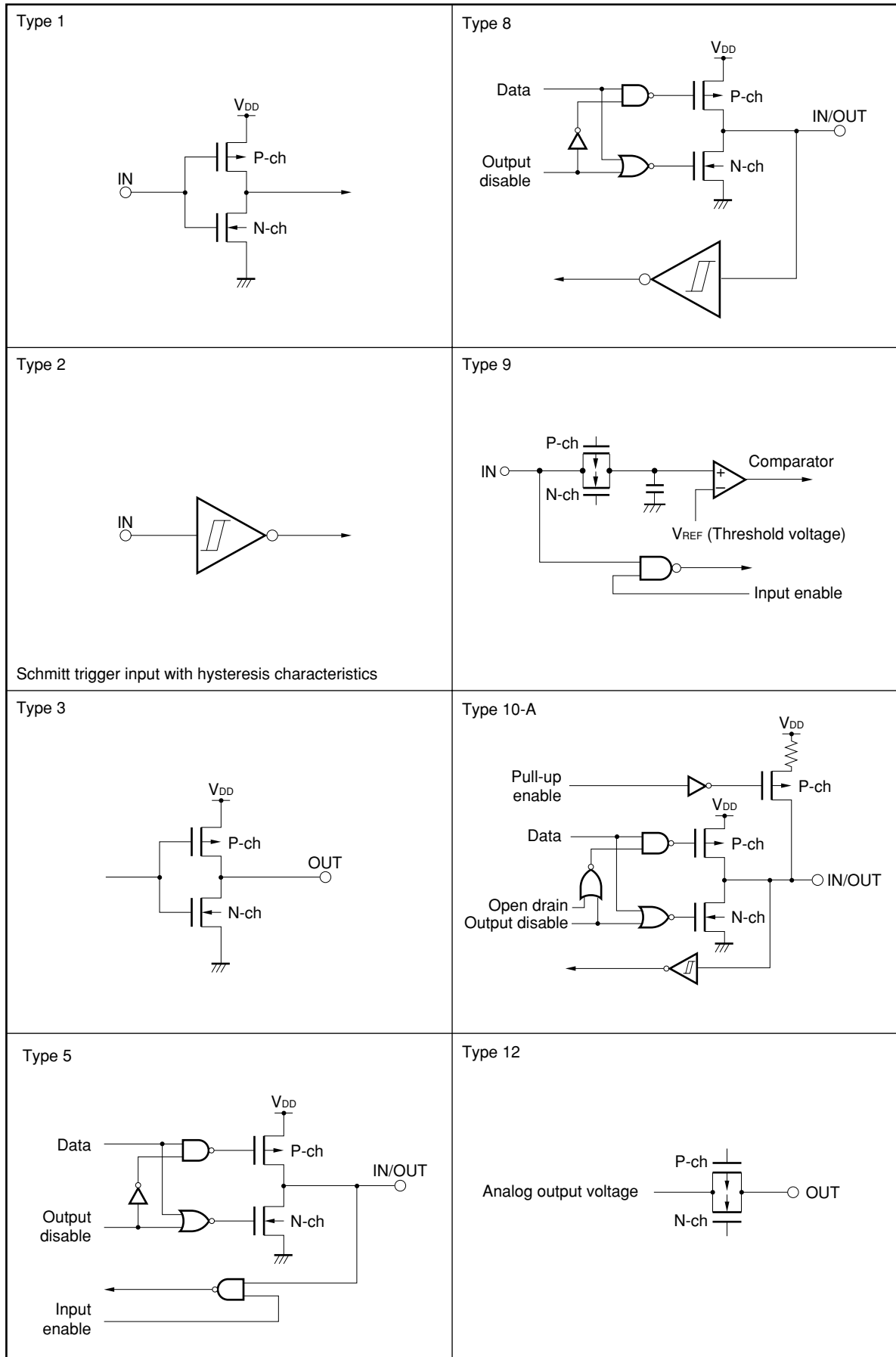
Table 2-1. Types of Pin I/O Circuits and Recommended Connections of Unused Pins (1/2)

Pin Name	I/O Circuit Type	Recommended Connection of Unused Pins
P00/TO110, P01/TO111	5	Input: Independently connect to V _{DD} or V _{SS} via a resistor.
P02/TCLR11, P03/TI11, P04/INTP110 to P07/INTP113/ADTRG	8	Output: Leave open.
P10 to TO120, P11/TO121	5	
P12/TCLR12, P13/TI12 P14/INTP120 P15/INTP121/SO2 P16/INTP122/SI2 P17/INTP123/ $\overline{\text{SCK2}}$	8	
P20/PWM0, P21/PWM1 P22/TXD0/SO0	5	
P23/RXD0/SI0, P24/ $\overline{\text{SCK0}}$	8	
P25/TXD1/SO1	5	
P26/RXD1/SI1, P27/ $\overline{\text{SCK1}}$	8	
P30/TO130, P31/TO131	5	
P32/TCLR13, P33/TI13 P34/INTP130	8	
P35/INTP131/SO3 P36/INTP132/SI3 P37/INTP133/ $\overline{\text{SCK3}}$	10-A	
P40/AD0 to P47/AD7 P50/AD8 to P57/AD15 P60/A16 to P63/A19	5	
P70/ANI0 to P77/ANI7	9	Directly connect to V _{SS} .
P90/ $\overline{\text{LBEN}}$ P91/ $\overline{\text{UBEN}}$ P92/ $\overline{\text{R/W}}$ P93/ $\overline{\text{DSTB}}$ P94/ASTB P95/HLDAK P96/HLDRQ P110/TO140, P111/TO141	5	Input: Independently connect to V _{DD} or V _{SS} via a resistor. Output: Leave open.
P112/TCLR14, P113/TI14 P114/INTP140 to P117/INTP143	8	

Table 2-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins (2/2)

Pin Name	I/O Circuit Type	Recommended Connection of Unused Pins
ANO0, ANO1	12	Leave open.
NMI	2	Directly connect to V _{SS} .
CLKOUT	3	Leave open.
WAIT	1	Directly connect to V _{DD} .
MODE	2	—
RESET		—
CV _{DD} /CKSEL		—
AV _{REF1} to AV _{REF3} , AV _{SS}	—	Directly connect to V _{SS} .
AV _{DD}	—	Directly connect to V _{DD} .
V _{PP}	—	Connect to V _{SS} .

Figure 2-1. Pins I/O Circuits



3. ELECTRICAL SPECIFICATIONS

3.1 Normal Operation Mode

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions	Ratings	Unit	
Supply voltage	V _{DD}	V _{DD} pin	-0.5 to +7.0	V	
	CV _{DD}	CV _{DD} pin	-0.5 to V _{DD} + 0.3 ^{Note 1}	V	
	CV _{SS}	CV _{SS} pin	-0.5 to +0.5	V	
	AV _{DD}	AV _{DD} pin	-0.5 to V _{DD} + 0.3 ^{Note 1}	V	
	AV _{SS}	AV _{SS} pin	-0.5 to +0.5	V	
Input voltage	V _{I1}	Note 2 , V _{DD} = 5.0 V ±10%	-0.5 to V _{DD} + 0.3 ^{Note 1}	V	
	V _{I2}	V _{PP} pin in flash memory programming mode, V _{DD} = 5.0 V ±10%	-0.5 to +11.0	V	
Clock input voltage	V _K	X1 pin, V _{DD} = 5.0 V ±10%	-0.5 to V _{DD} + 1.0 ^{Note 1}	V	
Output current, low	I _{CL}	1 pin	4.0	mA	
		Total of all pins	100	mA	
Output current, high	I _{CH}	1 pin	-4.0	mA	
		Total of all pins	-100	mA	
Output voltage	V _O	V _{DD} = 5.0 V ±10%	-0.5 to V _{DD} + 0.3 ^{Note 1}	V	
Analog input voltage	V _{IAN}	P70/ANI0 to P77/ANI7	AV _{DD} > V _{DD}	-0.5 to V _{DD} + 0.3 ^{Note 1}	V
			V _{DD} ≥ AV _{DD}	-0.5 to AV _{DD} + 0.3 ^{Note 1}	V
Analog reference input voltage	AV _{REF}	AV _{REF1} to AV _{REF3}	AV _{DD} > V _{DD}	-0.5 to V _{DD} + 0.3 ^{Note 1}	V
			V _{DD} ≥ AV _{DD}	-0.5 to AV _{DD} + 0.3 ^{Note 1}	V
Operating ambient temperature	T _A		-40 to +85	°C	
Storage temperature	T _{stg}		-65 to +125	°C	

- Notes**
1. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.
 2. X1, P70 to P77, AV_{REF1} to AV_{REF3}, and their alternate-function pins are excluded.

- Cautions**
1. Avoid direct connections among the IC device output (or I/O) pins and between V_{DD} or V_{CC} and GND. However, direct connections among open-drain and open-collector pins are possible, as are direct connections to external circuits that have timing designed to prevent output conflict with pins that become high-impedance.
 2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The normal operating ranges of ratings and conditions in which the quality of the product is guaranteed are specified in the following DC Characteristics and AC Characteristics.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C _i	fc = 1 MHz Pins other than tested pin: 0 V			15	pF
I/O capacitance	C _{io}				15	pF
Output capacitance	C _o				15	pF

Operating Conditions

Operation Mode	Internal System Clock Frequency (φ)	Operating Temperature (T _A)	Supply Voltage (V _{DD})
Direct mode, PLL mode	2 to 33 MHz ^{Note 1}	-40 to +85°C	5.0 V ±10%
	5 to 33 MHz ^{Note 2}	-40 to +85°C	5.0 V ±10%

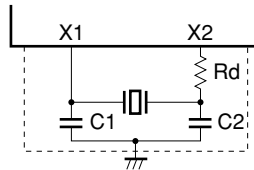
- Notes 1.** When A/D converter not used.
2. When A/D converter used.

Recommended Oscillator

Caution For the resonator selection and oscillator constant of the μPD70F3003A(A), customers are requested to apply to the resonator manufacturer for evaluation.

(1) Ceramic resonator connection (T_A = -40 to +85°C)

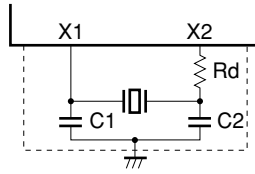
(a) μPD70F3003A



Manufacturer	Part Number	Oscillation Frequency f _{xx} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T _{OST} (ms)
			C1 (pF)	C2 (pF)	R _d (Ω)	MIN. (V)	MAX. (V)	
Kyocera Corporation	PBRC4.00HR	4.0	On-chip	On-chip	—	4.5	5.5	0.10
	PBRC5.00HR	5.0	On-chip	On-chip	—	4.5	5.5	0.08
	PBRC6.00HR	6.0	On-chip	On-chip	—	4.5	5.5	0.08
	PBRC6.60HR	6.6	On-chip	On-chip	—	4.5	5.5	0.08
TDK	FCR4.0MC5	4.0	On-chip	On-chip	—	4.5	5.5	0.14
	FCR5.0MC5	5.0	On-chip	On-chip	—	4.5	5.5	0.14
	FCR6.0MC5	6.0	On-chip	On-chip	—	4.5	5.5	0.11
Murata Mfg. Co., Ltd	CSTS0400MG06	4.0	On-chip	On-chip	—	4.5	5.5	0.12
	CSTCR4M00G05	4.0	On-chip	On-chip	—	4.5	5.5	0.14
	CSTS0600MG06	6.0	On-chip	On-chip	—	4.5	5.5	0.14
	CSTCR6M00G55-R0	6.0	On-chip	On-chip	—	4.5	5.5	0.18

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
 2. Do not wire any other signal lines in the area indicated by the broken lines.
 3. Thoroughly evaluate the matching between the μPD70F3003A and the resonator.

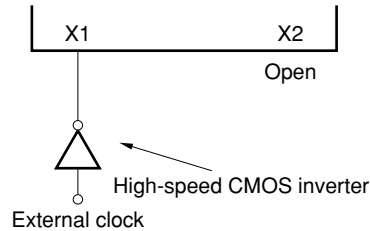
(b) μ PD70F3025A



Manufacturer	Part Number	Oscillation Frequency f_{xx} (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	R_d (W)	MIN. (V)	MAX. (V)	
Kyocera Corporation	PBRC4.00HR	4.0	On-chip	On-chip	—	4.5	5.5	0.12
	PBRC5.00HR	5.0	On-chip	On-chip	—	4.5	5.5	0.04
	PBRC6.00HR	6.0	On-chip	On-chip	—	4.5	5.5	0.04
	PBRC6.60HR	6.6	On-chip	On-chip	—	4.5	5.5	0.04
TDK	FCR4.0MC5	4.0	On-chip	On-chip	—	4.5	5.5	0.14
	FCR5.0MC5	5.0	On-chip	On-chip	—	4.5	5.5	0.13
	FCR6.0MC5	6.0	On-chip	On-chip	—	4.5	5.5	0.13
Murata Mfg. Co., Ltd	CSTS0400MG06	4.0	On-chip	On-chip	—	4.5	5.5	0.12
	CSTCR4M00G55-R0	4.0	On-chip	On-chip	—	4.5	5.5	0.14
	CSTS0600MG06	6.0	On-chip	On-chip	—	4.5	5.5	0.16
	CSTCR6M00G55-R0	6.0	On-chip	On-chip	—	4.5	5.5	0.19

- Cautions**
1. Connect the oscillator as closely to the X1 and X2 pins as possible.
 2. Do not wire any other signal lines in the area indicated by the broken lines.
 3. Thoroughly evaluate the matching between the μ PD70F3025A and the resonator.

(2) External clock input



- Cautions**
1. Put the high-speed CMOS inverter as close to the X1 pins as possible.
 2. Sufficiently evaluate the matching between the μ PD70F3003A, 70F3025A, or 70F3003A(A), and the high-speed CMOS inverter.

DC Characteristics (T_A = -40 to +85°C, V_{DD} = 5.0 V ±10%, V_{SS} = 0 V)

(1/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH}	Except X1 and Note	2.2		V _{DD} + 0.3	V
		Note	0.8V _{DD}		V _{DD} + 0.3	V
Input voltage, low	V _{IL}	Except X1 and Note	-0.5		+0.8	V
		Note	-0.5		0.2V _{DD}	V
Clock input voltage, high	V _{XH}	X1	0.8V _{DD}		V _{DD} + 0.5	V
Clock input voltage, low	V _{XL}	X1	-0.5		0.6	V
Schmitt trigger input threshold voltage	V _T ⁺	Note , rising		3.0		V
	V _T ⁻	Note , falling		2.0		V
Schmitt trigger input hysteresis width	V _T ⁺ - V _T ⁻	Note	0.5			V
Output voltage, high	V _{OH}	I _{OH} = -2.5 mA	0.7V _{DD}			V
		I _{OH} = -100 μA	V _{DD} - 0.4			V
Output voltage, low	V _{OL}	I _{OC} = 2.5 mA			0.45	V
Input leakage current, high	I _{LIH}	V _I = V _{DD}			10	μA
Input leakage current, low	I _{LIL}	V _I = 0 V			-10	μA
Output leakage current, high	I _{LOH}	V _O = V _{DD}			10	μA
Output leakage current, low	I _{LOL}	V _O = 0 V			-10	μA
Software pull-up resistor	R	P35/INTP131/SO3, P36/INTP132/SI3, P37/INTP133/SCK3	15	40	90	kΩ

Note P02 to P07, P12 to P17, P23, P24, P26, P27, P32 to P37, P112 to P117, $\overline{\text{RESET}}$, NMI, MODE, and their alternate-function pins.

Remark TYP. values are reference values for when T_A = 25°C and V_{DD} = 5.0 V.

(2/2)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Supply current	μPD70F3003A, 70F3003A(A)	Operating	I _{DD1}	Direct mode		$2.2 \times \phi + 7.5$	$2.5 \times \phi + 22$	mA
				PLL mode		$2.3 \times \phi + 9.5$	$2.6 \times \phi + 25$	mA
		In HALT mode	I _{DD2}	Direct mode		$1.2 \times \phi + 7.5$	$1.3 \times \phi + 15$	mA
				PLL mode		$1.3 \times \phi + 9.5$	$1.4 \times \phi + 17$	mA
		In IDLE mode	I _{DD3}	Direct mode		$8 \times \phi + 300$	$10 \times \phi + 500$	μA
				PLL mode		$0.1 \times \phi + 2$	$0.2 \times \phi + 3$	mA
		In STOP mode	I _{DD4}	CESEL = 0, Note 1		2	50	μA
				CESEL = 0, Note 2		2	200	μA
	CESEL = 1, Note 1				30	200	μA	
	CESEL = 1, Note 2				30	500	μA	
	μPD70F3025A	Operating	I _{DD1}	Direct mode		$2.5 \times \phi + 8$	$2.8 \times \phi + 22.5$	mA
				PLL mode		$2.6 \times \phi + 10$	$2.9 \times \phi + 25.5$	mA
		In HALT mode	I _{DD2}	Direct mode		$1.3 \times \phi + 7.5$	$1.4 \times \phi + 15$	mA
				PLL mode		$1.3 \times \phi + 12.5$	$1.4 \times \phi + 20$	mA
		In IDLE mode	I _{DD3}	Direct mode		$8 \times \phi + 300$	$10 \times \phi + 500$	μA
				PLL mode		$0.1 \times \phi + 2$	$0.2 \times \phi + 3$	mA
In STOP mode		I _{DD4}	CESEL = 0, Note 1		2	50	μA	
			CESEL = 0, Note 2		2	200	μA	
	CESEL = 1, Note 1			60	300	μA		
	CESEL = 1, Note 2			60	500	μA		

Notes 1. $-40^{\circ}\text{C} \leq T_A \leq +50^{\circ}\text{C}$

2. $50^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$

Remarks 1. TYP. values are reference values for when $T_A = 25^{\circ}\text{C}$ (except for the conditions in **Note 2**) and $V_{DD} = 5.0\text{V}$. The power supply current does not include AV_{REF1} to AV_{REF3} or the current that flows through software pull-up resistors.

2. ϕ : Internal system clock frequency

Data Retention Characteristics (T_A = -40 to +85°C, V_{DD} = V_{DDDR})

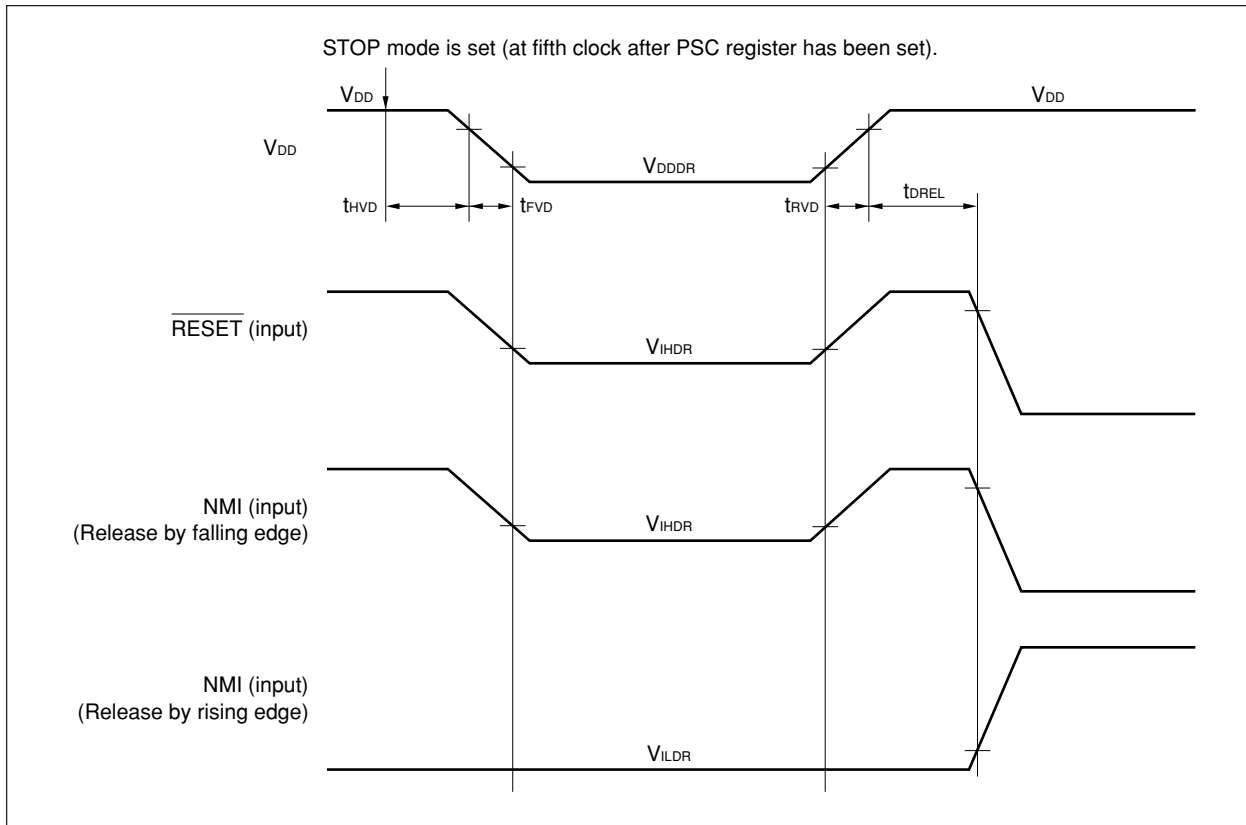
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Data hold voltage	V _{DDDR}	STOP mode	1.5		5.5	V	
Data hold current	I _{DDDR}	μPD70F3003A, 70F3003A(A)	CESEL = 0, Note 1		0.4V _{DDDR}	50	μA
			CESEL = 0, Note 2		0.4V _{DDDR}	200	μA
		CESEL = 1, Note 1		6V _{DDDR}	200	μA	
		CESEL = 1, Note 2		6V _{DDDR}	500	μA	
	μPD70F3025A	CESEL = 0, Note 1		0.4V _{DDDR}	50	μA	
		CESEL = 0, Note 2		0.4V _{DDDR}	200	μA	
		CESEL = 1, Note 1		12V _{DDDR}	300	μA	
		CESEL = 1, Note 2		12V _{DDDR}	500	μA	
Supply voltage rise time	t _{RVD}		200			μs	
Supply voltage fall time	t _{FVD}		200			μs	
Supply voltage hold time (vs. STOP mode setting)	t _{HVD}		0			ms	
STOP mode release signal input time	t _{DREL}		0			ns	
Data hold input voltage, high	V _{IHDR}	Note 3	0.9V _{DDDR}		V _{DDDR}	V	
Data hold input voltage, low	V _{ILDR}	Note 3	0		0.1V _{DDDR}	V	

Notes 1. -40°C ≤ T_A ≤ +50°C

2. 50°C < T_A ≤ 85°C

3. P02 to P07, P12 to P17, P23, P24, P26, P27, P32 to P37, P112 to P117, RESET, NMI, MODE, X1, and their alternate-function pins.

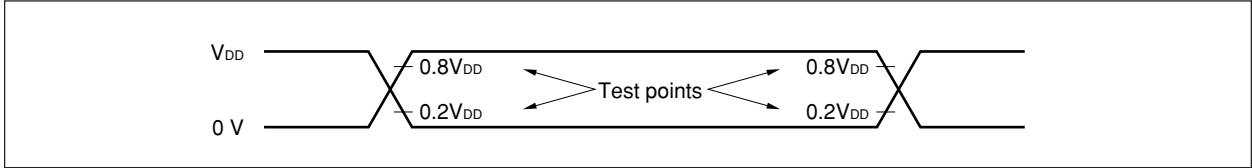
Remark TYP. values are reference values for when T_A = 25°C (except for the conditions in **Note 2**) and V_{DD} = 5.0 V.



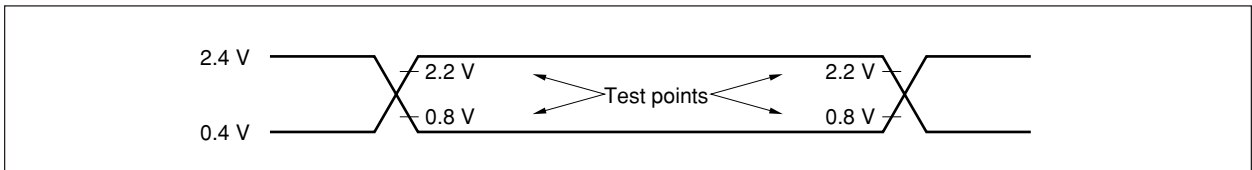
AC Characteristics ($T_A = -40$ to $+85^\circ\text{C}$, $V_{DD} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$)

AC test input test points

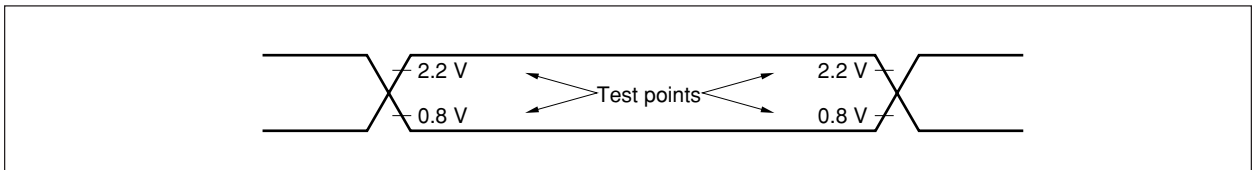
- (a) P02 to P07, P12 to P17, P23, P24, P26, P27, P32 to P37, P112 to P117, $\overline{\text{RESET}}$, NMI, MODE, X1, and their alternate-function pins



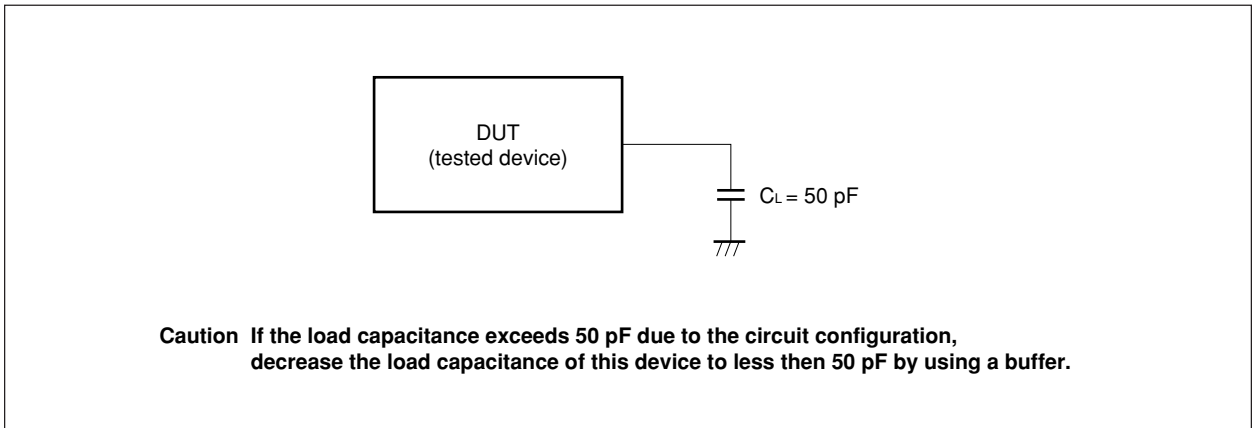
- (b) Other than (a)



AC test output test points



Load condition

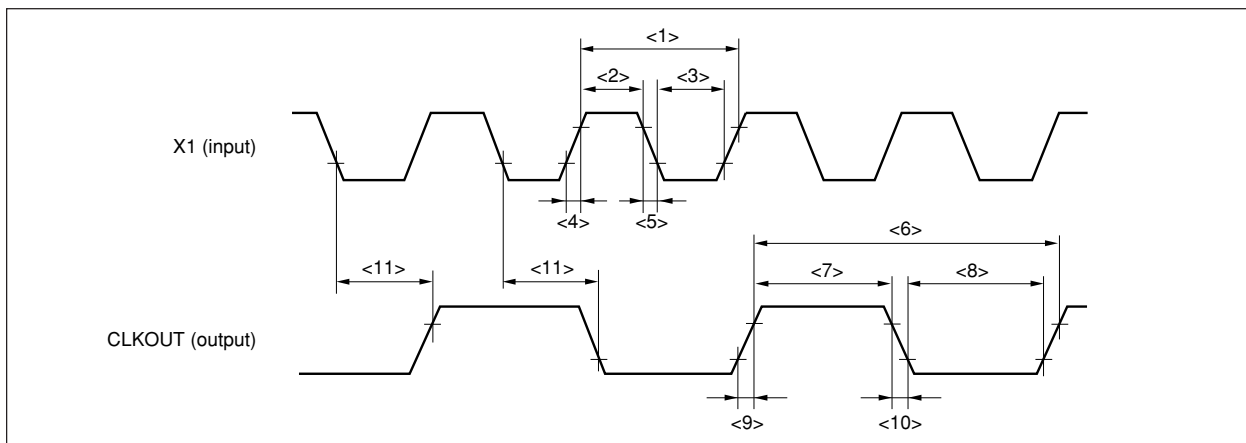


(1) Clock timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
X1 input cycle	<1> t _{CYX}	Direct mode	15	Note 1	ns
		PLL mode (PLL lock status)	151 ^{Note 2}	Note 3	ns
X1 input width, high	<2> t _{WXH}	Direct mode	6		ns
		PLL mode	60		ns
X1 input width, low	<3> t _{WXL}	Direct mode	6		ns
		PLL mode	60		ns
X1 input rise time	<4> t _{XR}	Direct mode		7	ns
		PLL mode		10	ns
X1 input fall time	<5> t _{XF}	Direct mode		7	ns
		PLL mode		10	ns
CPU operating frequency	— φ		Note 4	33	MHz
CLKOUT output cycle	<6> t _{CYK}		30	Note 5	ns
CLKOUT width, high	<7> t _{WKH}		0.5 T – 5		ns
CLKOUT width, low	<8> t _{WKL}		0.5 T – 5		ns
CLKOUT rise time	<9> t _{XR}			5	ns
CLKOUT fall time	<10> t _{XF}			5	ns
X1 ↓→ CLKOUT delay time	<11> t _{DXK}	Direct mode	3	17	ns

- Notes 1.** When A/D converter used: 100 ns
 When A/D converter not used: 250 ns
- 2.** When using A/D converter: The value when φ = 5 × f_{xx} and φ = f_{xx} are set. Setting φ = 1/2 × f_{xx} is prohibited.
 When not using A/D converter: The value when φ = 5 × f_{xx}, φ = f_{xx}, and φ = 1/2 × f_{xx} are set.
- 3.** When using A/D converter: 250 ns (when φ = 5 × f_{xx} is set) and 200 ns (when φ = f_{xx} is set). Setting φ = 1/2 × f_{xx} is prohibited.
 When not using A/D converter: 250 ns (when φ = 5 × f_{xx}, φ = f_{xx}, and φ = 1/2 × f_{xx} are set).
- 4.** When A/D converter used: 5 MHz
 When A/D converter not used: 2 MHz
- 5.** When A/D converter used: 200 ns
 When A/D converter not used: 500 ns

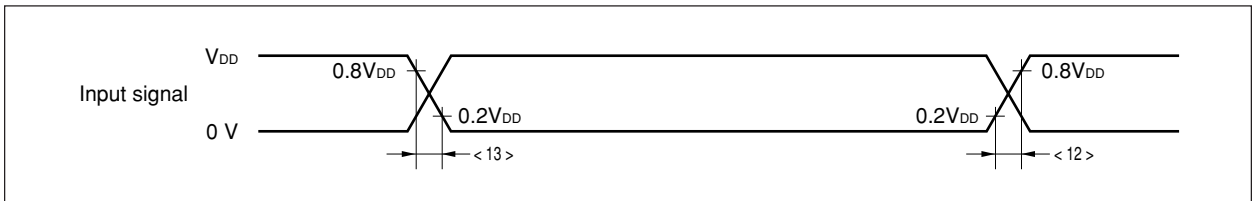
Remark T = t_{CYK}



(2) Input wave

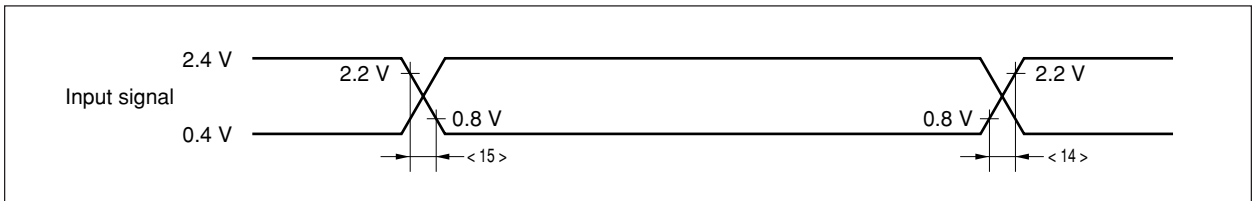
(a) P02 to P07, P12 to P17, P23, P24, P26, P27, P32 to P37, P112 to P117, RESET, NMI, MODE, and their alternate-function pins

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input rise time	<12> t_{IR2}			20	ns
Input fall time	<13> t_{IF2}			20	ns



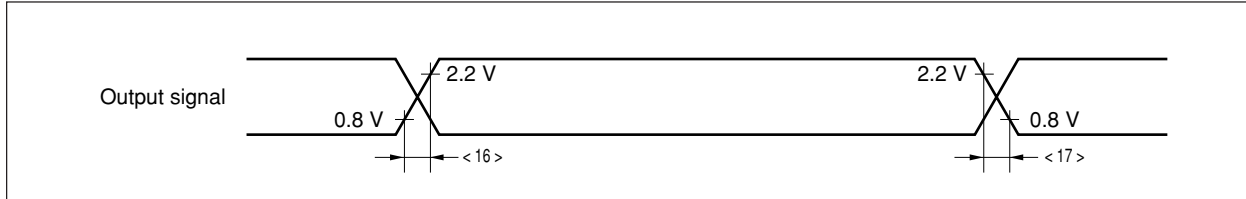
(b) Other than (a)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input rise time	<14> t_{IR1}			10	ns
Input fall time	<15> t_{IF1}			10	ns



(3) Output wave (other than CLKOUT)

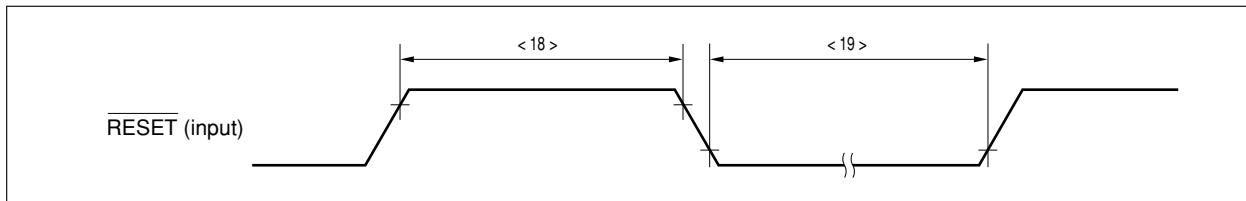
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Output rise time	<16> t _{OR}			10	ns
Output fall time	<17> t _{OF}			10	ns



(4) Reset timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ width, high	<18> t _{WRSH}		500		ns
$\overline{\text{RESET}}$ width, low	<19> t _{WRSL}	On power application, or on releasing STOP mode	500 + T _{OST}		ns
		Except on power application, or except on releasing STOP mode	500		ns

Remark T_{OST}: Oscillation stabilization time



(5) Read timing (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<20> tDKA		3	20	ns
Delay time from CLKOUT↑ to R \bar{W} , \bar{UBEN} , \bar{LBEN}	<78> tDKA2		-2	+13	ns
Delay time from CLKOUT↑ to address float	<21> tFKA		3	15	ns
Delay time from CLKOUT↓ to ASTB	<22> tDKST		3	15	ns
Delay time from CLKOUT↓ to \bar{DSTB}	<23> tDKD		3	15	ns
Data input setup time (to CLKOUT↑)	<24> tSIDK		5		ns
Data input hold time (from CLKOUT↑)	<25> tHKID		5		ns
\bar{WAIT} setup time (to CLKOUT↓)	<26> tSWTK		5		ns
\bar{WAIT} hold time (from CLKOUT↓)	<27> tHKWT		5		ns
Address hold time (from CLKOUT↑)	<28> tHKA		0		ns
Address setup time (to ASTB↓)	<29> tSAST	-40°C ≤ T _A ≤ +70°C	0.5 T - 10		ns
		70°C < T _A ≤ 85°C	0.5 T - 12		ns
Address hold time (from ASTB↓)	<30> tHSTA		0.5 T - 10		ns
Delay time from \bar{DSTB} ↓ to address float	<31> tFDA			0	ns
Data input setup time (to address)	<32> tSAID	-40°C ≤ T _A ≤ +70°C		(2 + n) T - 22	ns
		70°C < T _A ≤ 85°C		(2 + n) T - 25	ns
Data input setup time (to \bar{DSTB} ↓)	<33> tSDID	-40°C ≤ T _A ≤ +70°C		(1 + n) T - 20	ns
		70°C < T _A ≤ 85°C		(1 + n) T - 24	ns
Delay time from ASTB↓ to \bar{DSTB} ↓	<34> tDSTD		0.5 T - 10		ns
Data input hold time (from \bar{DSTB} ↑)	<35> tHDID		0		ns
Delay time from \bar{DSTB} ↑ to address output	<36> tDDA		(1 + i) T		ns
Delay time from \bar{DSTB} ↑ to ASTB↑	<37> tDDSTH		0.5 T - 10		ns
Delay time from \bar{DSTB} ↑ to ASTB↓	<38> tDDSTL		(1.5 + i) T - 10		ns
\bar{DSTB} low-level width	<39> tWDL	-40°C ≤ T _A ≤ +70°C	(1 + n) T - 10		ns
		70°C < T _A ≤ 85°C	(1 + n) T - 13		ns
ASTB high-level width	<40> tWSTH		T - 10		ns
\bar{WAIT} setup time (to address)	<41> tSAWT1	n ≥ 1, -40°C ≤ T _A ≤ +70°C		1.5 T - 20	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		1.5 T - 24	ns
	<42> tSAWT2	n ≥ 1, -40°C ≤ T _A ≤ +70°C		(1.5 + n) T - 20	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		(1.5 + n) T - 24	ns
\bar{WAIT} hold time (from address)	<43> tHAWT1	n ≥ 1	(0.5 + n) T		ns
	<44> tHAWT2	n ≥ 1	(1.5 + n) T		ns
\bar{WAIT} setup time (to ASTB↓)	<45> tSSTWT1	n ≥ 1, -40°C ≤ T _A ≤ +70°C		T - 18	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		T - 20	ns
	<46> tSSTWT2	n ≥ 1		(1 + n) T - 15	ns
\bar{WAIT} hold time (from ASTB↓)	<47> tHSTWT1	n ≥ 1	nT		ns
	<48> tHSTWT2	n ≥ 1	(1 + n) T		ns

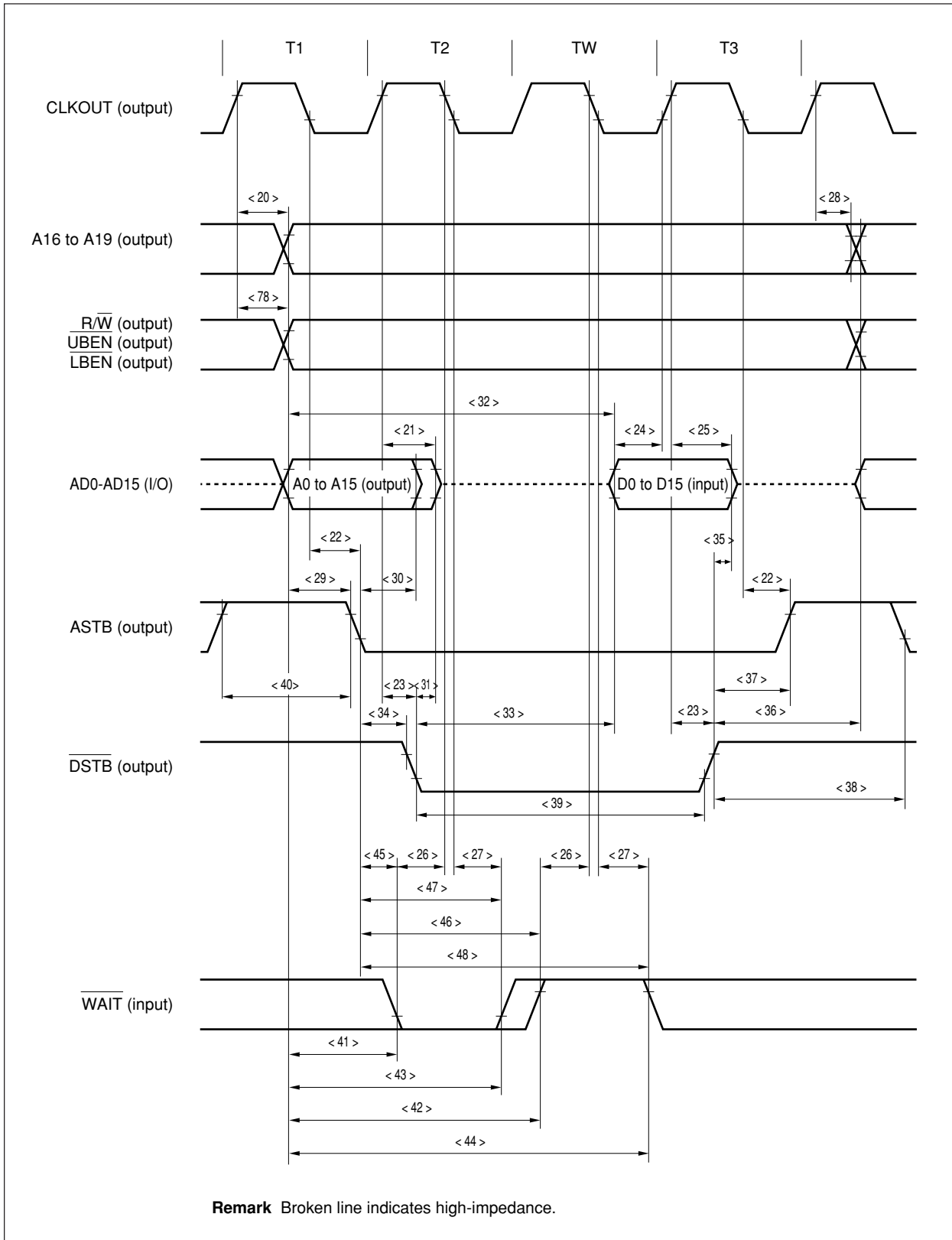
Remarks 1. T = t_{CLK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

3. i indicates the number of idle states (0 or 1) t be inserted in the read cycle.

4. Be sure to observe at least one of data input hold times t_{HKID} (<25>) and t_{HDID} (<35>).

(5) Read Timing (2/2): 1 wait



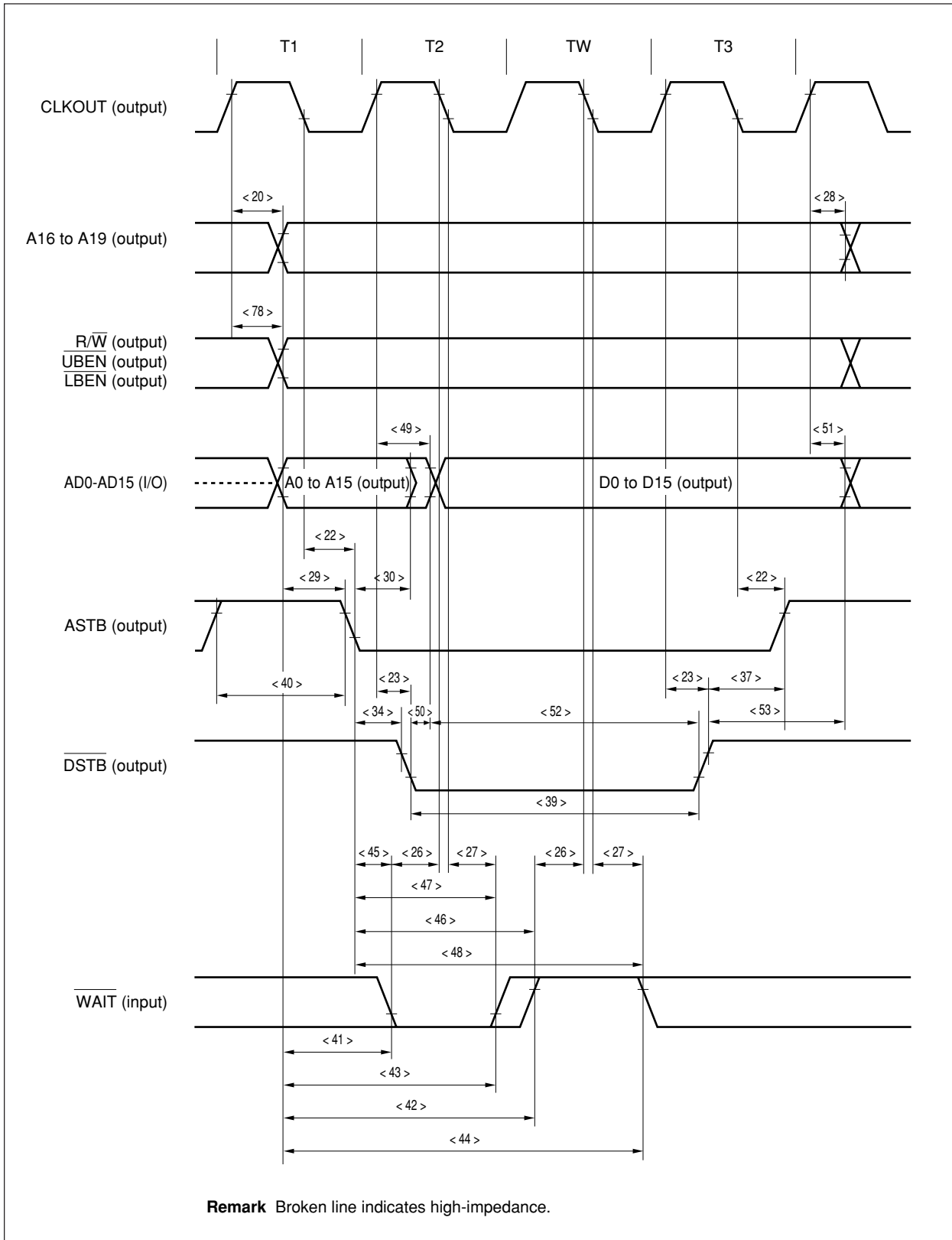
(6) Write timing (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	<20> tDKA		3	20	ns
Delay time from CLKOUT↑ to R \bar{W} , \bar{UBEN} , \bar{LBEN}	<78> tDKA2		-2	+13	ns
Delay time from CLKOUT↓ to ASTB	<22> tDKST		3	15	ns
Delay time from CLKOUT↑ to \bar{DSTB}	<23> tDKD		3	15	ns
\bar{WAIT} setup time (to CLKOUT↓)	<26> tSWTK		5		ns
\bar{WAIT} hold time (from CLKOUT↓)	<27> tHKWT		5		ns
Address hold time (from CLKOUT↑)	<28> tHKA		0		ns
Address setup time (to ASTB↓)	<29> tSAST	-40°C ≤ T _A ≤ +70°C	0.5 T - 10		ns
		70°C < T _A ≤ 85°C	0.5 T - 12		ns
Address hold time (from ASTB↓)	<30> tHSTA		0.5 T - 10		ns
Delay time from ASTB↓ to \bar{DSTB} ↓	<34> tDSTD		0.5 T - 10		ns
Delay time from \bar{DSTB} ↑ to \bar{ASTB} ↑	<37> tDDSTH		0.5 T - 10		ns
\bar{DSTB} low-level width	<39> tWDL	-40°C ≤ T _A ≤ +70°C	(1 + n) T - 10		ns
		70°C < T _A ≤ 85°C	(1 + n) T - 13		ns
\bar{ASTB} high-level width	<40> tWSTH		T - 10		ns
\bar{WAIT} setup time (to address)	<41> tSAWT1	n ≥ 1, -40°C ≤ T _A ≤ +70°C		1.5 T - 20	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		1.5 T - 24	ns
	<42> tSAWT2	n ≥ 1, -40°C ≤ T _A ≤ +70°C		(1.5 + n) T - 20	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		(1.5 + n) T - 24	ns
\bar{WAIT} hold time (from address)	<43> tHAWT1	n ≥ 1	(0.5 + n) T		ns
	<44> tHAWT2	n ≥ 1	(1.5 + n) T		ns
\bar{WAIT} setup time (to ASTB↓)	<45> tSSTWT1	n ≥ 1, -40°C ≤ T _A ≤ +70°C		T - 18	ns
		n ≥ 1, 70°C < T _A ≤ 85°C		T - 20	ns
	<46> tSSTWT2	n ≥ 1		(1 + n) T - 15	ns
\bar{WAIT} hold time (from ASTB↓)	<47> tHSTWT1	n ≥ 1	nT		ns
	<48> tHSTWT2	n ≥ 1	(1 + n) T		ns
Address hold time (from CLKOUT↑)	<49> tDKOD	-40°C ≤ T _A ≤ +70°C		20	ns
		70°C < T _A ≤ 85°C		23	ns
Delay time from \bar{DSTB} ↓ to data output	<50> tDDOD			10	ns
Data output hold time (from CLKOUT↑)	<51> tHKOD		0		ns
Data output setup time (to \bar{DSTB} ↑)	<52> tSODD		(1 + n) T - 15		ns
Data output hold time (from \bar{DSTB} ↑)	<53> tHDOD		T - 10		ns

Remarks 1. T = t_{CYK}

- n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(6) Write timing (2/2): 1 wait



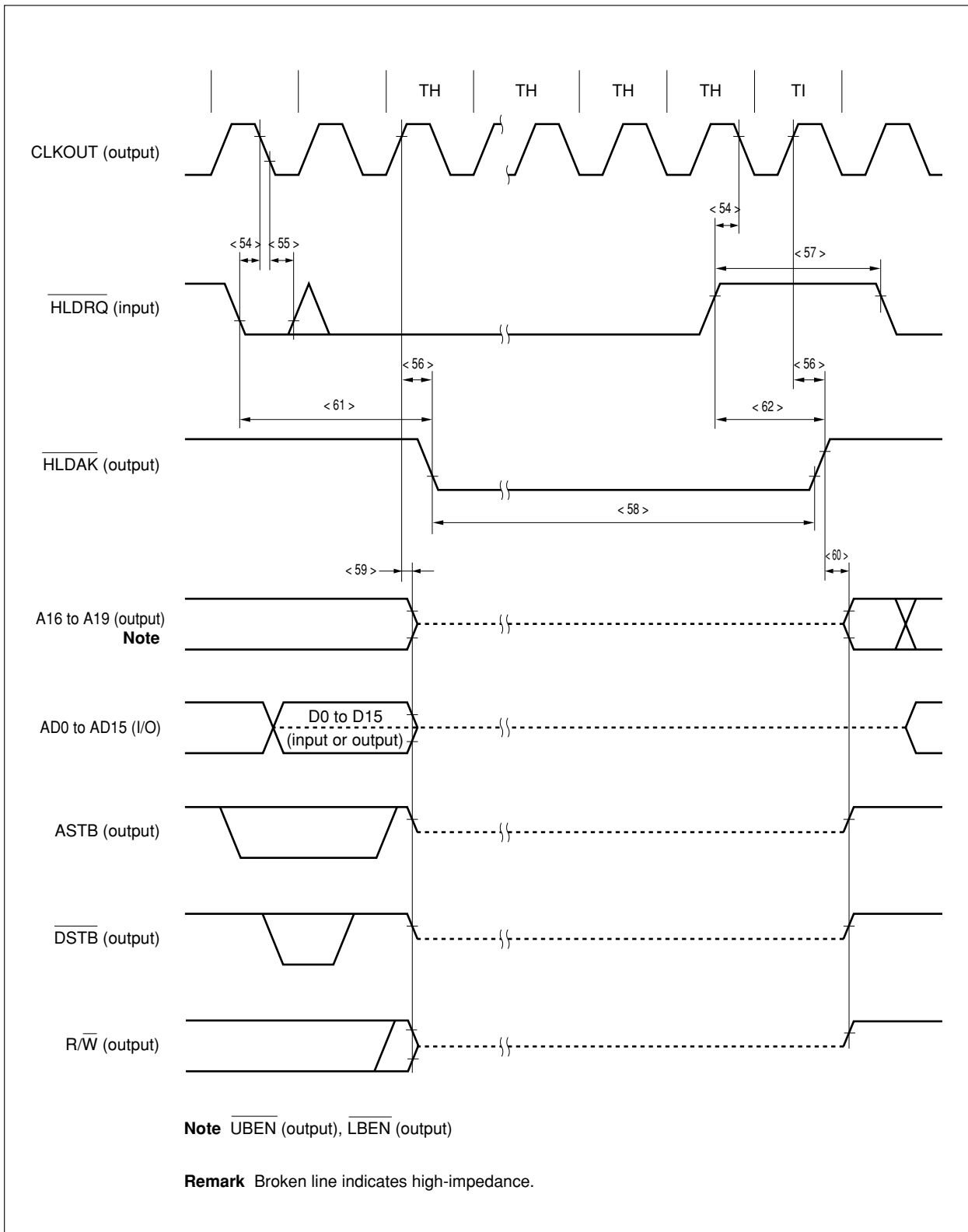
(7) Bus hold timing (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT↓)	<54> t_{SHOK}		5		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT↓)	<55> t_{HKHQ}		5		ns
Delay time from $\overline{\text{HLDAK}}$ to CLKOUT↑	<56> t_{DKHA}			20	ns
$\overline{\text{HLDRQ}}$ high-level width	<57> t_{WHQH}		T + 10		ns
$\overline{\text{HLDAK}}$ low-level width	<58> t_{WHAL}	$-40^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$	T - 10		ns
		$70^{\circ}\text{C} < T_A \leq 85^{\circ}\text{C}$	T - 12		ns
Delay time from CLKOUT↑ to bus float	<59> t_{DKF}			20	ns
Delay time from $\overline{\text{HLDAK}}$ ↑ to bus output	<60> t_{DHAC}		-3		ns
Delay time from $\overline{\text{HLDRQ}}$ ↓ to $\overline{\text{HLDAK}}$ ↓	<61> t_{DHQA1}			(2 n + 7.5) T + 20	ns
Delay time from $\overline{\text{HLDRQ}}$ ↑ to $\overline{\text{HLDAK}}$ ↑	<62> t_{DHQA2}		0.5 T	1.5 T + 20	ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

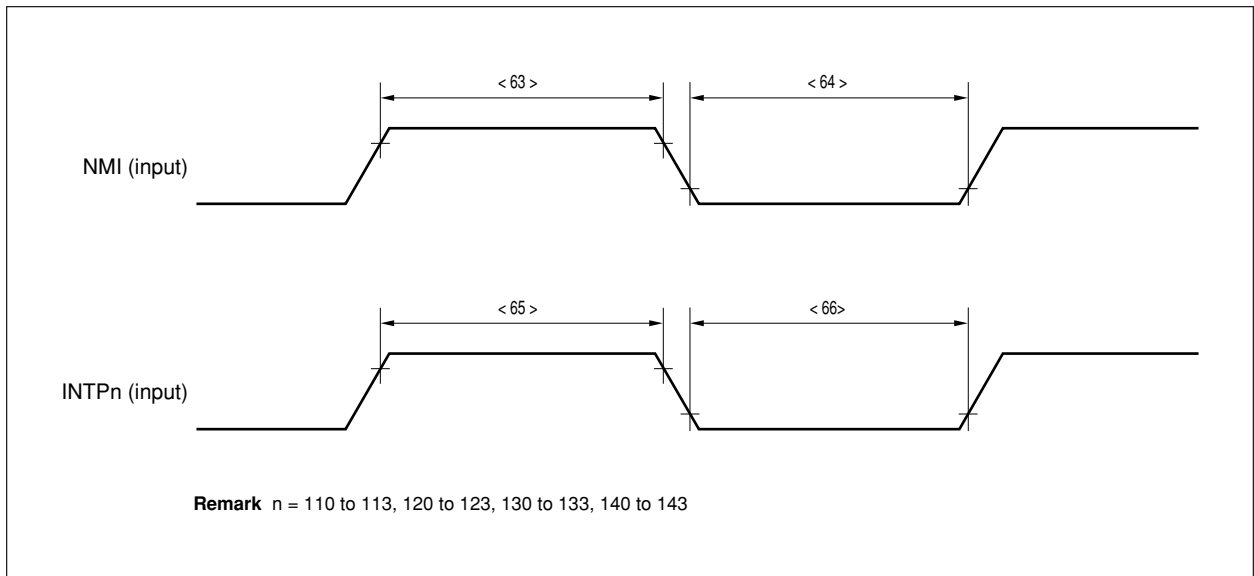
(7) Bus hold timing (2/2)



(8) Interrupt timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI width, high	<63> t_{WNH}		500		ns
NMI width, low	<64> t_{WNL}		500		ns
INTPn width, high	<65> t_{WITH}	n = 110 to 113, 120 to 123, 130 to 133, 140 to 143	3 T + 10		ns
INTPn width, low	<66> t_{WITL}	n = 110 to 113, 120 to 123, 130 to 133, 140 to 143	3 T + 10		ns

Remark T = t_{CYK}



(9) CSI timing (1/2)

(a) Master mode

(i) CSI0 to CSI2 timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
\overline{SCKn} cycle	<67> t_{CYSK1}	Output	120		ns
\overline{SCKn} high-level width	<68> t_{WSKH1}	Output	$0.5 t_{CYSK1} - 20$		ns
\overline{SCKn} low-level width	<69> t_{WSKL1}	Output	$0.5 t_{CYSK1} - 20$		ns
SIn setup time (to $\overline{SCKn}\uparrow$)	<70> t_{SSISK1}		30		ns
SIn hold time (from $\overline{SCKn}\uparrow$)	<71> t_{HSKS11}		0		ns
SOn output delay time (from $\overline{SCKn}\downarrow$)	<72> t_{DSKS01}			18	ns
SOn output hold time (from $\overline{SCKn}\uparrow$)	<73> t_{HSKS01}		$0.5 t_{CYSK1} - 5$		ns

Remark n = 0 to 2

(ii) CSI3 timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	
$\overline{SCK3}$ cycle	<67> t_{CYSK3}	Output	$R_L = 1.5$ $k\Omega$ $C_L = 50$ pF		ns	
$\overline{SCK3}$ high-level width	<68> t_{WSKH3}	Output		$0.5 t_{CYSK3} - 70$		ns
$\overline{SCK3}$ low-level width	<69> t_{WSKL3}	Output		$0.5 t_{CYSK3} - 70$		ns
SI3 setup time (to $\overline{SCK3}\uparrow$)	<70> t_{SSISK3}		100		ns	
SI3 hold time (from $\overline{SCK3}\uparrow$)	<71> t_{HSKSI3}		50		ns	
SO3 output delay time (from $\overline{SCK3}\downarrow$)	<72> t_{DSKS03}	$R_L = 1.5 K\Omega$ $C_L = 50 pF$		150	ns	
SO3 output hold time (from $\overline{SCK3}\uparrow$)	<73> t_{HSKS03}		$0.5 t_{CYSK3} - 5$		ns	

Remark R_L and C_L are the load resistance and load capacitance respectively of the $\overline{SCK3}$ and SO3 output lines.

(b) Slave mode

(i) CSI0 to CSI2 timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
\overline{SCKn} cycle	<67> t_{CYSK2}	Input	120		ns
\overline{SCKn} high-level width	<68> t_{WSKH2}	Input	30		ns
\overline{SCKn} low-level width	<69> t_{WSKL2}	Input	30		ns
SIn setup time (to $\overline{SCKn}\uparrow$)	<70> t_{SSISK2}		10		ns
SIn hold time (from $\overline{SCKn}\uparrow$)	<71> t_{HSKSI2}		10		ns
SOn output delay time (from $\overline{SCKn}\downarrow$)	<72> t_{DSKS02}			30	ns
SOn output hold time (from $\overline{SCKn}\uparrow$)	<73> t_{HSKS02}		t_{WSKH2}		ns

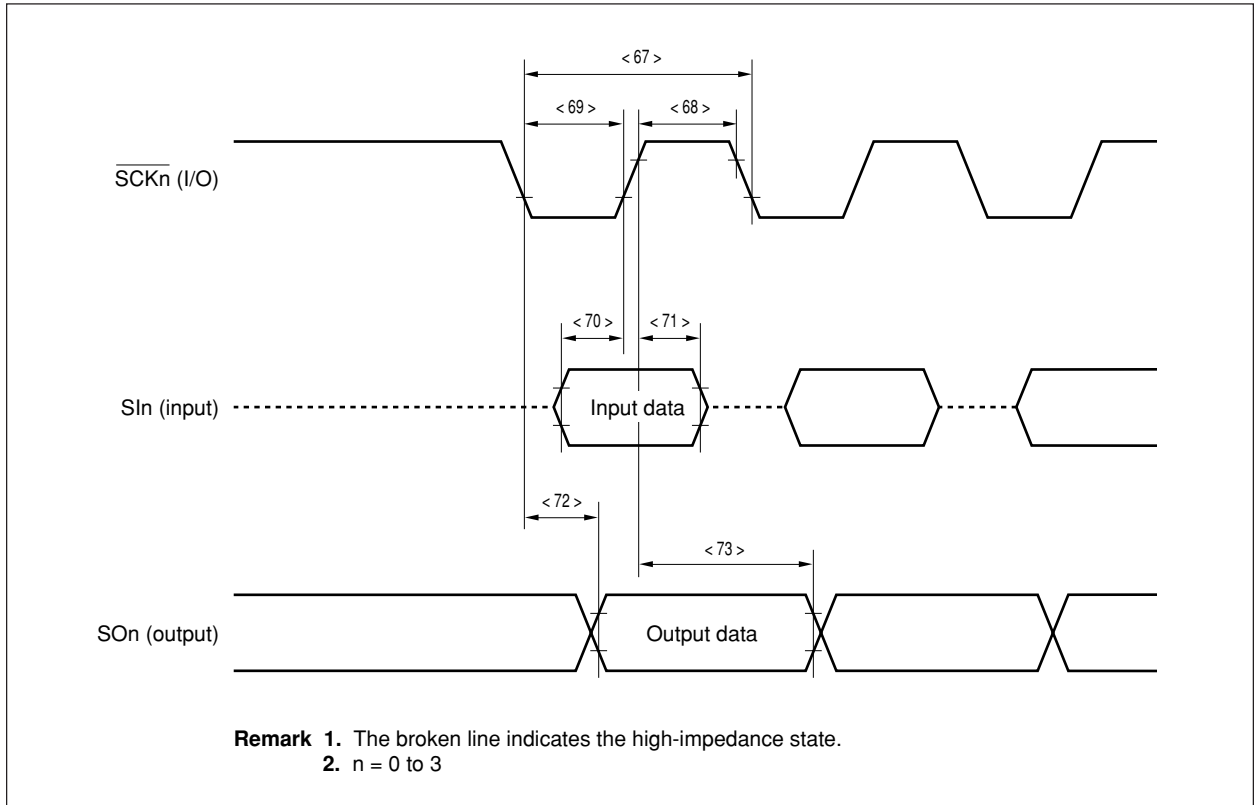
Remark n = 0 to 2

(9) CSI timing (2/2)

(ii) CSI3 timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCK3}$ cycle	<67> t_{CYSK4}	Input	500		ns
$\overline{SCK3}$ high-level width	<68> t_{WSKH4}	Input	180		ns
$\overline{SCK3}$ low-level width	<69> t_{WSKL4}	Input	180		ns
SI3 setup time (to $\overline{SCK3}\uparrow$)	<70> t_{SSISK4}		100		ns
SI3 hold time (from $\overline{SCK3}\uparrow$)	<71> t_{HSKSI4}		50		ns
SO3 output delay time (from $\overline{SCK3}\downarrow$)	<72> t_{DSKSO4}	$R_L = 1.5\text{ k}\Omega$		150	ns
SO3 output hold time (from $\overline{SCK3}\uparrow$)	<73> t_{HSKSO4}	$C_L = 50\text{ pF}$	t_{WSKH4}		ns

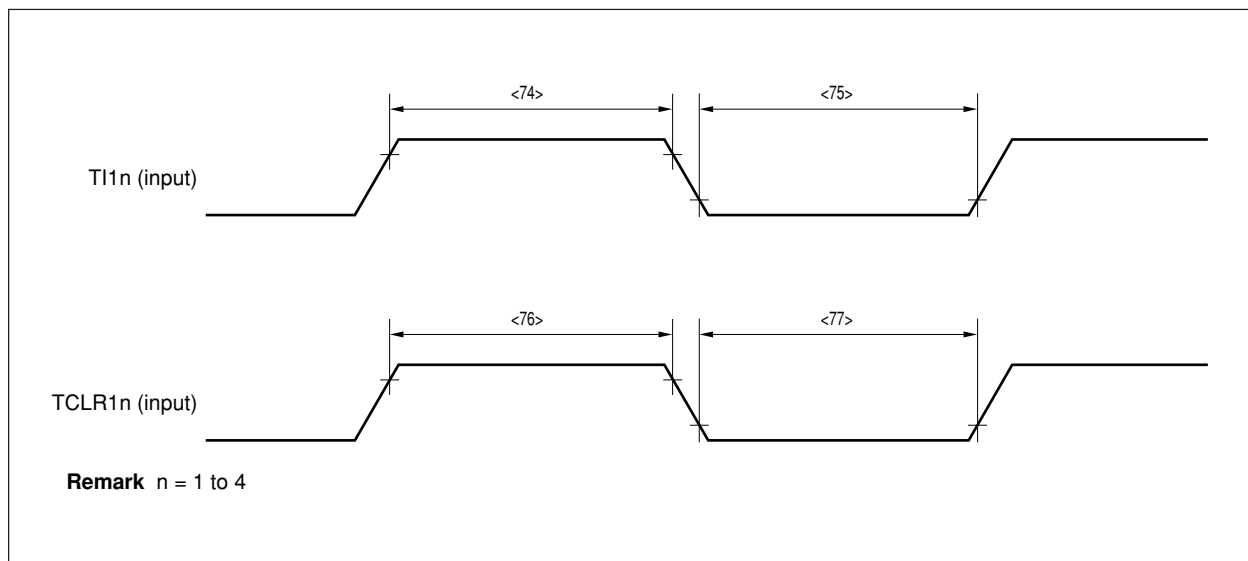
Remark R_L and C_L are the load resistance and load capacitance respectively of the $\overline{SCK3}$ and SO3 output lines.



(10) RPU timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Tl1n high-level width	<74> t_{WTH}		$3 T + 10$		ns
Tl1n low-level width	<75> t_{WTL}		$3 T + 10$		ns
TCLR1n high-level width	<76> t_{WCH}		$3 T + 10$		ns
TCLR1n low-level width	<77> t_{WCL}		$3 T + 10$		ns

Remark $T = t_{CYK}$



A/D Converter Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 5 V ±10%, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	—		10	10	10	bit
Overall error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}			±0.4	%FSR
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}			±0.7	%FSR
Quantization error	—				±1/2	LSB
Conversion time	t _{CONV}	4.5 V ≤ AV _{REF1} ≤ AV _{DD}	60			t _{cyk}
		3.5 V ≤ AV _{REF1} ≤ AV _{DD}	60			t _{cyk}
Sampling time	t _{SAMP}	4.5 V ≤ AV _{REF1} ≤ AV _{DD}	10			t _{cyk}
		3.5 V ≤ AV _{REF1} ≤ AV _{DD}	10			t _{cyk}
Zero-scale error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±3.5	LSB
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5	LSB
Full-scale error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±2.5	LSB
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5	LSB
Non-linearity error ^{Note 1}	—	4.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±2.5	LSB
	—	3.5 V ≤ AV _{REF1} ≤ AV _{DD}		±1.5	±4.5	LSB
Analog input voltage ^{Note 2}	V _{IAN}		-0.3		AV _{DD} + 0.3	V
Reference voltage	AV _{REF1}		3.5		AV _{DD}	V
AV _{REF1} current	I _{REF1}			1.2	3.0	mA
AV _{DD} supply current	I _{DD}			2.3	6.0	mA

- Notes**
1. Except quantization error.
 2. The conversion result is 000H when V_{IAN} = 0.
 Converted with 10-bit resolution when 0 < V_{IAN} < AV_{REF1}.
 The conversion result is 3FFH when AV_{REF1} ≤ V_{IAN} ≤ AV_{DD}.

D/A Converter Characteristics (T_A = -40 to +85°C, V_{DD} = AV_{DD} = 5 V ±10%, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	—		8	8	8	bit
Overall error	—	Load conditions: 2 MΩ, 30 pF AV _{REF2} = V _{DD} AV _{REF3} = 0			0.8	%
	—	Load conditions: 2 MΩ, 30 pF AV _{REF2} = 0.75 V _{DD} AV _{REF3} = 0.25 V _{DD}			1.0	%
	—	Load conditions: 4 MΩ, 30 pF AV _{REF2} = V _{DD} AV _{REF3} = 0			0.6	%
	—	Load conditions: 4 MΩ, 30 pF AV _{REF2} = 0.75 V _{DD} AV _{REF3} = 0.25 V _{DD}			0.8	%
Settling time	—	Load conditions: 2 MΩ, 30 pF			10	μs
Output resistance	RO			8		kΩ
AV _{REF2} input voltage	AV _{REF2}		0.75V _{DD}		V _{DD}	V
AV _{REF3} input voltage	AV _{REF3}		0		0.25V _{DD}	V
Resistance between AV _{REF2} and AV _{REF3}	R _{AIREF}	DACS0, DACS1 = 55H	2	4		kΩ

3.2 Flash Memory Programming Mode

Basic Characteristics (T_A = 10 to 40°C (when rewriting), T_A = -40 to +85°C (when not rewriting), V_{DD} = AV_{DD} = 5 V ±10%, V_{SS} = AV_{SS} = 0 V)

(1) μPD70F3003A (all ranks), 70F3025A (except K, E, P, X rank)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	φ		10		33	MHz
V _{PP} supply voltage	V _{PP1}	During flash memory programming	9.7	10.3	10.6	V
	V _{PP_L}	V _{PP} low-level detection	-0.5		0.2V _{DD}	V
	V _{PP_M}	V _{PP} , V _{DD} level detection	0.8V _{DD}		1.2V _{DD}	V
	V _{PP_H}	V _{PP} high-voltage level detection	9.7	10.3	10.6	V
V _{DD} supply current	I _{DO}	V _{PP} = V _{PP1}			3.0 × φ + 25	mA
V _{PP} supply current	I _{PP}	V _{PP} = 10.3 V			200	mA
Step erase time	t _{ER}	Note 1		0.2		s
Overall erase time per area	t _{ERA}	When the step erase time = 0.2 s, Note 2			40	s/area
Write-back time	t _{WB}	Note 3		5		ms
Number of write-backs per write-back command	C _{WB}	When the write-back time = 5 ms, Note 4			50	Count/write-back command
Number of erase/write-backs	C _{ERWB}				16	Count
Step writing time	t _{WT}	Note 5		50		μs
Overall writing time per word	t _{WTW}	When the step writing time = 50 μs (1 word = 4 bytes), Note 6	50		500	μs/word
Number of rewrites per area	C _{ERWR}	1 erase + 1 write after erase = 1 rewrite, Note 7	20			Count/area

- Notes**
- The recommended setting value of the step erase time is 0.2 s.
 - The prewrite time prior to erasure and the erase verify time (write-back time) are not included.
 - The recommended setting value of the step erase time is 5 ms.
 - Write-back is executed once by the issuance of the write-back command. Therefore, the retry count must be the maximum value minus the number of commands issued.
 - The recommended setting value of the step writing time is 50 μs.
 - 100 μs is added to the actual writing time per word. The internal verify time during and after the writing is not included.
 - When writing initially to shipped products, it is counted as one rewrite for both “erase to write” and “write only”.

Example (P: Write, E: Erase)

Shipped product → P → E → P → E → P: 3 rewrites
 Shipped product → E → P → E → P → E → P: 3 rewrites

- Cautions**
1. V_{PP} pull-down resistance value (RV_{PP}) is recommended to be in the range 5 k Ω to 15 k Ω .
 2. Set the transfer rate between programmer and device as follows.
CSI0: 0.2 to 1 MHz
UART0: 4,800 to 76,800 bps

- Remarks**
1. When the PG-FP3 is used, a time parameter required for writing/erasing by downloading parameter files is automatically set. Do not change the settings unless otherwise specified.
 2. Area 0 = 00000H to 1FFFFH, area 1 = 20000H to 3FFFFH (area 1 is provided in the μ PD70F3025A only)
 3. The rank is indicated by the 5th character from the left in the lot number.
 4. The I rank applies to engineering samples (ES) only. The operation of an ES is not guaranteed.
 5. ϕ : Internal system clock frequency

(2) μPD70F3025A (X rank)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	ϕ	Note 1	10		33	MHz
V _{PP} supply voltage	V _{PP1}	During flash memory programming	9.7	10.3	10.6	V
	V _{PPL}	V _{PP} low-level detection	-0.5		0.2V _{DD}	V
	V _{PPM}	V _{PP} , V _{DD} level detection	0.8V _{DD}		1.2V _{DD}	V
	V _{PPH}	V _{PP} high-voltage level detection	9.7	10.3	10.6	V
V _{DD} supply current	I _{DD}	V _{PP} = V _{PP1}			3.0 × ϕ + 25	mA
V _{PP} supply current	I _{PP}	V _{PP} = 10.3 V			200	mA
Step erase time	t _{ER}	Note 1		2		s
Overall erase time per area	t _{ERA}	When the step erase time = 2 s, Note 2			40	s/area
Step writing time	t _{WT}	Note 3		200		μs
Overall writing time per word	t _{WTW}	When the step writing time = 200 μs (1 word = 4 bytes), Note 4	200		2000	μs/word
Number of rewrites per area	C _{ERWR}	1 erase + 1 write after erase = 1 rewrite, Note 5	20			Count/area

- Notes 1.** The recommended setting value of the step erase time is 2 s.
- 2.** The prewrite time prior to erasure and the erase verify time (write-back time) are not included.
- 3.** The recommended setting value of the step writing time is 200 μs.
- 4.** 100 μs is added to the actual writing time per word. The internal verify time during and after the writing is not included.
- 5.** When writing initially to shipped products, it is counted as one rewrite for both “erase to write” and “write only”.

Example (P: Write, E: Erase)

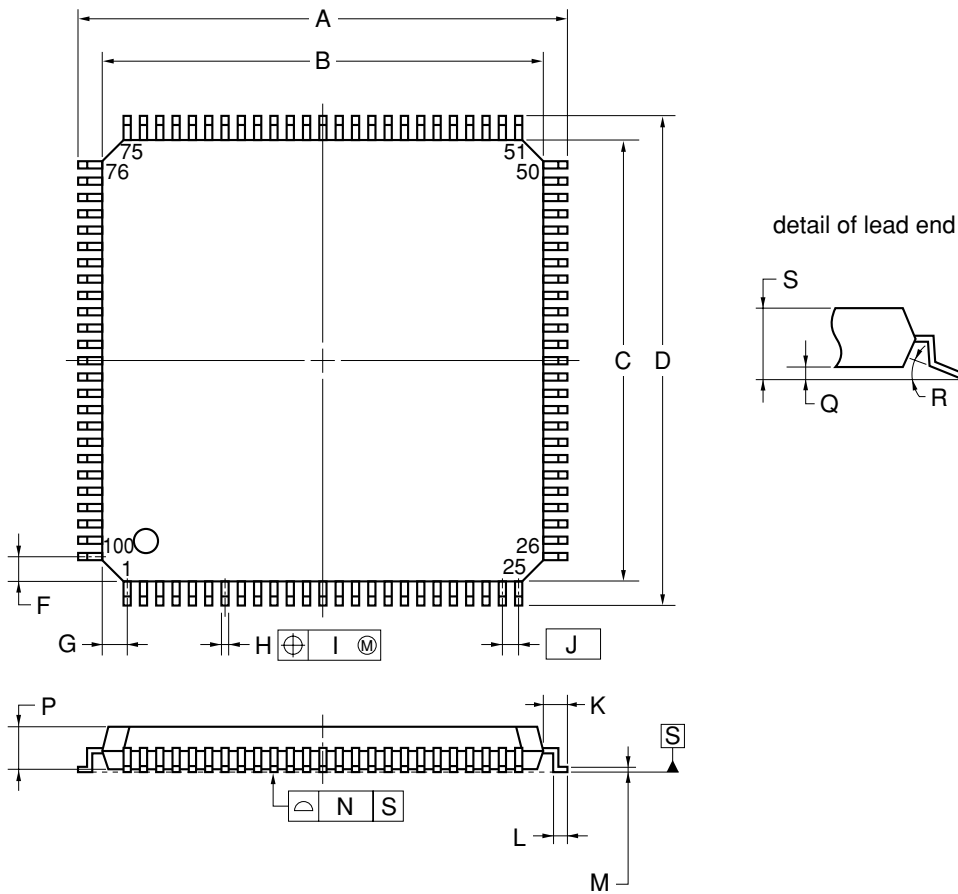
Shipped product → P → E → P → E → P: 3 rewrites
 Shipped product → E → P → E → P → E → P: 3 rewrites

- Cautions 1.** V_{PP} pull-down resistance value (RV_{PP}) is recommended to be in the range 5 kΩ to 15 kΩ.
- 2.** Set the transfer rate between programmer and device as follows.
- CSI0: 0.2 to 1 MHz**
UART0: 4,800 to 76,800 bps

- Remarks 1.** When the PG-FP3 is used, a time parameter required for writing/erasing by downloading parameter files is automatically set. Do not change the settings unless otherwise specified.
- 2.** Area 0 = 00000H to 1FFFFH, area 1 = 20000H to 3FFFFH
- 3.** The rank is indicated by the 5th character from the left in the lot number.
- 4.** The K, E, P, and X rank products do not support handshake mode. The I rank applies to engineering samples (ES) only. The operation of an ES is not guaranteed.
- 5.** ϕ : Internal system clock frequency

★ 4. PACKAGE DRAWING

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	0.22 ^{+0.05} _{-0.04}
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	0.17 ^{+0.03} _{-0.07}
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	3° ^{+7°} _{-3°}
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

5. RECOMMENDED SOLDERING CONDITIONS

The μPD70F3003A, 70F3025A, and 70F3003A(A) should be soldered and mounted under the following recommended conditions.

For technical information, see the following website.

Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)

Table 5-1. Surface Mounting Type Soldering Conditions

- (1) μPD70F3003AGC-33-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
- μPD70F3025AGC-33-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Three times or less, Exposure limit: 3 days ^{Note} (after that, prebake at 125°C for 10 to 72 hours)	IR35-103-3
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Three times or less, Exposure limit: 3 days ^{Note} (after that, prebake at 125°C for 10 to 72 hours)	VP15-103-3
Partial heating	Pin temperature: 300°C max., Time 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remark For soldering methods and conditions other than those recommended above, consult an NEC Electronics sales representative.

- ★ (2) μPD70F3003AGC-33-8EU-A: 100-pin plastic LQFP (fine pitch) (14 × 14)
- μPD70F3025AGC-33-8EU-A: 100-pin plastic LQFP (fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds max. (at 220°C or higher), Count: Three times or less, Exposure limit: 7 days ^{Note} (after that, prebake at 125°C for 20 to 72 hours)	IR60-207-3
Wave soldering	For details, consult an NEC Electronics sales representative.	—
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

- Remarks**
1. Products with -A at the end of the part number are lead-free products.
 2. For soldering methods and conditions other than those recommended above, consult an NEC Electronics sales representative.

★ (3) μPD70F3003AGC(A)-33-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 3 days ^{Note} (after that, prebake at 125°C for 10 to 72 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Two times or less, Exposure limit: 3 days ^{Note} (after that, prebake at 125°C for 10 to 72 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time 3 seconds max. (per pin row)	—

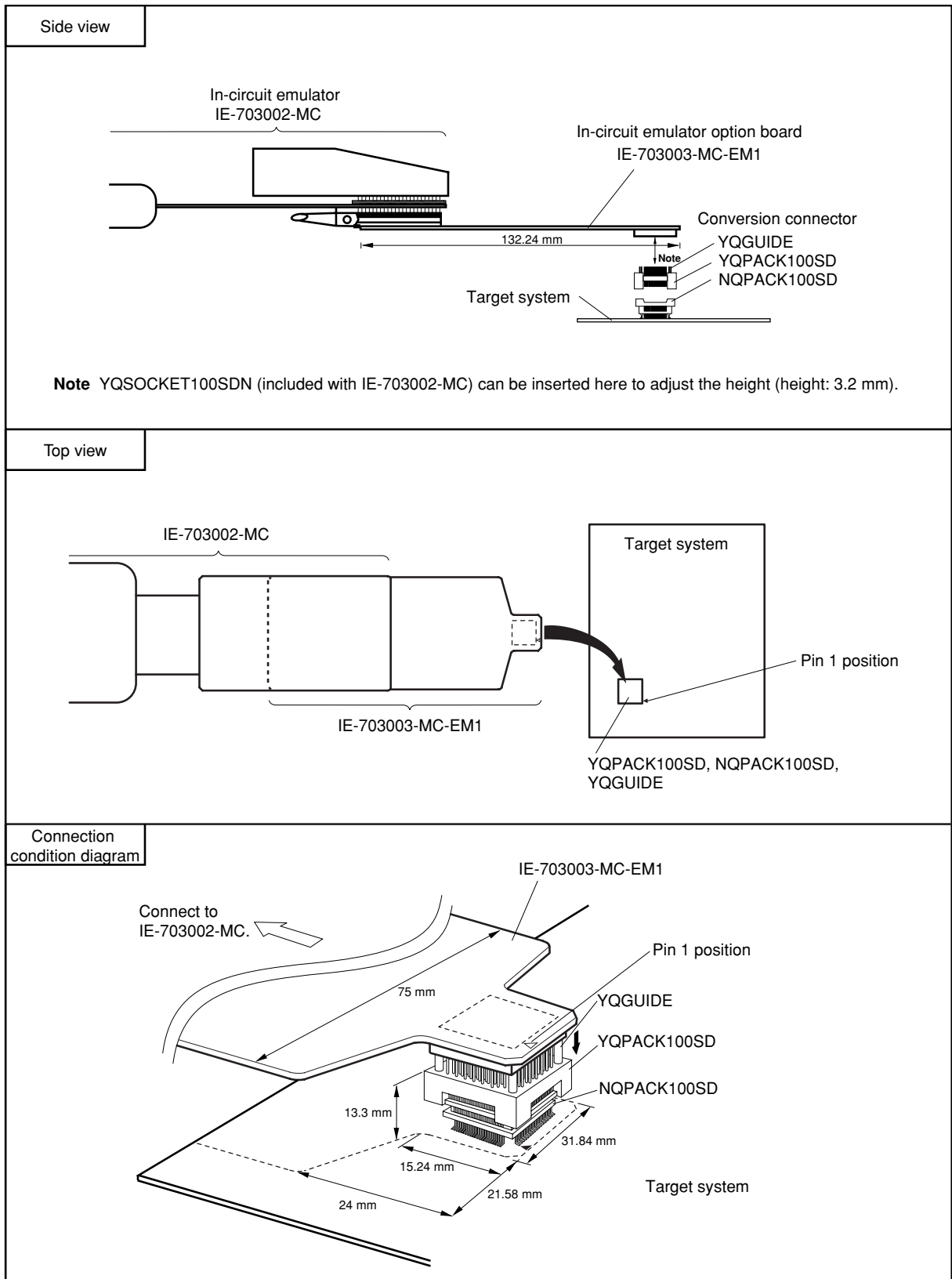
Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remark For soldering methods and conditions other than those recommended above, consult an NEC Electronics sales representative.

★ APPENDIX NOTES ON TARGET SYSTEM DESIGN

The following shows a diagram of the connection conditions between the in-circuit emulator option board and conversion connector. Design your system making allowances for conditions such as the form of parts mounted on the target system as shown below.



NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Related document: μ PD703003A, 703004A, 703025A, 703003A(A), 703025A(A) Data Sheet (U13188E)

Reference Materials Electrical Characteristics for Microcomputer (U15170J^{Note})

Note This document number is that of Japanese version.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC Electronics product in your application, please contact the NEC Electronics office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

[GLOBAL SUPPORT]

<http://www.necel.com/en/support/support.html>

NEC Electronics America, Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782

NEC Electronics (Europe) GmbH
Duesseldorf, Germany
Tel: 0211-65030

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318

- **Sucursal en España**
Madrid, Spain
Tel: 091-504 27 87

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-558-3737

- **Succursale Française**
Vélizy-Villacoublay, France
Tel: 01-30-67 58 00

NEC Electronics Shanghai Ltd.
Shanghai, P.R. China
Tel: 021-5888-5400

- **Filiale Italiana**
Milano, Italy
Tel: 02-66 75 41

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-2719-2377

- **Branch The Netherlands**
Eindhoven, The Netherlands
Tel: 040-265 40 10

NEC Electronics Singapore Pte. Ltd.
Novena Square, Singapore
Tel: 6253-8311

- **Tyskland Filial**
Taebby, Sweden
Tel: 08-63 87 200

- **United Kingdom Branch**
Milton Keynes, UK
Tel: 01908-691-133

- **The information in this document is current as of July, 2005. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality, reliability and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. To minimize risks of damage to property or injury (including death) to persons arising from defects in NEC Electronics products, customers must incorporate sufficient safety measures in their design, such as redundancy, fire-containment and anti-failure features.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific".

The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.

"Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.

"Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

"Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)

- (1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.
- (2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).