R2A20056BM

Lithium-Ion Battery Charger IC with Auto Load Current Distribution

R03DS0075EJ0100
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Description

R2A20056BM is a semiconductor integrated circuit designed for Lithium-ion battery charger control IC. Built-in Input current limitation circuit compliant with USB requirements and dual output (system and battery) control circuit allows to supply the system power and the battery charging power simultaneously from input power.

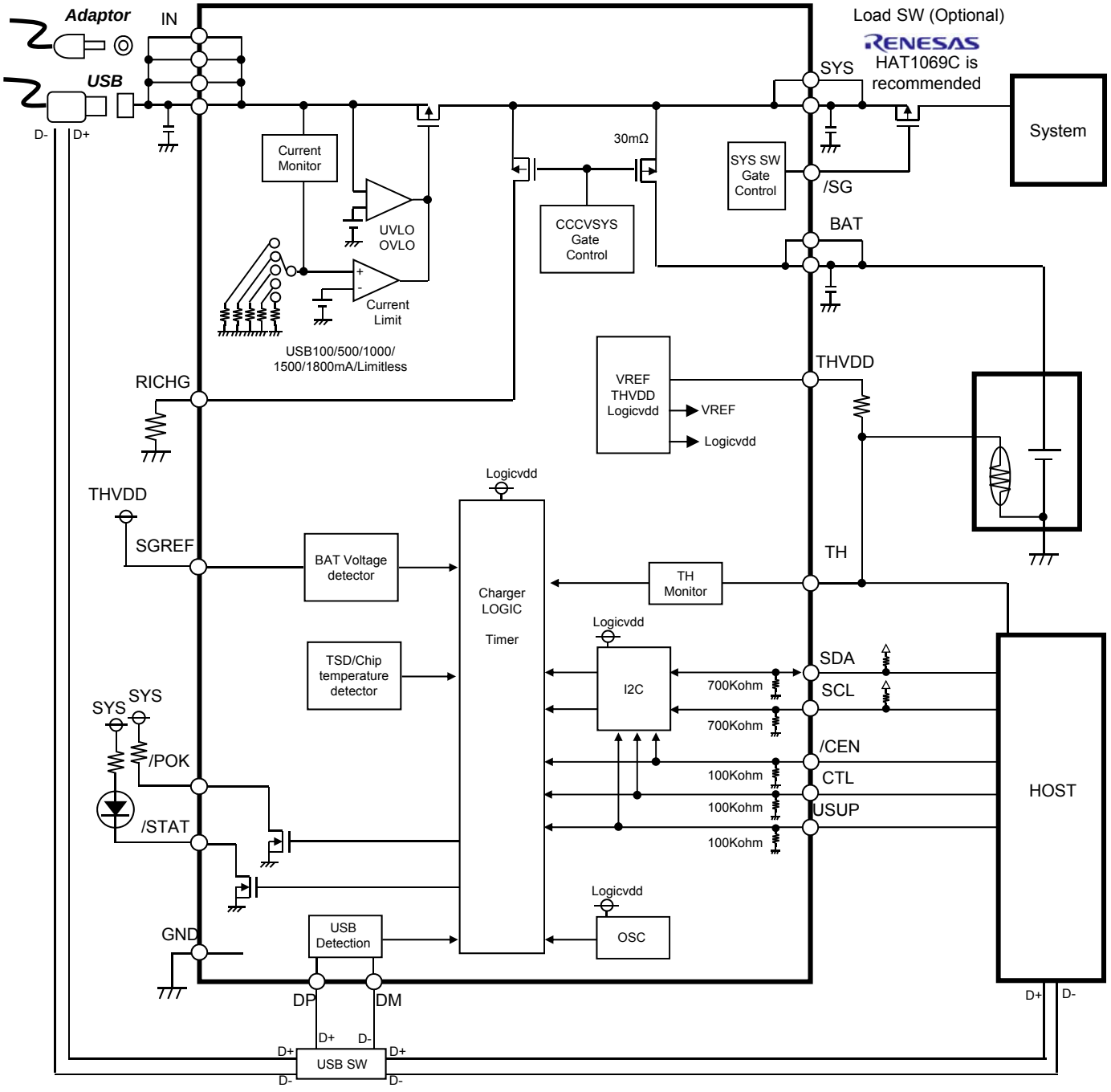
Features

- Allows to USB charging
  - Automatic USB detection and automatic input current limitation setup
    (USB battery charging 1.2 and VBUS divided port)
  - Input current limitation is programmable by I2C
    I^2C 100mA/500mA/1000mA/1500mA/1800mA/Limitless/Suspend
- Weak battery charge function
- High precision charge control voltage : 4.2V+/-21mV (+/-0.5%)
- Auto load current distribution control
  - Auto power management between system load and battery charge within input current limitation
  - Built-in low Ron path switch (30mohm)
  - System output voltage regulation
    Default position : V_{IN} pass-through
    Switching between V_{IN} pass-through and V_{SYS45}
- Compliance with JEITA guideline
  - Thermistor I/F detects battery temp. to control CC/CV parameters by built-in charge profile
- I2C interface
  - Adjustable charging parameters
- Protection function
  - Input UVLO/OVLO - Battery over voltage detection - Timer
  - Chip temperature detection - Thermal shutdown
- Recharge function
- Gate control for system Load SW (/SG)
- Input power OK output (/POK)
- Charge State output (/STAT)

Application

- Digital Still Camera
- Digital Video Camera
- Mobile Phone
- PDA/PND
- Tablet/Note PC
- Portable Audio Player
- Portable Game Machine

Block Diagram



Pin function

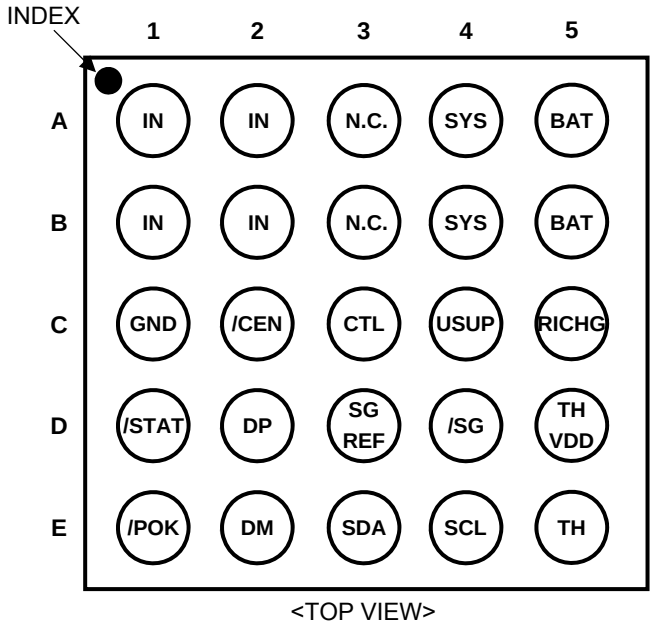
No.	Terminal name	I/O	Function
A1,A2,B1,B2	IN	I	Power input(Each IN terminal must be short-circuited on the board)
A3,B3	N.C.	-	Non connect (keep these terminals open)
A4,B4	SYS	O	System power output (Each SYS terminal must be short-circuited on the board)
A5,B5	BAT	I/O	Battery connection terminal (Each BAT terminal must be short-circuited on the board)
C1	GND	GND	Ground
C2	/CEN	I	Charge enable
C3	CTL	I	Input current limitation terminal
C4	USUP	I	Suspend terminal
C5	RICHG	O	Resistor connection terminal for setting charge current
D1	/STAT	O	Charge State output (During charge:ON, Error : Blinking)
D2	DP	I	USB DP port input
D3	SGREF	I	Reference voltage input terminal for /SG control voltage
D4	/SG	O	Gate control terminal for system Load SW
D5	THVDD	O	Regulated voltage output for the thermistor (2.0V)
E1	/POK	O	Input power OK output(Open Drain)
E2	DM	I	USB DM port input
E3	SDA	I/O	Serial data input/output
E4	SCL	I	Serial clock input
E5	TH	I	Thermistor input

/CEN	Charge function
Lo	Enable
Hi	Disable

USUP	Suspend
Lo	Disable
Hi	Enable

CTL	SDP input current limit
Lo	100mA
Hi	500mA

Pin configuration



<TOP VIEW>

Absolute maximum ratings

(Ta=25degC, unless otherwise specified.)

Symbol	Items		Ratings	Unit
V_{max}	Input voltage	IN	-0.3 to 25	V
		Other Pin	-0.3 to 6.5	V
I_{INmax}	Input current	IN	2.5	A
		IN (peak) *1	4.0	A
I_{omax}	Output current	SYS	2.5	A
		SYS (peak) *1	4.0	A
		BAT	2.5	A
		BAT (peak) *1	4.0	A
		THVDD	1	mA
I_{osmax}	Output sink current	/STAT,/POK	15	mA
T_{opr}	Operating temperature range		-30 to 85	degC
T_{stg}	Storage temperature range		-40 to 125	degC
T_j	Junction temperature		-30 to 125	degC
P_d	Power dissipation *2		2.12	W

*1 Within 200µs

*2 This value is at 75mm x 75mm x 1mm of FR4 board with 4 layers at Ta=25 degC.
It depends on the board condition.

Recommended operating condition

(Ta=25degC, unless otherwise specified.)

Symbol	Items	Min	Max	Unit
V_{IN}	IN input voltage	4.5	5.5	V
I_{IN}	IN input current	-	1.5	A
I_{SYS}	SYS output current	-	2	A
I_{BAT}	BAT output current	-	2	A
I_{CHG}	Charge current	-	1	A
T_j	Junction temperature	-30	125	degC
R_{ICHG}	Resistor value for setting charge current	1.6	24	Kohm

Electrical Characteristics

(Ta=25degC and Vin=5V, unless otherwise specified.)

Item	Symbol	Condition	Rated value			Unit
			Min.	Typ.	Max.	
Input voltage detection						
V_{IN} detection voltage	V_{UVLO}	When V_{IN} voltage rising 250mV Hysteresis	3.1	3.3	3.5	V
V_{IN} detection voltage	$V_{InBat(VIN-VBAT)}$	V_{BAT}=3.6V, When V_{IN} voltage rising, 45mV Hysteresis	0	90	180	mV
/POK detection time *1	$t_{DGLH(/POK)}$	V_{IN}:0V to 5V, /POK = Lo		64		ms
Input over voltage protection(OVP)	V_{OVP}	When V_{IN} voltage rising, 110mV Hysteresis	6.1	6.3	6.5	V
OVP detection time *1	$t_{DGLH(OVP)}$	When V_{IN} voltage rising		32		µs
OVP release detection time *1	$t_{DGLL(OVP)}$	When V_{IN} voltage falling		64		ms
Over Load detection	V_{HL}	When V_{IN} voltage falling	4.3	4.4	4.5	V
Circuit current						
BAT discharge current 1	$I_{SB1(BAT)}$	V_{BAT}=4.2V, No Load on SYS Pin			7.5	µA
BAT discharge current 2	$I_{SB2(BAT)}$	V_{IN}=5V, V_{BAT}=4.2V, No Loads on SYS Pin, At charge completion			7.5	µA
BAT discharge current 3	$I_{SB3(BAT)}$	V_{BAT}=3.2V, No Load on SYS Pin, At 'error 1'			20	µA
Standby current	$I_{SB(IN)}$	V_{IN}=5V,Suspend			1.5	mA
Circuit current	$I_{CC(IN)}$	V_{IN}=5V, /CEN=HI, I_{SYS}=0			6	mA
Auto load current distribution and Input current limitation						
ON Resistance between IN and SYS	R_{IN-SYS}	V_{IN}=5.0V,I_{SYS}=0.2A USB1500mA setting		250	450	mΩ
ON Resistance between BAT and SYS (supplied from BAT)	$R_{BAT-SYS}$	V_{IN}=0V,V_{BAT}=4.2V, I_{SYS}=0.2A		30	60	mΩ
VSYS regulation voltage	V_{SYS45}	V_{IN}=5V,V_{BAT}=3.5V	4.4	4.5	4.6	V
Input current limitation	I_{LIM0}	USB100mA Mode	80	90	100	mA
	I_{LIM1}	USB500mA Mode	450	475	500	mA
	I_{LIM2}	USB1000mA Mode	800	900	1000	mA
	I_{LIM3}	USB1500mA Mode	1200	1350	1500	mA
	I_{LIM4}	ADP1800mA Mode	1500	1710	1800	mA
VSYS regulation voltage (When current distribution works)	V_{SYS43}	USB500mAMode When current distribution works V_{IN}=5V,V_{BAT}=3.7V	4.2	4.3	4.4	V
Regulation voltage between BAT and SYS	V_{SYSR}	USB100mAMode I_{SYS}=200mA V_{IN}=5V,V_{BAT}=3.7V	0.05	0.1	0.15	V

*1:Design guarantee

Electrical Characteristics

(Ta=25degC and Vin=5V, unless otherwise specified.)

Item	Symbol	Condition	Rated value			Unit
			Min.	Typ.	Max.	
Battery voltage detection						
Charge control voltage(4.20V)	$V_{chg4.20V}$	V_{CHG}=4.20V,I_{BAT}=0A	4.179	4.200	4.221	V
Charge control voltage(4.15V)	$V_{chg4.15V}$	V_{CHG}=4.15V,I_{BAT}=0A	4.10	4.15	4.20	V
Charge control voltage(4.10V)	$V_{chg4.10V}$	V_{CHG}=4.10V,I_{BAT}=0A	4.05	4.10	4.15	V
Charge control voltage(4.05V)	$V_{chg4.05V}$	V_{CHG}=4.05V,I_{BAT}=0A	4.00	4.05	4.10	V
Charge control voltage(4.00V)	$V_{chg4.00V}$	V_{CHG}=4.00V,I_{BAT}=0A	3.95	4.00	4.05	V
Charge start voltage	V_{start}	When V_{BAT} voltage rising, 100mV Hysteresis	1.40	1.50	1.60	V
Quick charge start voltage	V_{qchgon}	When V_{BAT} voltage rising, 100mV Hysteresis	2.90	3.00	3.10	V
Recharge start voltage	V_{rechg}	When V_{BAT} voltage falling,	3.70	3.80	3.90	V
Overvoltage detection voltage	V_{ov}	When V_{BAT} voltage rising	4.27	4.35	4.43	V
Charge current detection						
Quick charge current(1.0C)	$I_{chg1.0C}$	RICHG=(3Kohm),V_{BAT}=3.5V	450	500	550	mA
Quick charge current(0.5C)	$I_{chg0.5C}$	RICHG=(3Kohm),V_{BAT}=3.5V	200	250	300	mA
Trickle charge current(0.2C)	$I_{prechg0.2C}$	RICHG=(3Kohm),V_{BAT}=2.5V	70	100	130	mA
Trickle charge current(0.1C)	$I_{prechg0.1C}$	RICHG=(3Kohm),V_{BAT}=2.5V	35	50	65	mA
Charge completion current(0.2C)	$I_{fc0.2C}$	RICHG=(3Kohm),When CV control	70	100	130	mA
Charge completion current(0.1C)	$I_{fc0.1C}$	RICHG=(3Kohm),When CV control	35	50	65	mA
Charge completion current(0.05C)	$I_{fc0.05C}$	RICHG=(3Kohm),When CV control	10	25	40	mA
Timer circuit						
Oscillation frequency	F_{osc}		57.6	64.0	70.4	KHz
Trickle charge timer *1	T_{dchg}		54	60	66	Min
Quick charge timer *1	T_{chg}		270	300	330	Min
Weak Battery timer *1	T_{wchg}		36	40	44	Min
Chip temperature detection						
Chip temperature detection *1	T_{treg}	Chip temperature, 10degC Hysteresis		110		degC
Chip temperature reset detection*1	T_{trgrst}	Chip temperature		125		degC
Thermal shutdown temperature*1	T_{sd}	Chip temperature		150		degC
Thermistor detection *2						
THVDD output voltage	V_{THVDD}	Io=0mA	1.90	2.00	2.10	V
Temperature protection detect voltage 1	T_{THMVL}	R_{pu}=100K,R_{th}=311.6K, 2.5degC(±2.5degC)	73.15	75.70	78.12	%
Temperature protection detect voltage hysteresis 1	V_{THMVL}	2.5degC+2.5degC（±2degC）	17	51	85	mV
Temperature protection detect voltage 2	T_{THML}	R_{pu}=100K,R_{th}=184.5K, 12.5degC(±2.5degC)	61.93	64.85	67.71	%
Temperature protection detect voltage hysteresis 2	V_{THML}	12.5degC+2.5℃（±2degC）	20	59	98	mV
Temperature protection detect voltage 3	T_{THMH}	R_{pu}=100K,R_{th}=45.5K, 42.5degC(±2.5degC)	29.03	31.27	33.63	%
Temperature protection detect voltage hysteresis 3	V_{THMH}	42.5degC-2.5℃（±2degC）	16	47	78	mV
Temperature protection detect voltage 4	T_{THMVH}	R_{pu}=100K,R_{th}=24.5K, 57.5degC(±2.5degC)	18.18	19.69	21.32	%
Temperature protection detect voltage hysteresis 4	V_{THMVH}	57.5degC-2.5degC（±2degC）	11	32	53	mV
Thermistor connection detect voltage	T_{THCON}	R_{pu}=100K	90	93	96	%

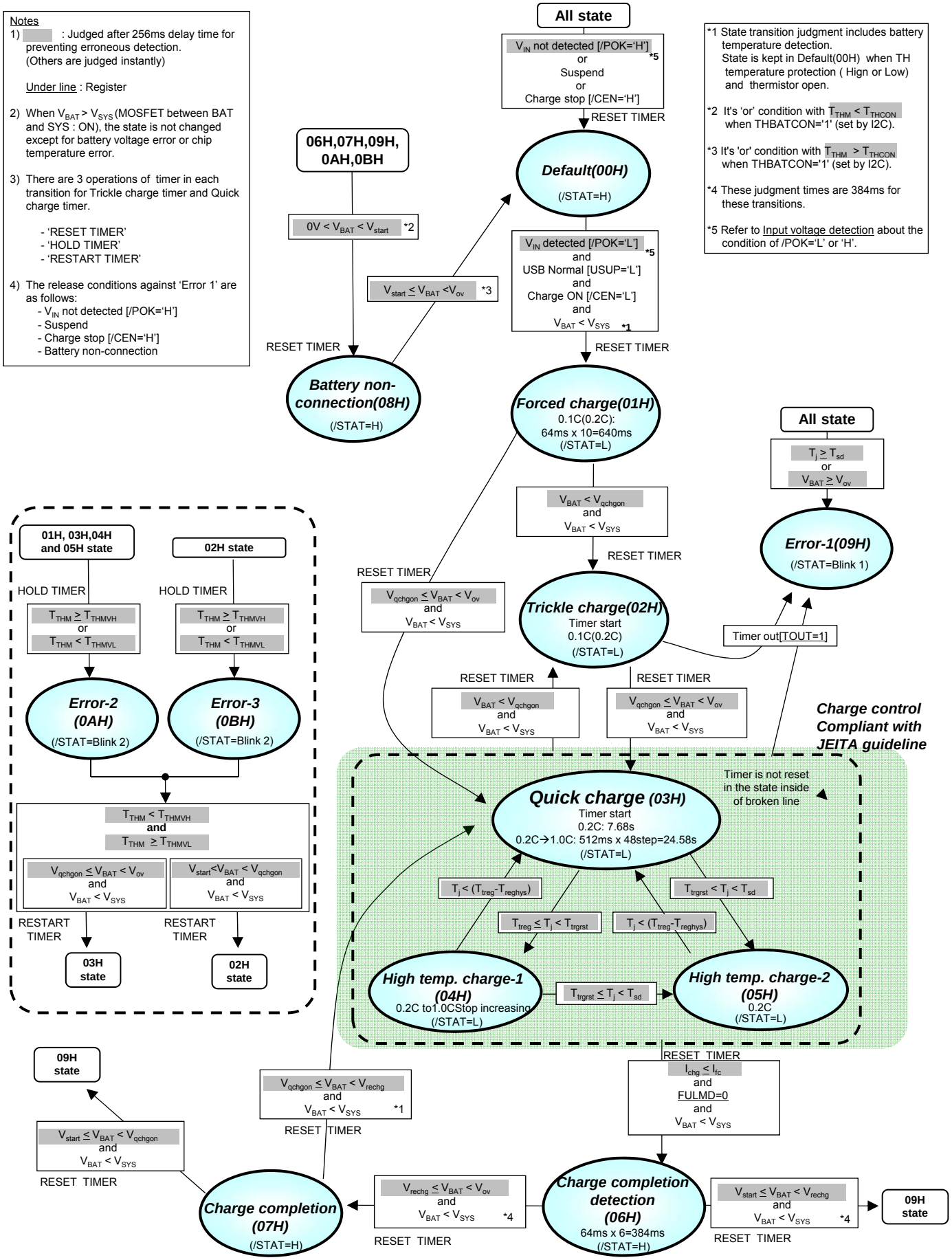
*1: Design guarantee
*2: NCP15WF104F03RC(MURATA)

Electrical Characteristics

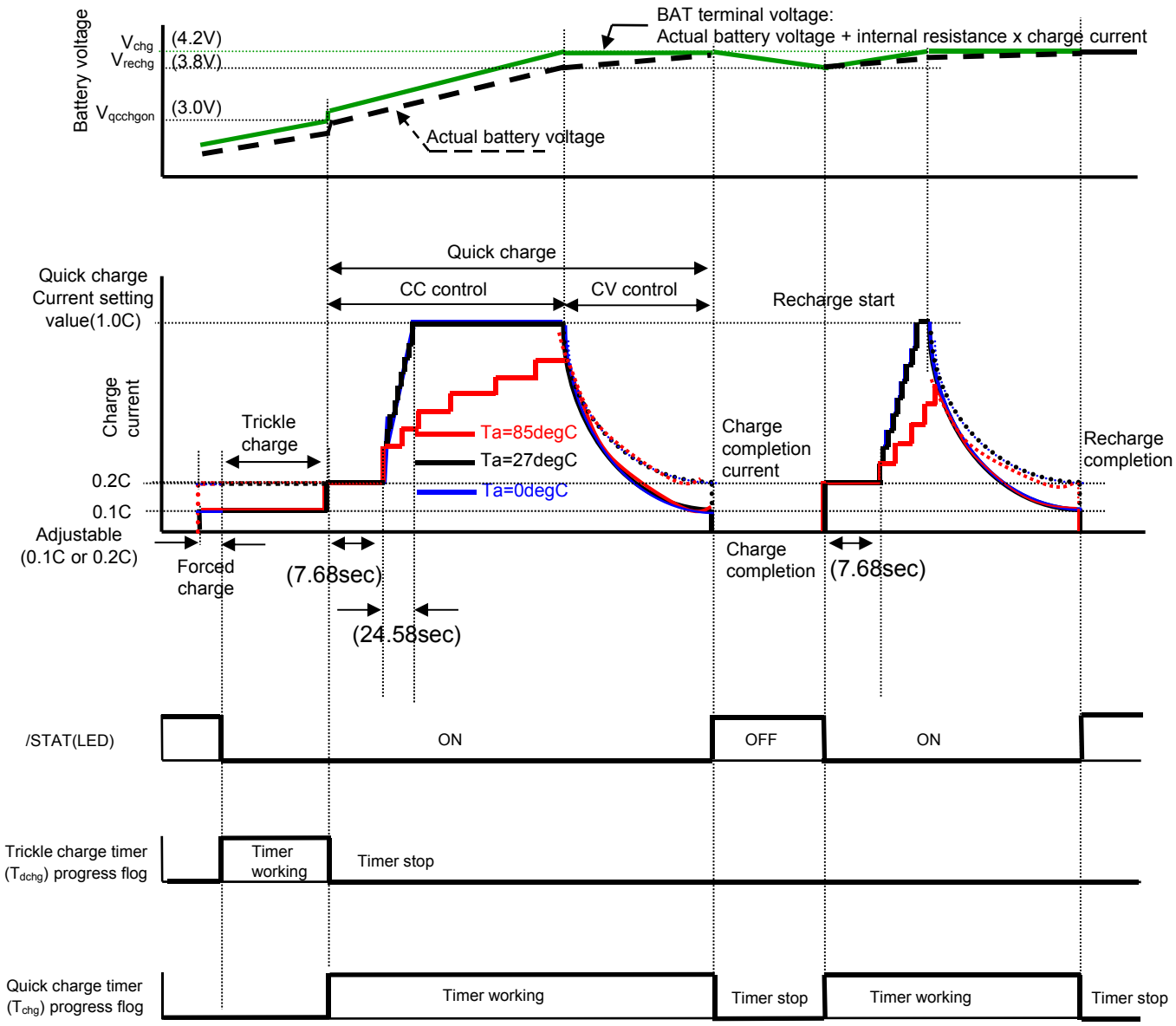
(Ta=25degC and Vin=5V, unless otherwise specified.)

Item	Symbol	Condition	Rated value			Unit
			Min.	Typ.	Max.	
/CEN,CTL,USUP terminal						
Input High voltage	V_{INH}		1.2			V
Input Low voltage	V_{INL}				0.5	V
Input source current	I_{IH}	V_{INH}=2.8V			50	µA
Input sink current	I_{IL}	V_{INL}=0.03V			1	µA
SCL,SDA terminal						
Input High voltage	$V_{INH(I2C)}$		1.4			V
Input Low voltage	$V_{INL(I2C)}$				0.3	V
Output Low voltage (SDA)	$V_{OL(SDA)}$	I_{sink}=3mA			0.4	V
Input source current	$I_{IH(I2C)}$	$V_{INH(I2C)}$=1.8V			5	µA
Input sink current	$I_{IL(I2C)}$	$V_{INL(I2C)}$=0.03V			1	µA
/POK,/STAT terminal						
Output Low voltage	V_{OL}	I_{SINK}=5mA			0.4	V
Gate control for System Load SW						
Low battery detection voltage (Internal)	$V_{sysswoff}$	V_{SGREF}>V_{sysref_sw}	3.3	3.4	3.5	V
Low battery detection voltage hysteresis (Internal Setting)	$V_{sysswoff\_in\_hys}$	V_{SGREF}>V_{sysref_sw}	33	100	166	mV
Low battery detection voltage hysteresis (External Setting)	$V_{sysswoff\_out\_hys}$	$V_{sysswoff\_out}$=3.4V	100	200	300	mV
SGREF detection voltage	V_{sysref_sw}		1.7	1.8	1.9	V
USB detection						
DP to DM short resistance	R_{DPM_SHORT}	USB battery charging 1.2		125	200	Ω
DP terminal voltage	V_{DP_SRC}	USB battery charging 1.2	0.5	0.6	0.7	V
DM terminal voltage	V_{DM_SRC}	USB battery charging 1.2	0.5	0.6	0.7	V
DP terminal sink current	I_{DP_SINK}	USB battery charging 1.2	50		150	µA
DM terminal sink current	I_{DM_SINK}	USB battery charging 1.2	50		150	µA
Data detection voltage (When rising)	V_{DAT_REF}	USB battery charging 1.2	0.25		0.40	V
Divided Port						
Divided Port Middle voltage	V_{DIV_MID}		1.90	2.00	2.10	V
Divided Port High voltage	V_{DIV_HIGH}		2.55	2.68	2.81	V

Charge state diagram



Charge state diagram



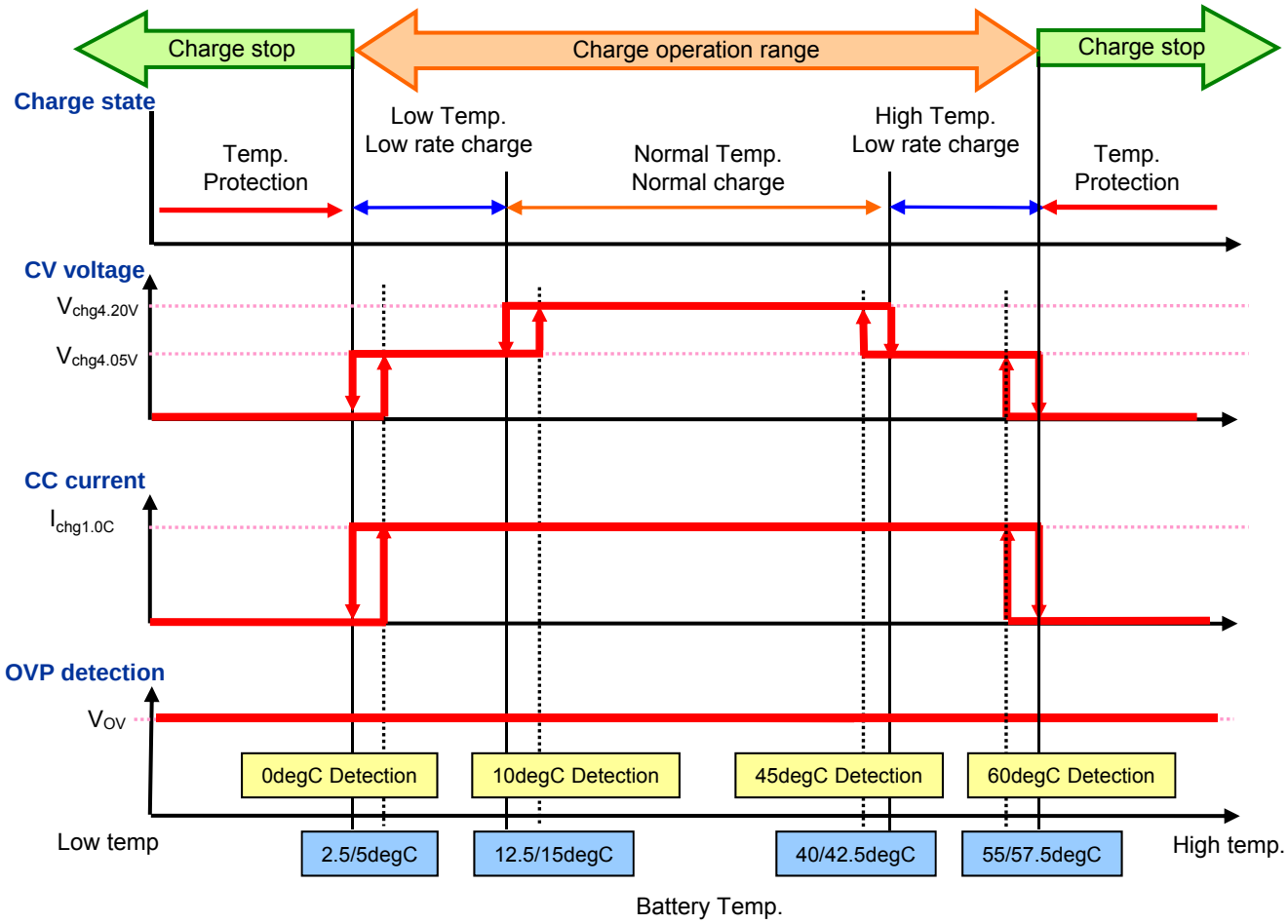
Note:
* During quick charge, junction temperature is monitored to limit charge current value between 0.2C-1.0C so that the junction temperature may not exceed Ttreg.

* The High temp. charge-1 (04H) is operating at Ta=85 degC in above waveform.

Function description

Battery temperature detection

This IC detects battery temperature with thermistor I/F and controls CV voltage according to built-in charge profile.



There is the delay time(64ms x 4times=256ms) for preventing erroneous detection before judging the battery temperature.

Control Diagram corresponding JEITA Guideline

When PSE control (ADR=02H) is 'Enable' setting, the charge control voltage changes as the above chart according to JEITA guide line. But when VCHG setting (ADR=00H) is 4.00V, the charge control voltage at low rate charge is also 4.00V not 4.05V.
When PSE control (ADR=02H) is 'Disable' setting, the charge control voltage depends on the VCHG setting (ADR=00H).
When THBATCON (ADR=02H) is 'Enable' setting, the battery connection is detected with battery voltage or TH voltage. For details, please refer to 'Battery connection detection'.
When thermistor is not used, please connect TH terminal with THVDD terminal and set 'PSE control (ADR=02H)' to 'Disable'.

Resister value for thermistor

TEMP. (deg.C)	R(KΩ)
2.5	311.6
5.0	272.5
12.5	184.5
15.0	162.7

TEMP. (deg.C)	R(KΩ)
40.0	50.7
42.5	45.5
55.0	27.1
57.5	24.5

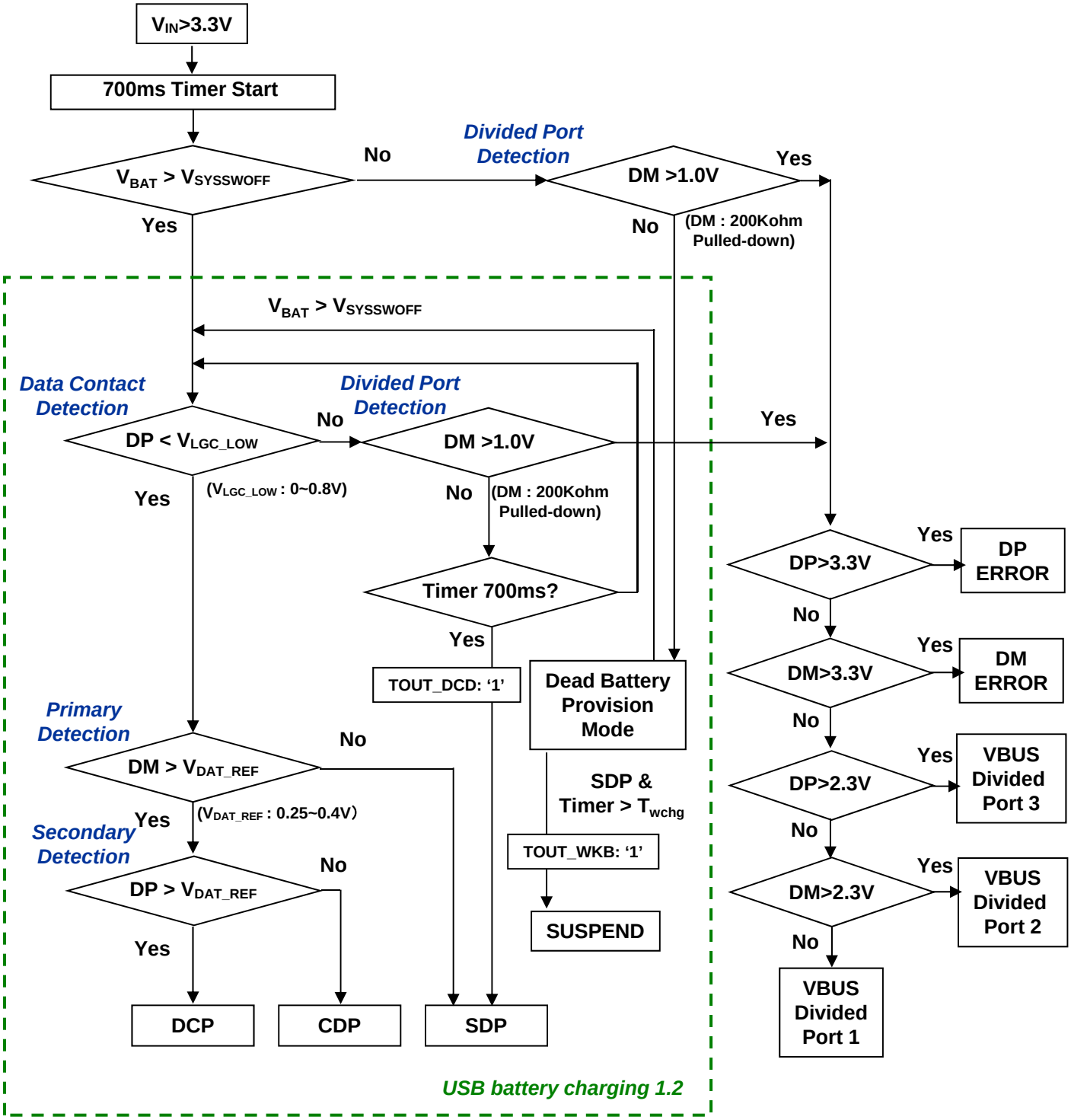
* : NCP15WF104F03RC (Murata)

Function description

USB port detection

[USB port detection flow chart]

This IC detects the type of USB port as the following chart after USB connection.



Function description

6 types of USB port detection are enabled by detecting DP and DM terminals and the current limit is automatically set for each port. This detection starts after applying the voltage above V_{ULVO} (TYP. 3.3V) to IN terminal or sending reset signal by RST_USBDET (ADR:02H).

No.	Port	USB battery charging 1.2	Current limit (mA)
1	SDP (Standard Downstream Port)	O	100 or 500 *1
2	CDP (Charging Downstream Port)	O	1500
3	DCP (Dedicated Charging Port)	O	1500
4	VBUS Divided Port 1	-	500
5	VBUS Divided Port 2	-	1000
6	VBUS Divided Port 3	-	1800

*1 It depends on CTL terminal setting

CTL	SDP current limit
Lo	100mA
Hi	500mA

The detection result is stored in the registers.
When DP and DM terminals are open, this IC regards the port as SDP and indicates '1' in 'TOUT_DCD' register.
When DP>3.3V or DM>3.3V, this IC indicates 'ERROR' register and enter the suspend mode. Suspend is can be dissolved by 'RST_USBDET' or 'USBMD'.

04H USB Detection result (Read only)

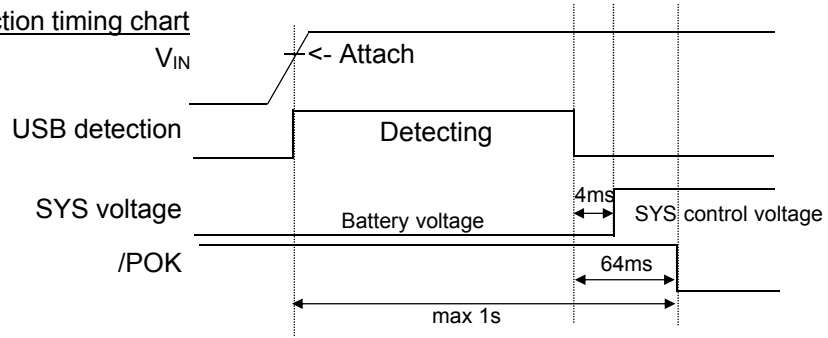
Bit5	Bit4	Bit3	USB
0	0	0	SDP (Standard Downstream Port)
0	0	1	CDP (Charging Downstream Port)
0	1	0	DCP (Dedicated Charging Port)
1	0	0	VBUS Divided Port 1
1	0	1	VBUS Divided Port 2
1	1	0	VBUS Divided Port 3
0	1	1	DP ERROR
1	1	1	DM ERROR

For VBUS Divided Port, this IC detects the combination of the divided voltage with 'DP' and 'DM' terminals as the following chart.

Port	DP	DM	Current limit(mA)
VBUS Divided Port 1	2.00V	2.00V	500
VBUS Divided Port 2	2.00V	2.68V	1000
VBUS Divided Port 3	2.68V	2.00V	1800

* These voltages are the divided voltage at V_{IN}=5.0V. These voltages also change with V_{IN} voltage at this dividing ratio.
* Please set the downside resistance of the divided resistances to be above 100Kohm.

USB detection timing chart



DP and DM terminal become Hi-Z (open) after USB detection.

Function description

Dead Battery Provision

When VBAT < $V_{sysswoff\_set}$ (low battery detection voltage) at the USB detection, the behaviors for each USB port are as follows:

< SDP (Standard Downstream Port) >
- SG terminal is 'H'.
- Trickle charge or quick charge can start.
- Dead Battery Provision starts and DP terminal outputs V_{DP_SRC} (Typ. 0.6V).
- If VBAT doesn't exceed $V_{sysswoff}$ in T_{wchg} (typ. 40min.), it shifts into the suspend mode. Please reconnect with V_{IN} to resolve this suspend mode.
- It can stop Weak Battery timer to set Timer Control (ADR=01H) to 'RESET' or 'Count Stop'. Setting input current with 'USBMD'='1' can avoid shifting into the suspend mode.
- When VBAT > $V_{sysswon}$ ($V_{sysswoff}$ + $V_{sysswoff\_hys}$) , the USB detection is carried out again. During the USB detection, it shifts into the suspend mode and SYS terminal outputs BAT voltage. The charge function starts from 'Default (00H)' and SG terminal is 'L'. DP and DM terminals becomes Hi-Z (open) after the USB detection. If the battery voltage drops below $V_{sysswoff}$ after this, Dead Battery Provision doesn't start again. /SG is set to 'H' but Weak Battery timer and V_{DP_SRC} output from DP terminal don't operate.

< DCP (Dedicated charging Port) >
- SG terminal is 'H'.
- Trickle charge or quick charge can start.
- Dead Battery Provision starts and DP terminal outputs V_{DP_SRC} (Typ. 0.6V).
- Weak Battery timer (Typ. 40 min) doesn't count up. But the each charging timer (trickle or quick charge timer) counts up.
- When VBAT > $V_{sysswon}$ ($V_{sysswoff}$ + $V_{sysswoff\_hys}$) , the USB detection is carried out again. During USB detection, it shifts into the suspend mode and SYS terminal outputs BAT voltage. The charge function starts from 'Default (00H)' and SG terminal is 'L'. DP and DM terminals becomes Hi-Z (open) after the USB detection. If the battery voltage drops below $V_{sysswoff}$ after this, Dead Battery Provision doesn't start again. /SG is set to 'H' but V_{DP_SRC} output from DP terminal doesn't operate.

< CDP (Charging Downstream Port) >
- the operation is the same as DCP. But during Dead Battery Provision mode, this port is detected as 'DCP' and USB detection register (ADR=04H) also indicates 'DCP'.

< Divided port 1,2,3>
- There isn't Dead Battery Provision for Divided port. USB detection after good battery detection doesn't start.
- SG terminal is 'H'.

Connecting IN terminal when BAT is open is regarded as 'Weak Battery' and Dead Battery Provision starts. If Dead Battery Provision continues in T_{wchg}, it shifts into the suspend mode. For avoiding shifting into the suspend mode, set timer control (ADR=01H) to 'RESER' or 'Count STOP'.

Function description

SGREF terminal setup

The low battery detection voltage ($V_{sysswoff}$) is used for the following functions.
- Detection weak battery after 'Forced charge (01H)'
- On/off function for MOSFET for System load SW'

SGREF terminal voltage (V_{SGREF}) can set the low battery detection voltage($V_{sysswoff}$).

[SGREF detection voltage (Typ. 1.8V) < V_{SGREF}]
- The internal setting is selected.
  $V_{sysswoff}$ = $V_{sysswoff\_in}$ (Typ. 3.4V) , Hysteresis voltage = $V_{syssw\_in\_hys}$ (Typ. 100mV)

We recommend that SGREF is connected with THVDD when using the internal setting.

[GND < V_{SGREF} < SGREF detection voltage (Typ. 1.8V)]
- $V_{sysswoff}$ = $V_{sysswoff\_out}$

  Relational expressions are as follows:

  V_{SGREF} = 0.354 x $V_{sysswoff\_out}$

  $V_{syssw\_out\_hys}$ = 200mV x $V_{sysswoff\_out}$ / 3.4V

* Input 0.3V to SGREF if the low battery detection function is not used.
It is possible to divide THVDD voltage with upper 51KΩ and lower 9.1KΩ resistances .

Gate control for system Load SW (/SG)

This function controls '/SG' terminal.
'/SG' terminal is connected with the LoadSW (recommended Renesas HAT1069C) between The SYS terminal and SYSTEM, and controls power supply to SYSTEM ON/OFF.
And '/SG' terminal can be used for the control of an USB SW because this terminal becomes 'H' (OFF) during the USB detection.

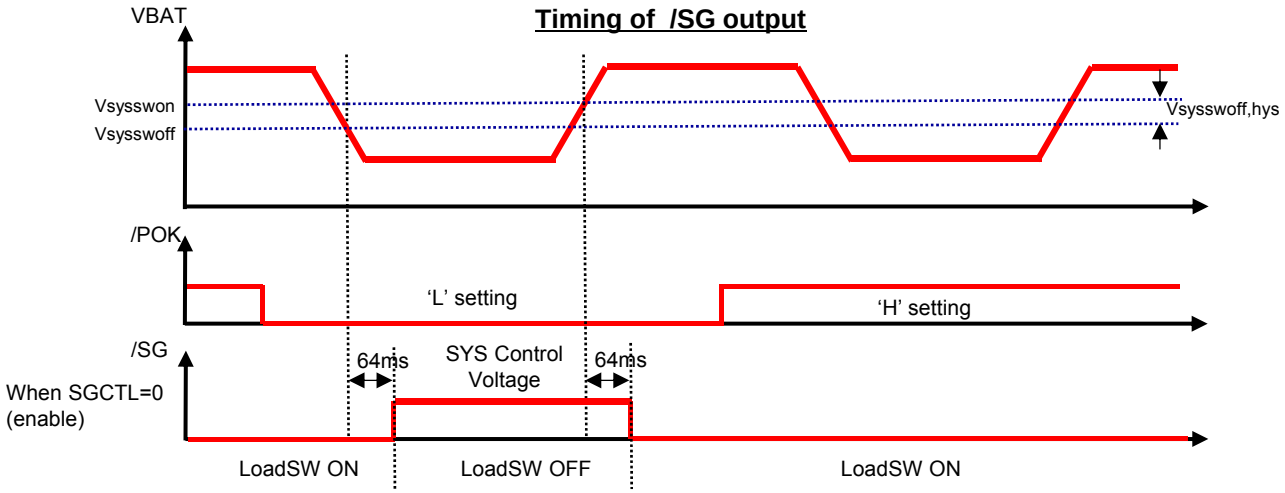
1. '/SG' = 'H' ('OFF') during the USB detection or Dead Battery Provision. 'H' voltage during the USB detection can become the BAT voltage. Refer to 'Starting function after IN connected'.
2. This function can be selected for 'Enable' or 'Disable' by SGCTL (ADR=02H).
3. When the battery voltage is low, all current can be used for charging by stopping the current supply for SYSTEM with the LoadSW off. (After USB detection & SGCTL: Enable)

[/SG control in each condition about the IN and the BAT (Except for the USB detection, Dead Battery Provision and SGCTL: Disable)]

(1) IN : connect , BAT : connect
- V_{BAT} < V_{start} — ON('L')
- V_{start} < V_{BAT} < $V_{SYSSWOFF}$ — OFF('H')
- $V_{SYSSWOFF}$ < V_{BAT} — ON('L')

(2) IN : connect , BAT : non-connect — ON('L')
(3) IN : non-connect , BAT : connect — ON('L')
(4) IN : non-connect , BAT : non-connect — IC and SYSTEM are not operated

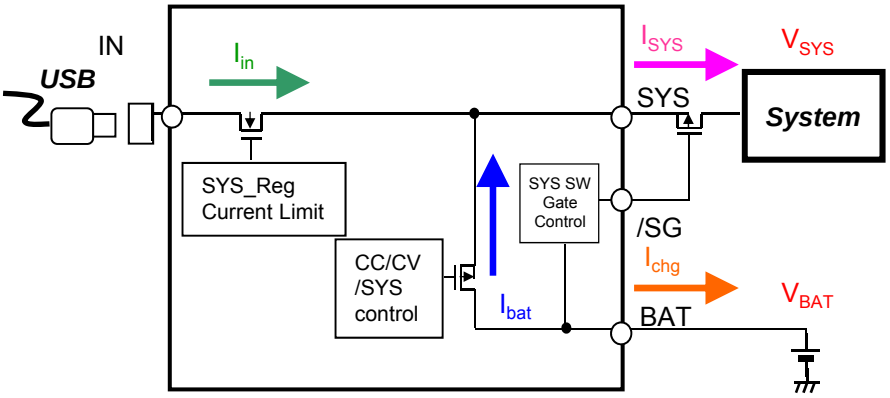
Timing of /SG output



Function description

Input current limitation / Control between SYS and BAT

- USB detection (USB battery charging 1.2)
- Input current limitation(100mA/500mA/1000mA/1500mA/1800mA/limitless/Suspend) can be set by I2C.
-The current limit is dropped as the list for protection when SYS is shorted.
-When the total sum of the charge current and the system current is below the input limit current,
  SYS terminal outputs IN voltage directly. When IN voltage is over 5.4V, SYS voltage is controlled to be below 5.4V.
  Capable for switching between V_{SYS45} and V_{IN} pass-through by I2C.
-IC switches the system power supply and the battery charge seamlessly within input current limitation.



Input Current Limit when SYS is shorted.

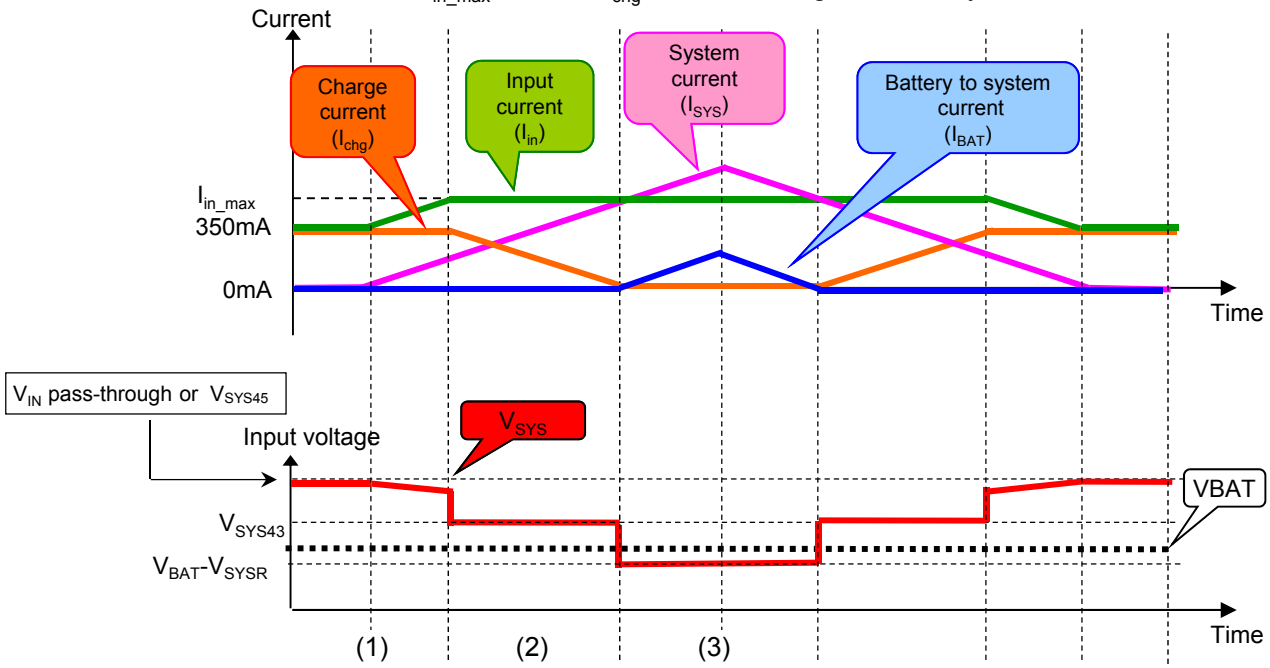
Current Limit Setting	at SYS short
100mA 500mA	20%
1000mA	40%
1500mA 1800mA	50%

(Design Guarantee)

Auto load current distribution control

Example of power control between the system supply and the battery charge

Conditions : IN=5.0V is connected, I_{in_max}=500mA, I_{chg}=350mA, Chargeable battery is connected.



(1) The IC charges the battery at I_{chg}=350mA and supplies the system current(ISYS) within I_{in_max}=500mA.

(2) When the system current(I_{SYS}) increases and the total sum of I_{SYS} and I_{chg} reaches I_{in_max}, the IC reduces the charge current.

(3) When the system current (I_{SYS}) increases more and I_{SYS} exceeds I_{in_max}, V_{SYS} falls to V_{BAT}-V_{SYSR} and the battery supplies the load current to system through the Path SW. (IC attempts to sustain the system voltage no matter what causes it to drop.)

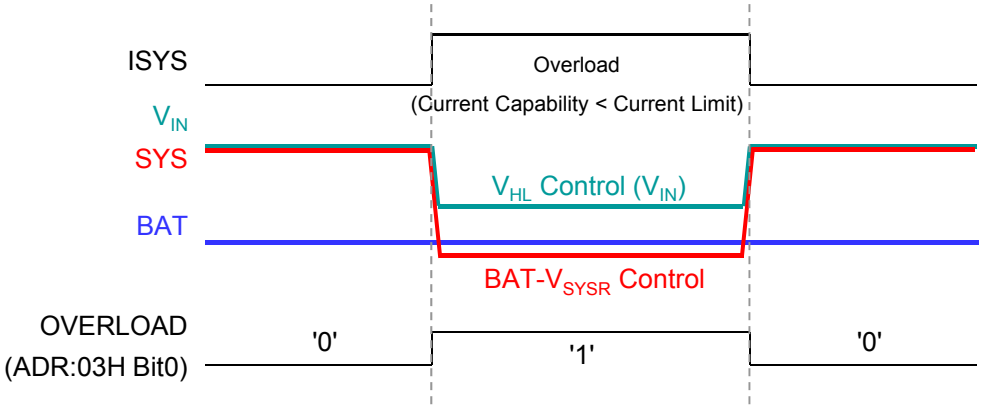
Function description

Over load detection

When IN voltage drops below V_{HL}, the input current is controlled as the current at the time regardless of the current limit setting. The OVERLOAD register (ADR:03H Bit0) indicate '1'.

This IC detects lack of current capability of power supply and prevents exceeded current from flowing from IN terminal.

Operation of Over load detection



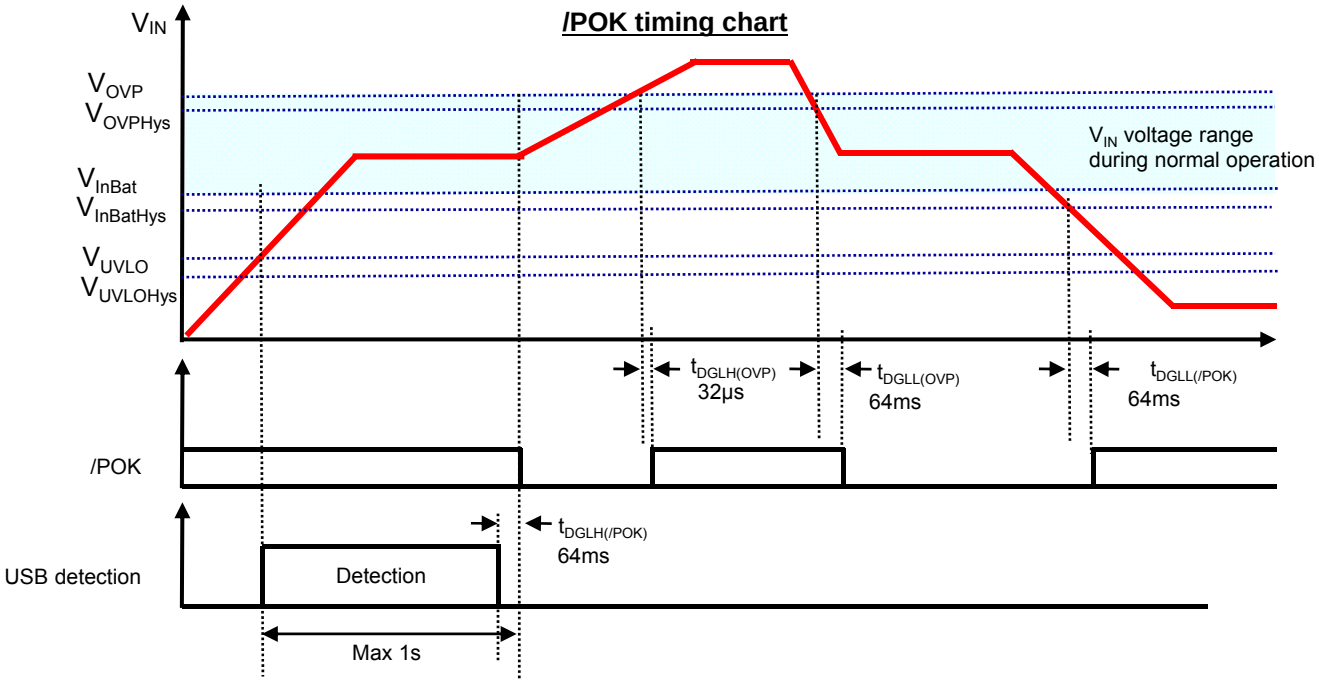
* This detection operates when IN voltage < V_{HL}.
In this mode, charging doesn't operate.

Input voltage detection

$V_{UVLO} \leq V_{IN} \leq V_{OVP}$ and $V_{IN} \geq V_{BAT}+V_{InBat}$: Power supply from IN to SYS and charging are available. /POK =L.

$V_{OVP} \leq V_{IN}$ or the suspend mode : Power supply from IN to SYS and charging are not available. /POK=H.

/POK timing chart



The suspend mode is shifted at the following situation:
- USUP : 'H' - I2C setting (CTL3) - USB detection
- Weak Battery Timer : Time out
- DP ERROR or DM ERROR (After USB detection)
- USB detection reset (RST_USBDET : Enable)

Function description

Battery connection detection

THBATCON : 'Disable'

connection sequence	Battery condition	Thermistor		
		Included in battery *1	on board *2	No use *3
BAT -> IN	Normal	Starting from Default(00H)	Starting from Default(00H)	Starting from Default(00H)
	Open Battery	Starting from Default(00H)	Starting from Default(00H)	Starting from Default(00H)
IN -> BAT *4	Normal	Starting from Default(00H)	Forbidden	
	Open Battery	Default(00H)		

THBATCON : 'Enable'

connection sequence	Battery condition	Thermistor		
		Included in battery *1	On board	No use
BAT -> IN	Normal	Starting from Default(00H)	Forbidden	
	Open Battery	Starting from Default(00H)		
IN -> BAT *4	Normal	Starting from Default(00H)		
	Open Battery	Starting from Default(00H)		

*1 : TH voltage is in the charging range.
Charging doesn't starts with no battery because TH voltage is not in the charging range.
*2 : TH voltage is in the charging range.
*3 : PSE Control : 'Disable'
*4 : Don't start charging with no battery.

Function description

Battery connection is detected by battery voltage as follows:

- Battery voltage (V_{BAT}) > Charge start voltage (V_{start})

When register [THBATCON (ADR:02H)] is set to ‘Enable’, Battery connection is detected by battery voltage or TH terminal voltage as follows:

- Battery voltage (V_{BAT}) > Charge start voltage (V_{start})
- TH terminal voltage < Thermistor connection detect voltage (V_{THCON})

When thermistor is included in battery pack and this register is set to ‘Enable’, charging can also starts for an open battery.
When thermistor isn’t included in battery pack, please don’t set this register ‘Enable’.

The list in the previous page shows the behavior with 3 kinds of thermistor setting and 2 kinds of battery.
<Thermistor> ‘Included in battery’ , ‘On board’ , ‘No use’
<Battery> ‘Normal’ , ‘Open battery’

When THBATCON(ADR:02H) is ‘Disable’ setting (Default setting) , the battery connection is detected by only battery voltage.
When IN is connected after ‘battery connection’, charging starts from ‘Default (00H)’ state for both ‘Normal’ and ’Open battery ‘.
When IN is connected before ‘battery connection’, charging starts for ‘Normal’ battery as same as when IN is connected after ‘battery connection’. For ’Open battery ‘, the state stays at ‘default(00H)’ because it can’t detect battery connection. And charging is forbidden with no battery when thermistor is ‘On board’ or ‘No use’.

If THBATCON (ADR:02H) is set to ‘Enable’, battery connection is detected by either battery voltage or TH terminal voltage. Charging also starts for ’Open battery’ as same as ‘Normal’.
So it is possible to charge for all batteries when thermistor is ‘Included in battery’.
When thermistor is ‘On board’ or ‘No use’, THBATCON (ADR:02H) ‘Enable’ setting is forbidden.
And please don’t charge with no battery.

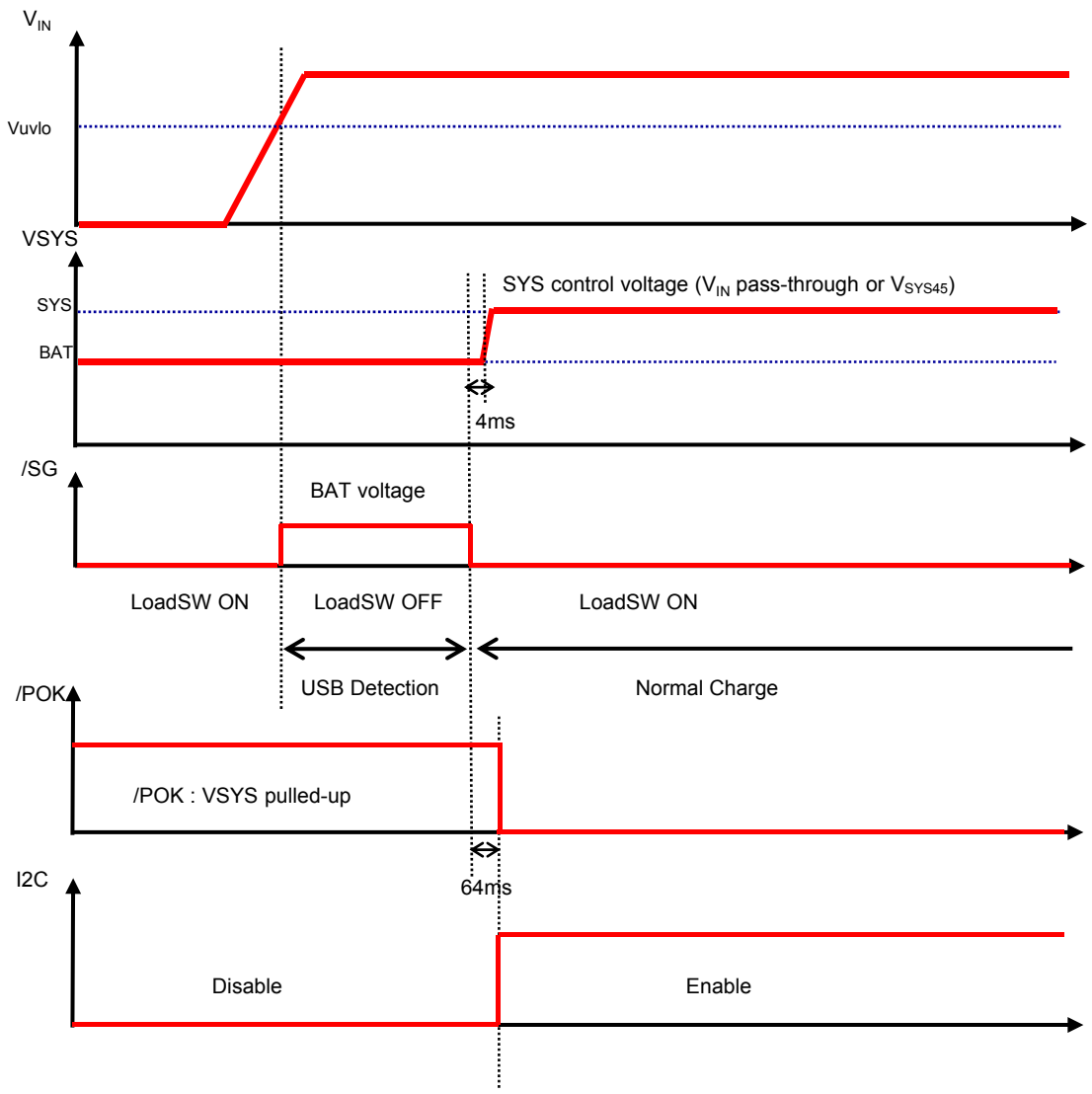
Function description

Starting function after IN connected

We show starting function for each battery and USB port.

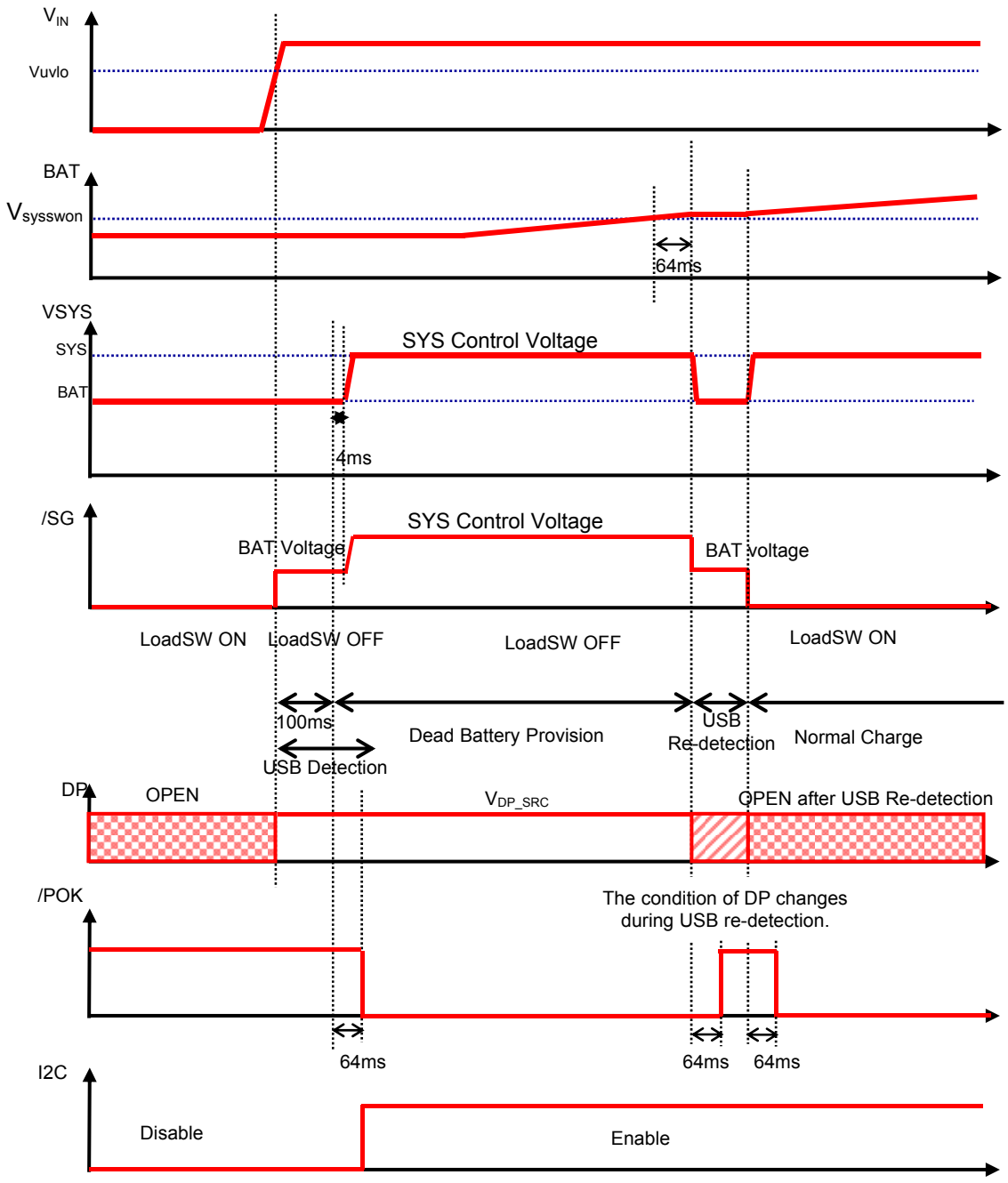
(1) USB detection with Good Battery (V_{BAT}>$V_{SYSSWOFF}$) after IN connected
(2) USB detection with Weak Battery (V_{BAT}<$V_{SYSSWOFF}$) after IN connected
[Battery Charging 1.2 Port]
(3) USB detection with Weak Battery after IN connected [Divided Port]
(4) USB detection with no Battery after IN connected [Battery Charging 1.2 Port]
(5) USB detection with no Battery after IN connected [Divided Port]

(1) USB detection with Good Battery (V_{BAT}>$V_{SYSSWOFF}$) after IN connected



(2) USB detection with Weak Battery (V_{BAT}<$V_{SYSSWOFF}$) after IN connected

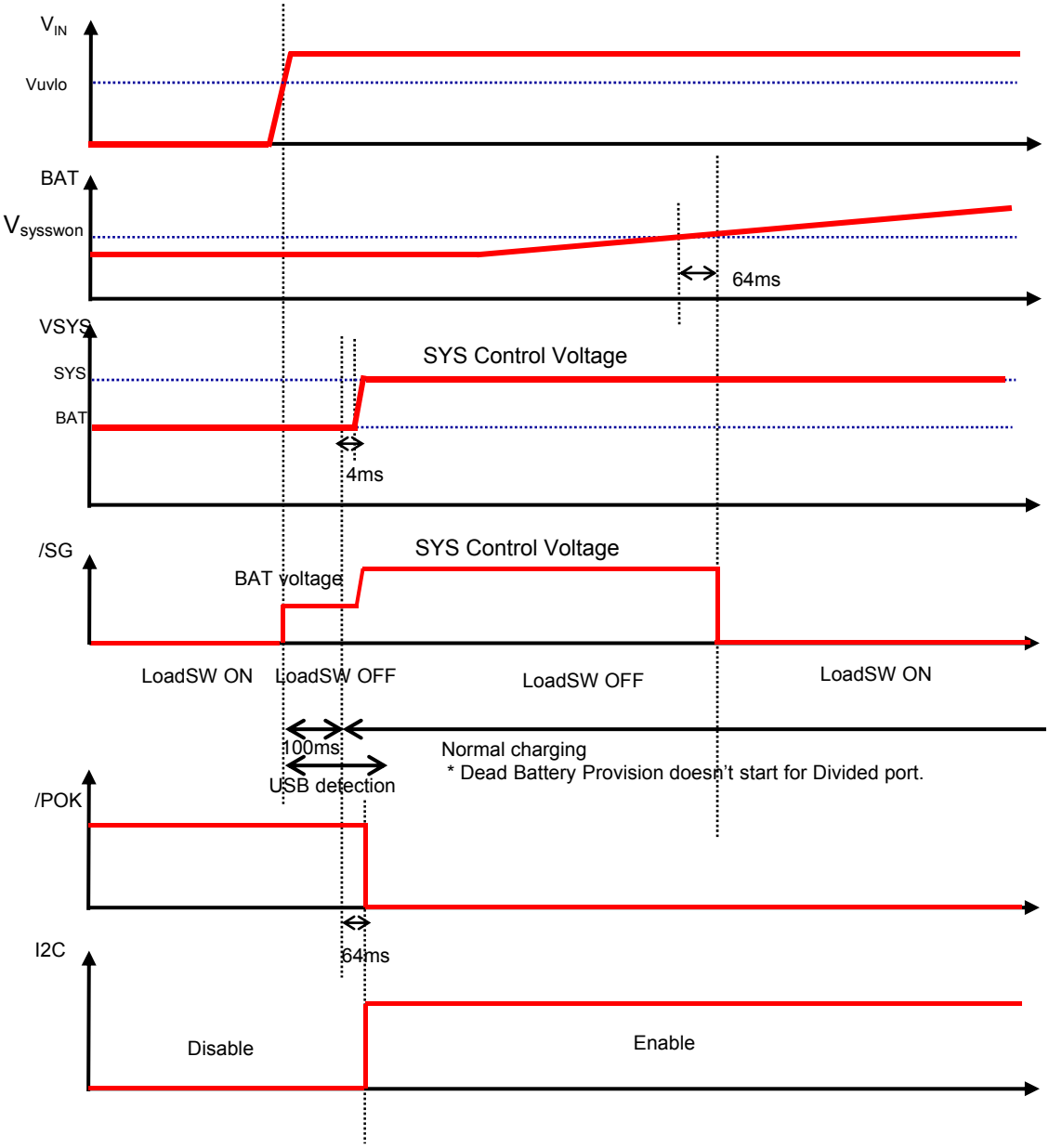
[Battery Charging 1.2 Port]



* Weak battery timer operates during Dead Battery Provision at SDP.
If the battery voltage doesn't exceed $V_{sysswoff}$ in T_{wchg} (typ. 40min.), it shifts into the suspend mode.
(Refer to 'Dead Battery Provision'.)

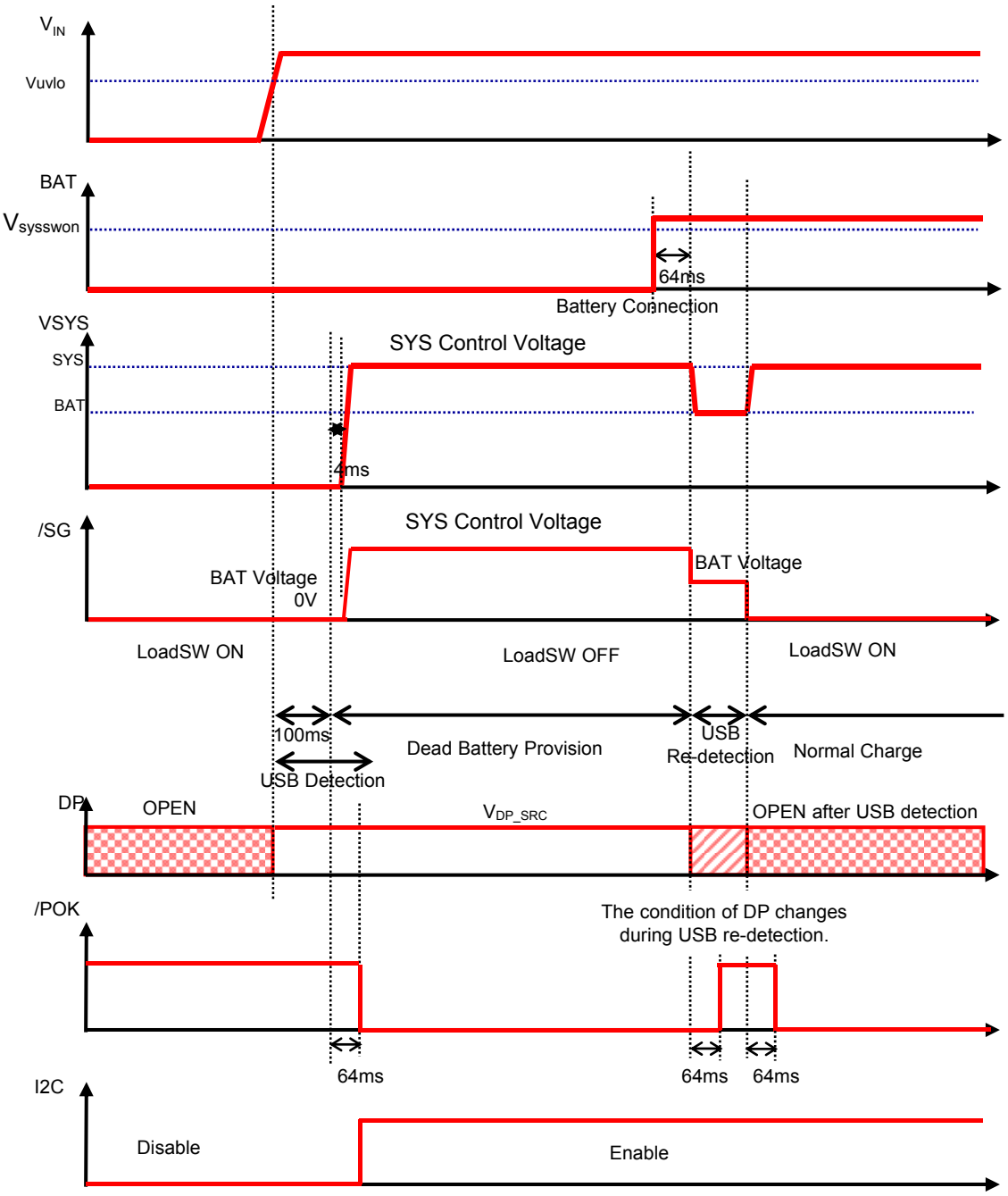
(3) USB detection with Weak Battery (V_{BAT}<$V_{SYSSWOFF}$) after IN connected

[Divided Port]



(4) USB detection with no Battery after IN connected

[Battery Charging 1.2 Port]



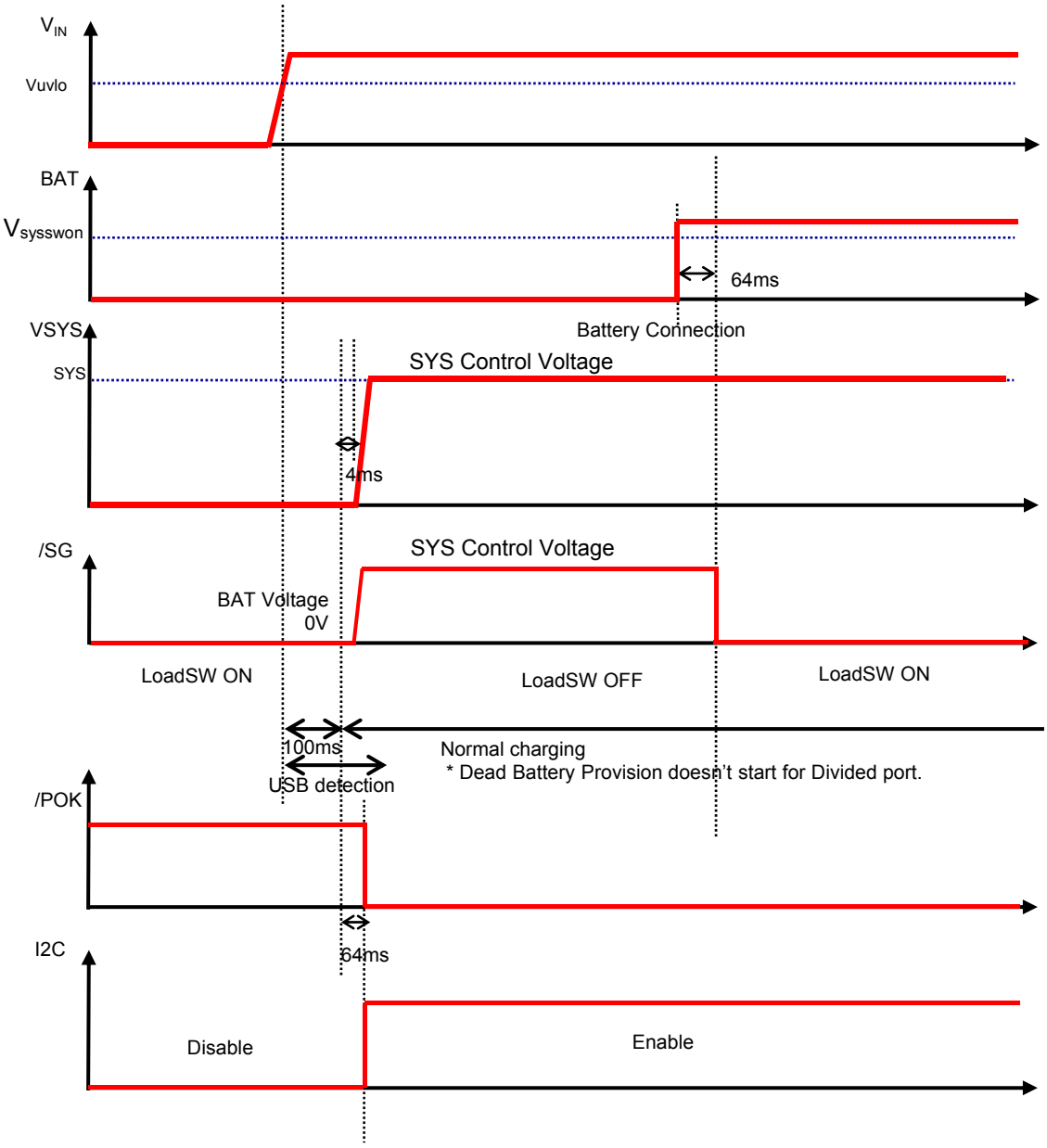
* Weak battery timer operates during Dead Battery Provision at SDP.
  If the battery voltage doesn't exceed $V_{sysswoff}$ in T_{wchg} (typ. 40min.), it shifts into the suspend mode.
  (Refer to 'Dead Battery Provision'.)

* Dead Battery Provision lasts when a weak battery is connected.
  USB re-detection starts when the battery becomes a good battery.

* Please start charging after connecting a battery. Don't start charging with no battery.

(5) USB detection with no Battery after IN connected

[Divided Port]



* /SG doesn't change when a weak battery is connected.
  /SG becomes 'L' after the battery becomes a good battery.

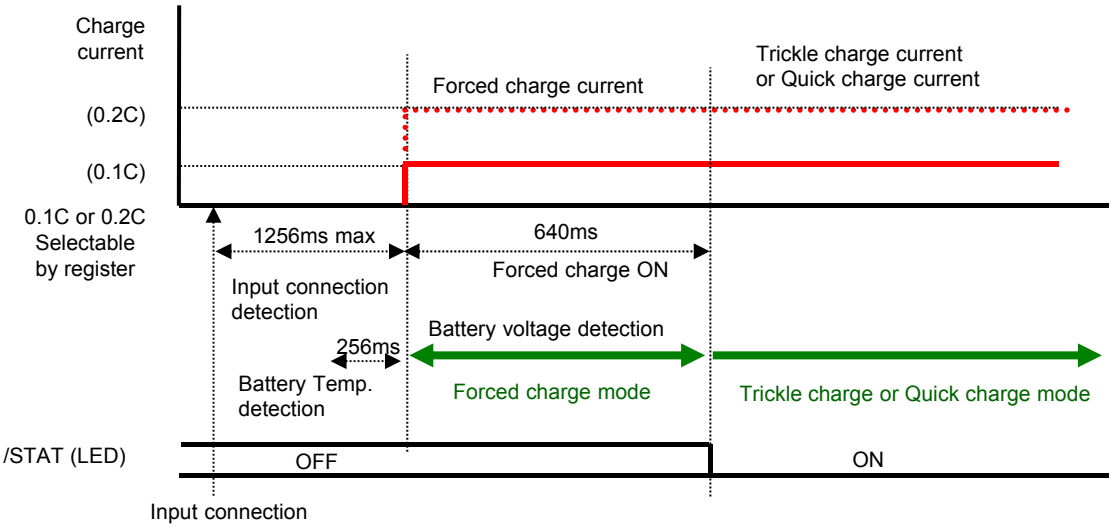
* Please start charging after connecting a battery. Don't start charging with no battery.

Function description

Forced charge

After input power detection, forced charge starts for canceling the cutoff state of battery due to over-discharge. The forced charged current is the same as trickle charge current setting. Register (ADR=00H Bit6) is available for changing setting.
Charging starts even with an open battery by this function.
Please refer to Battery connection detection.

Timing from input detection to charge start



Trickle charge (0.1C constant current charge)

After input detection and battery detection, trickle charge starts when $V_{BAT} < V_{qcchgon}$ (Typ. 3.0V).
- When detecting $V_{BAT} \geq V_{qcchgon}$, the state shifts to quick charge mode.
- Trickle charge timer starts when trickle charge starts.
- After trickle charge timer expires, the state shifts to 'error mode 1' if $V_{BAT} < V_{qcchgon}$. However trickle timer stops when the battery voltage becomes below V_{start}. When BAT is shorted, this timer also stops. NOBAT(ADR=03H, Bit5) indicates detecting the battery voltage below V_{start}. After NOBAT='1' by detecting $V_{BAT} \leq V_{start}$, please stop charging with /CEN.
- When detecting $V_{BAT} \geq V_{ov}$ (Typ. 4.35V), the state shifts to 'error mode 1'.

Trickle charge setting is selectable between 0.1C and 0.2C by register (ADR=00H Bit4,5).

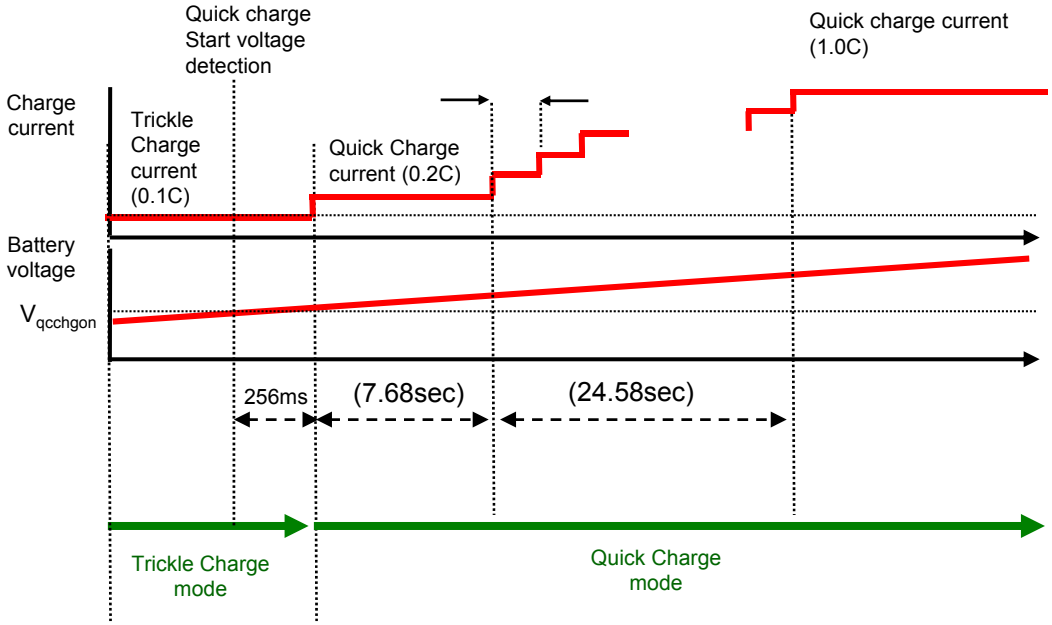
Quick charge (1.0C constant current charge)

Quick charge starts after detecting $V_{BAT} \geq V_{qcchgon}$.
- When detecting $V_{BAT}=V_{chg}$, the state shifts to CV (constant voltage) charge mode.
- Quick charge timer starts when quick charge starts.
- When detecting $V_{BAT} < (V_{chgon}$ – hysteresis voltage) (Typ. 2.9V) , the state shifts to trickle charge mode.
- When detecting $V_{BAT} \geq V_{ov}$ (Typ. 4.35V), the state shifts to 'error mode 1'.

During quick charge, this IC monitors junction temperature and controls the current between 0.2C and 1.0C not to exceed T_{treg}.
The quick charge current is selectable between 0.5C and 1.0C by register (ADR=00H Bit 0).

Function description

Timing to Quick charge(1.0C)

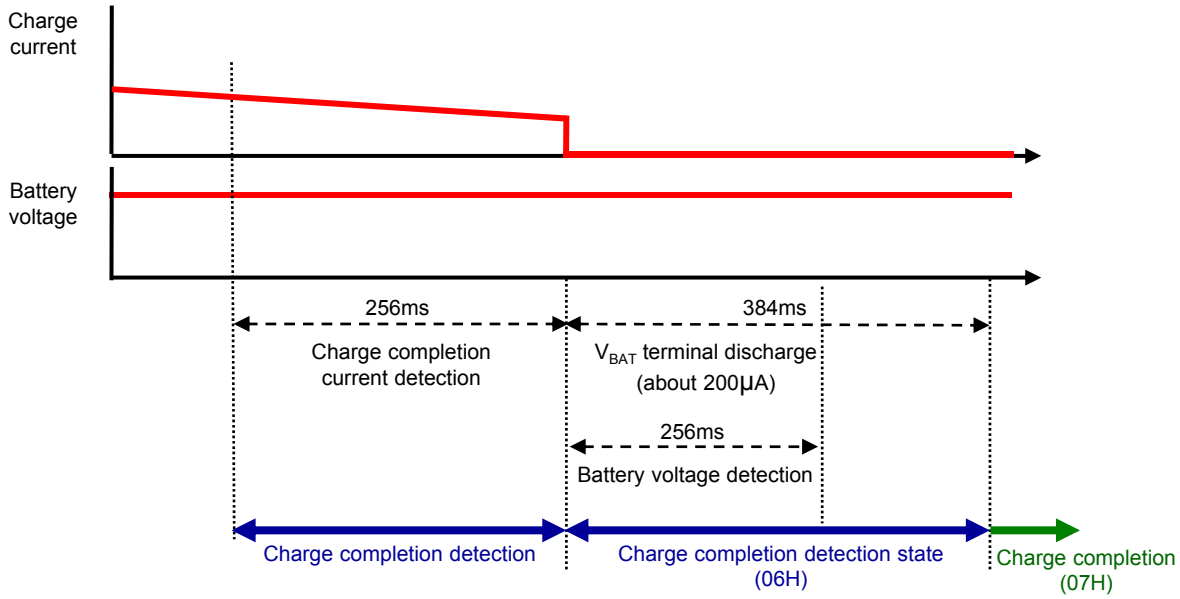


Constant voltage charge

When detecting V_{BAT}=Charge Control voltage during quick charge mode, constant voltage charge starts.

- When the charge current falls below charge completion current during constant voltage charge, the state shifts to charge completion detection mode. If $V_{BAT} \geq V_{rechg}$ (Typ. 3.8V), the state shifts to charge completion state.
- When $V_{start} \leq V_{BAT} < V_{rechg}$, the state shifts to 'error mode 1'.
- When $V_{BAT} < V_{start}$, the state shifts to Battery non-connection mode.
- The current (about 200μA) is discharged from BAT terminal during the charge completion detection mode. After this state, the next state is selected among Charge completion, Battery non-connection or Error-1 by the battery voltage.
- The charge control voltage is selectable from 4.00V to 4.20V (50mV steps) by register (ADR=00H Bit 1,2,3).

Timing of charge completion detection

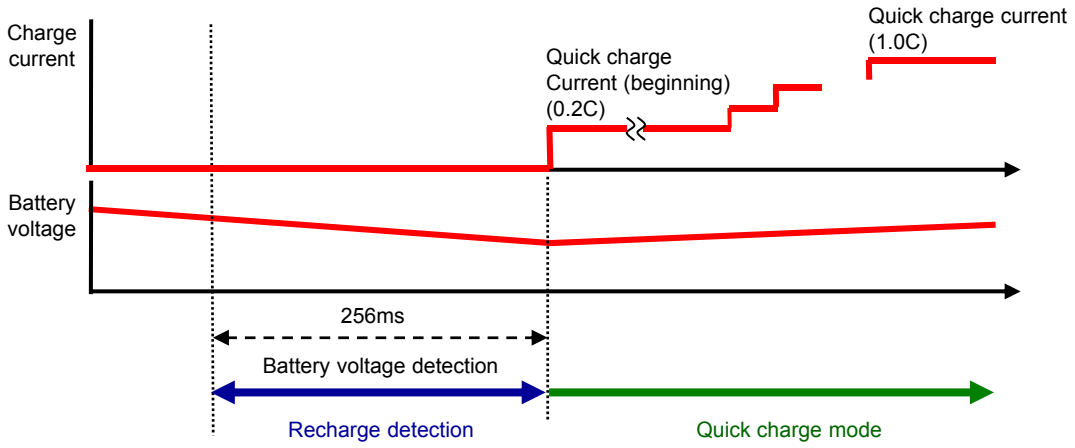


Function description

Recharge function

After charge completion, battery voltage continues to be monitored.
When $V_{BAT} < V_{rechg}$, recharge starts.
Quick charge timer also starts to operate when recharge starts.

Timing of recharge judgment



LED control (/STAT)

Mode	LED	Blink cycle	
Default	OFF	-	
Forced charge	ON	-	
Trickle charge	ON	-	
Quick charge	ON	-	
High temp. charge-1	ON	-	
High temp. charge-2	ON	-	
Charge completion detection	OFF	-	
Charge completion	OFF	-	
Error-1 *1	Blink 1	128ms	ON Duty 50%
Error-2 *1	Blink 2	1024ms	ON Duty 50%
Error-3 *1	Blink 2	1024ms	ON Duty 50%
Battery non-connection	OFF	-	

*1:Refer to the Charge state diagram

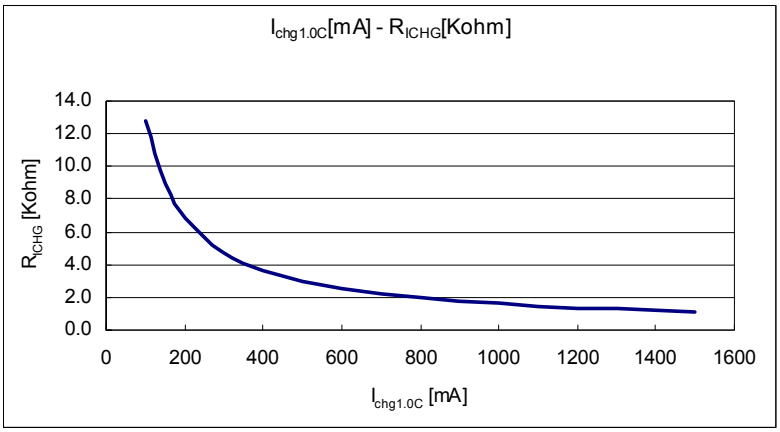
Function description

Charge Current Setting

Charge Current is set by the external resistance with RICHG terminal.
Here is the formula between R_{ICHG} and $I_{chg1.0C}$.

$$R_{ICHG} = 812 \times I_{chg1.0C}^{-0.9}$$

R_{ICHG} (Kohm) : External Resistance with RICHG
$I_{chg1.0C}$ (mA) : Quick charge setting



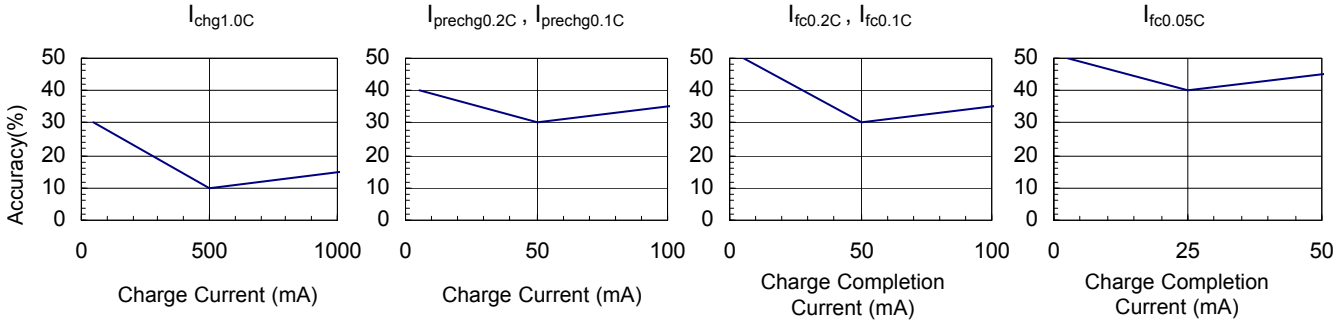
0.2C, 0.1C and 0.05C are 20%, 10% and 5% current of 1.0C.
They can be set by register (ADR=00H).

The accuracy of each current is as the following list.
Please use the current over 5mA.

Accuracy of each setting about charge current and charge completion current

Item	Quick Charge Current($I_{chg1.0C}$) Setting		
	500mA≤$I_{chg1.0C}$	$I_{chg1.0C}$=500mA	50mA≤$I_{chg1.0C}$<500mA
$I_{chg1.0C}$	+-[10+($I_{chg1.0C}$-500mA)/100mA] [%]	+-10[%]	+-[30+(50mA-$I_{chg1.0C}$)/22.5mA] [%]
$I_{prechg0.2C}$	+-[30+($I_{chg1.0C}$-500mA)/100mA] [%]	+-30[%]	+-[40+(50mA-$I_{chg1.0C}$)/45mA] [%]
$I_{prechg0.1C}$	+-[30+($I_{chg1.0C}$-500mA)/100mA] [%]	+- 30[%]	+-[40+(50mA-$I_{chg1.0C}$)/45mA] [%]
$I_{fc0.2C}$	+-[30+($I_{chg1.0C}$-500mA)/100mA] [%]	+- 30[%]	+-[50+(50mA-$I_{chg1.0C}$)/22.5mA] [%]
$I_{fc0.1C}$	+-[30+($I_{chg1.0C}$-500mA)/100mA] [%]	+- 30[%]	+-[50+(50mA-$I_{chg1.0C}$)/22.5mA] [%]
$I_{fc0.05C}$	+-[40+($I_{chg1.0C}$-500mA)/100mA] [%]	+- 40[%]	+-[50+(50mA-$I_{chg1.0C}$)/45mA] [%]

[Design guarantee except for Ichg=500mA]



Function description

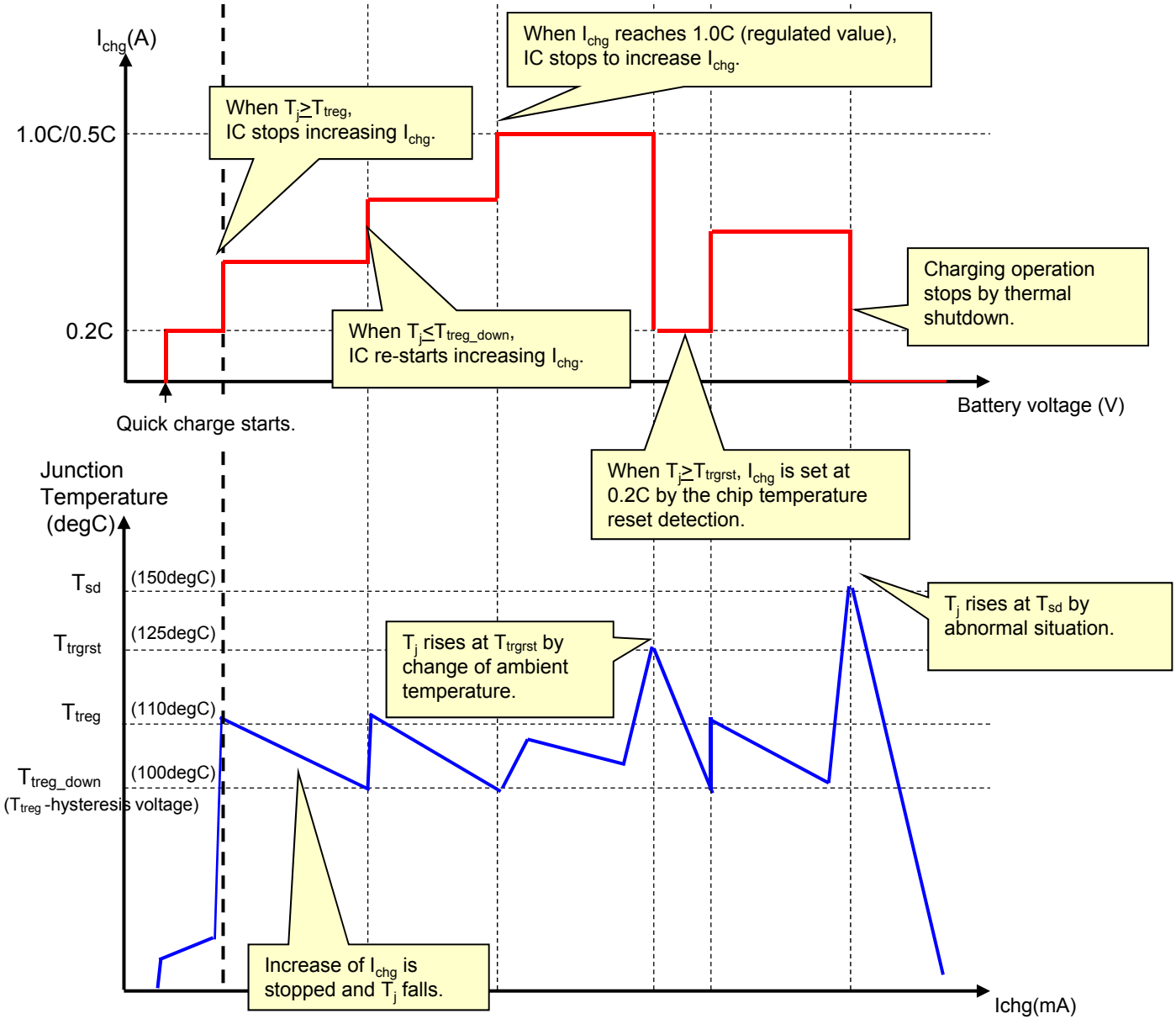
Chip temperature detection

During quick charge, junction temperature is monitored to limit charge current between 0.2C to 1.0C so that junction temperature may not exceed T_{treg}.

Thermal shutdown

When junction temperature reaches Tsd(default: 150degC) under charge, IC stops to supply from IN to SYS and the state moves to error mode.

Chip temperature detection and Thermal shutdown



Register Map

ADR		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	R/W	-	TRICKLE	FC		VCHG			ICHG
01H	R/W	USBMD	TIMER			CTL3			/CEN2
02H	R/W	SYSMODE		RST_USBDET	THBATCON	SGCTL	FULMD	RECHG	PSE
03H	R	GDBAT	VBATH	NOBAT	FULL	TOUT	TSD	POK	OVERLOAD
04H	R	TOUT_WKB	TOUT_DCD	USB			TEMP		
05H	R	0	0	0	0	STAT3	STAT2	STAT1	STAT0

03H State register (Read only)

	0	1	Condition of '1'
OVERLOAD	Not Overload	Overload	$V_{IN} < V_{HL}$
POK	Not Detect V_{IN}	Detect V_{IN}	/POK='L'
TSD	IC chip temperature is Normal	Thermal protection work (IC stop)	$T_j > T_{sd}$
TOUT	Timer normal	Time out (Charging stop)	Timeout of Trickle or Quick Charge timer
FULL	Charging not complete	Charging complete	$I_{chg} < I_{fc}$ (During CV)
NOBAT	Battery detected	No Battery	$V_{BAT} < V_{start}$
VBATH	Battery voltage normal	Battery over voltage	$V_{BAT} > V_{OV}$
GDBAT	Weak Battery	Good Battery	$V_{SYSSWOFF} < V_{BAT}$

05H<4> ~ <7> Keep 0
When charge FULL, FULL=0 and TOUT=0.
When Suspend, TSD=0,TOUT=0,FULL=0,VBATH=0,NOBAT=1.

04H TEMP register (Read only)

Bit2	Bit1	Bit0	TEMP
0	0	0	Temperature protection (Low Temp.)
0	0	1	Low rate charge (Low Temp.)
0	1	0	Normal charge
0	1	1	Low rate charge (High temp.)
1	0	0	Temperature protection (High temp.)
1	0	1	No Thermistor

04H USB detection result (Read only)

Bit5	Bit4	Bit3	USB
0	0	0	SDP (Standard Downstream Port)
0	0	1	CDP (Charging Downstream Port)
0	1	0	DCP (Dedicated Charging Port)
1	0	0	Divided Port 1
1	0	1	Divided Port 2
1	1	0	Divided Port 3
0	1	1	DP ERROR
1	1	1	DM ERROR

04H TOUT_WKB register (Read only)

Bit7	Weak Battery Timer
0	Normal
1	Time out

04H TOUT_DCD register (Read only)

Bit6	Connect Detection
0	Normal
1	Time out

05H State register (Read only)

STAT3	STAT2	STAT1	STAT0	State
0	0	0	0	Default
0	0	0	1	Forced charge
0	0	1	0	Trickle charge
0	0	1	1	Quick charge
0	1	0	0	High temp. charge-1
0	1	0	1	High temp. charge-2
0	1	1	0	Charge completion detection
0	1	1	1	Charge completion
1	0	0	0	Battery non-connection
1	0	0	1	Error-1
1	0	1	0	Error-2
1	0	1	1	Error-3

Register setting

***Default setting**

ADR=00H R/W	ICHG	Quick charge current	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		0.5C	-	-	-	-	-	-	-	0
		*1.0C	-	-	-	-	-	-	-	1
	VCHG	Charge control voltage	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		4.00V	-	-	-	-	0	0	0	-
		4.05V	-	-	-	-	0	0	1	-
		4.10V	-	-	-	-	0	1	0	-
		4.15V	-	-	-	-	0	1	1	-
		*4.20V	-	-	-	-	1	0	0	-
		No Use	-	-	-	-	1	0	1	-
			-	-	-	-	1	1	0	-
			-	-	-	-	1	1	1	-
	FC	Charge completion current	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		0.05C	-	-	0	0	-	-	-	-
		*0.1C	-	-	0	1	-	-	-	-
		0.2C	-	-	1	0	-	-	-	-
		No Use	-	-	1	1	-	-	-	-
	TRICKLE	Trickle charge current	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		*0.1C	-	0	-	-	-	-	-	-
		0.2C	-	1	-	-	-	-	-	-

ADR=01H R/W	/CEN2	Charger control *1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		*Enable	-	-	-	-	-	-	-	0
		Disable	-	-	-	-	-	-	-	1
	CTL3	Input current limitation *2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		*100mA	-	-	-	-	0	0	0	-
		500mA	-	-	-	-	0	0	1	-
		1000mA	-	-	-	-	0	1	0	-
		1500mA	-	-	-	-	0	1	1	-
		1800mA	-	-	-	-	1	0	0	-
		Limitless	-	-	-	-	1	0	1	-
		No Use	-	-	-	-	1	1	0	-
		SUSPEND	-	-	-	-	1	1	1	-
	TIMER	Timer control	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		Disable(reset)	-	0	0	0	-	-	-	-
		*Enable(normal)	-	0	0	1	-	-	-	-
		Enable(slow x 2) *3	-	0	1	0	-	-	-	-
		Enable(slow x 4) *4	-	0	1	1	-	-	-	-
		Enable(count stop) *5	-	1	0	0	-	-	-	-
		No Use	-	1	0	1	-	-	-	-
			-	1	1	0	-	-	-	-
			-	1	1	1	-	-	-	-
	USBMD	USB control select *2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		*Depend on Terminals	0	-	-	-	-	-	-	-
		Depend on Register	1	-	-	-	-	-	-	-

Register setting

ADR=02H R/W	PSE	PSE control	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		*Enable	-	-	-	-	-	-	-	0
		Disable	-	-	-	-	-	-	-	1
	RECHG	Recharge control	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		*Enable	-	-	-	-	-	-	0	-
		Disable	-	-	-	-	-	-	1	-
	FULMD	Operation after charge completion	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		*Stop charge	-	-	-	-	-	0	-	-
		Continue to charge(inform FULL)	-	-	-	-	-	1	-	-
	SGCTL	/SG control	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		*Enable	-	-	-	-	0	-	-	-
		Disable	-	-	-	-	1	-	-	-
	THBATCON	Battery detection by TH terminal	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		*Disable	-	-	-	0	-	-	-	-
		Enable	-	-	-	1	-	-	-	-
	RST_USBDET	USB detection reset	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		*Disable	-	-	0	-	-	-	-	-
		Enable (Reset)	-	-	1	-	-	-	-	-
	SYSMODE	SYS Output MODE *1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
		* V_{IN} pass-through	0	0	-	-	-	-	-	-
			0	1	-	-	-	-	-	-
		V_{SYS45} (Typ. 4.5V)	1	0	-	-	-	-	-	-
		V_{IN} pass-through	1	1	-	-	-	-	-	-

*1) When /CEN=L and /CEN2(register)='0', Charge operation is enable.

[Truth Table]

/CEN	/CEN2	Charge Operation
Lo	0	Charge start
Lo	1	Charge stop
Hi	0	Charge stop
Hi	1	Charge stop

*2) When USBMD=0, Terminal setting(USUP) is available. When USBMD=1, Register(CTL3) is available and the suspend function by Weak battery timer is unavailable.
Re-connect with IN when going into the suspend mode by Weak battery timer.

*3) Slow: 2 times of normal mode(Trickle charge timer=120min., Quick charge timer=600min , Weak battery timer = 80min.)

*4) Slow: 4 times of normal mode(Trickle charge timer=240min., Quick charge timer=1200min , Weak battery timer = 160min.)

*5) Count stop : Timer is suspended.(Not reset)

*6) When RST_USB=1, the USB detecting is in reset and /SG output is 'L'.
When RST_USB=0, the USB detecting will restart.
During the USB detection, /SG is 'H'.
After USB detection, /SG output is determined by the SG function.
USB re-detection by RST_USBDET can reset the suspend by USB detecting error.

*7) The SYS voltage setting can be set by the SYSMODE register.

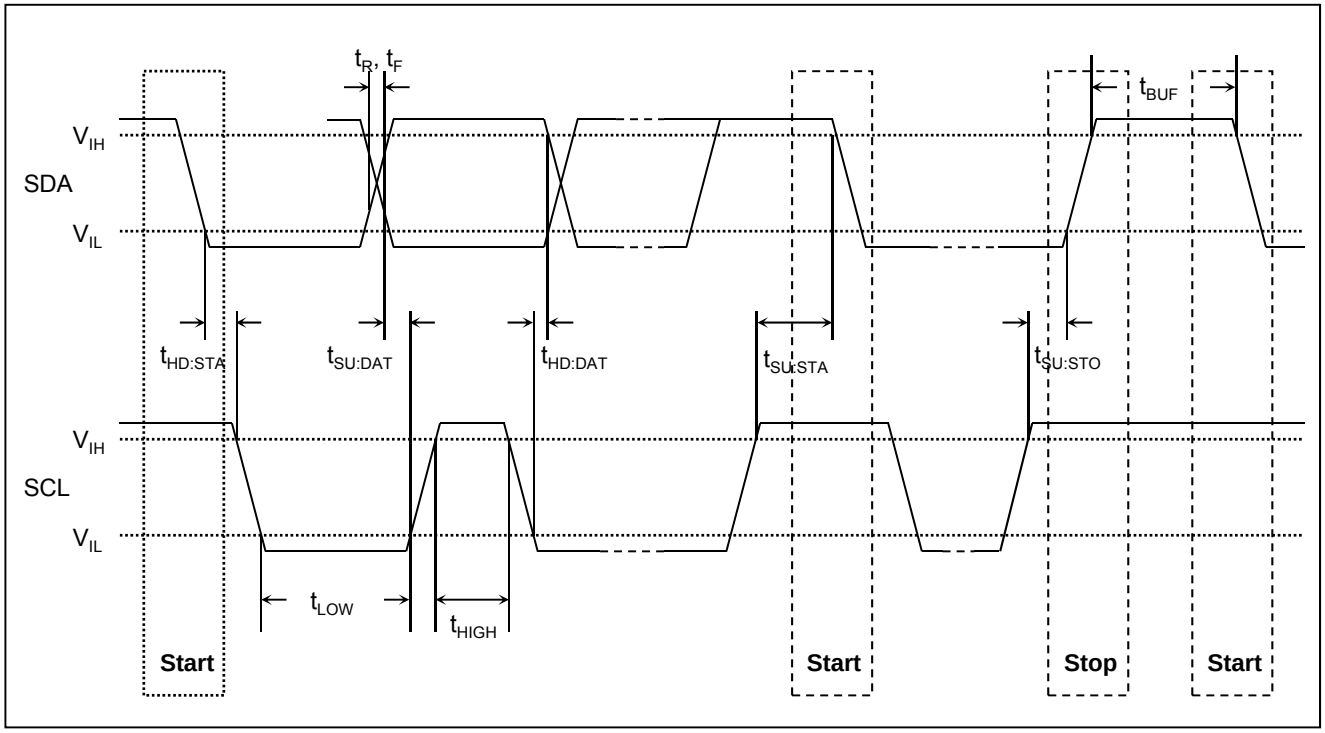
* When V_{IN}<2.0V, the register is reset. (This value is design guarantee).

I²C BUS Line Characteristics

Symbol	Item	Min.	Max.	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
t_{BUF}	Bus free time between STOP condition and START condition	1.3	-	µs
$t_{HD:STA}$	START condition hold time (After this period, the first clock pulse is generated)	0.6	-	µs
t_{LOW}	SCL low period	1.3	-	µs
t_{HIGH}	SCL high period	0.6	-	µs
$t_{SU:STA}$	START condition setup time	0.6	-	µs
$t_{HD:DAT}$	Data hold time	0	0.9	µs
$t_{SU:DAT}$	Data setup time	100	-	ns
t_R	Rise time (SDA and SCL)	-	300	ns
t_F	Fall time (SDA and SCL)	-	300	ns
$t_{SU:STO}$	STOP condition setup time	0.6	-	µs
C_b	Bus line capacitive load	-	400	pF

Note : Above values are specified by V_{IH}min and V_{IL}max.

I²C Timing Chart

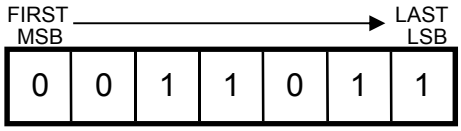


Serial communication format

1. Start condition

Set SDA from High to Low when SCL=High.

2. Slave address



3. Stop condition

Set SDA from Low to High when SCL=High.

4. Read/Write code

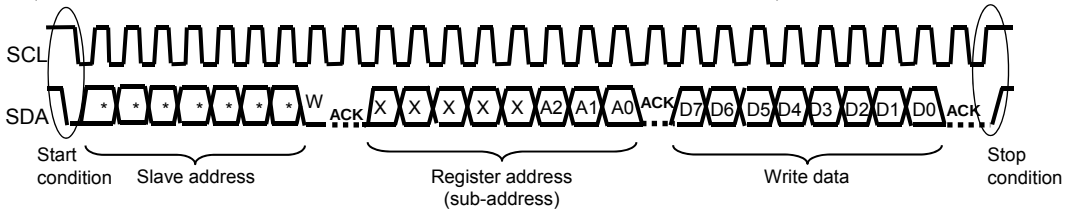
Write code : SDA=Low
Read code : SDA=High

5. Write mode :Data input from Master to R2A20056

R2A20056 will respond with an Acknowledge '0' when;
- Master inputs Slave address (8bit) and Write code after start condition
- Master inputs Register address (8bit)
- Master inputs Write data (8bit)

Lastly, Master will input Stop condition.

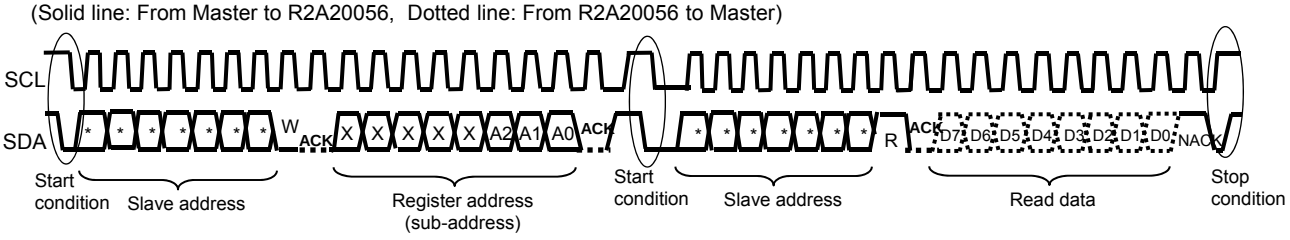
(Solid line: From Master to R2A20056, Dotted line: From R2A20056 to Master)



6. Read mode :Data output from R2A20056 to Master

When Master inputs Slave address(8bit) and Write code after start condition, R2A20056 responds with an Acknowledge'0'.
And then, when Master inputs Register address(8bit), R2A20056BM responds with an Acknowledge'0'.
And then, when Master inputs Start condition, Slave address, and Read code, R2A20056 responds with an Acknowledge'0' and outputs Read data.
Lastly, Master inputs Acknowledge'1'(or opens bus line) and Stop condition.

(Solid line: From Master to R2A20056, Dotted line: From R2A20056 to Master)



Serial communication format

[Pull-down resistance with 'SCL' and 'SDA' terminals]

There are pull-down resistances with 'SCL' and 'SDA' terminals in this IC.

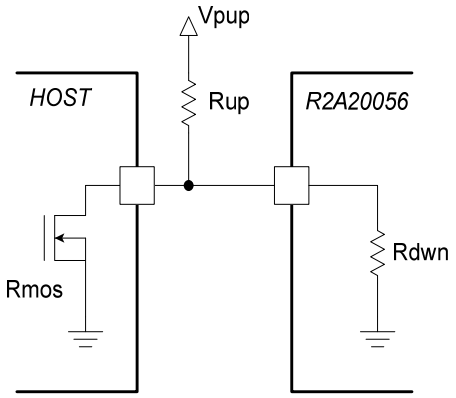
Item	Rated Value			Unit
	Min.	Typ.	Max.	
pull-down Resistance of SCL,SDA	500	700	900	KΩ

Please set the pull-up resistances to satisfy the calculating formula.

V_{pup}[V] : Pull-up voltage

R_{up}[KΩ] : Pull-up resistance

R_{mos}[KΩ] : ON resistance of NMOS in HOST



[The circuit around SDA, SCL terminals]

< 'H' voltage >

$$V_H = V_{pup} \times \frac{R_{dwn}}{R_{up} + R_{dwn}}$$

R_{dwn} is affected lightly because of $R_{up} << R_{dwn}$.

< 'L' voltage>

$$V_L = V_{pup} \times \frac{(R_{mos} // R_{dwn})}{R_{up} + (R_{mos} // R_{dwn})}$$

R_{dwn} is affected lightly because of $R_{mos} << R_{dwn}$.

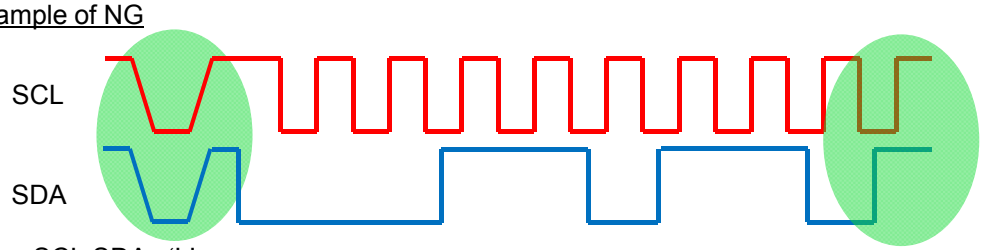
[I2C communication notice]

If 'L' signal is input to 'SCL' and 'SDA' terminals before normal I2C signal, this IC may not accept this I2C signal because of detecting 'Start condition'.
When the pull-up voltage is turned off during continuing to supply voltage to the IN terminal, the 'L' signal may be miss-detected as the start condition.
Please take measures as follows:

Resending the command in the error
Please resend the command when ACK is not returned normally.

Timing adjust when turning off the pull-up power supply
Please make 'SCL' fall faster than 'SDA' when pull-up power is turned off while voltage is supplied to the IN terminal.

The example of NG

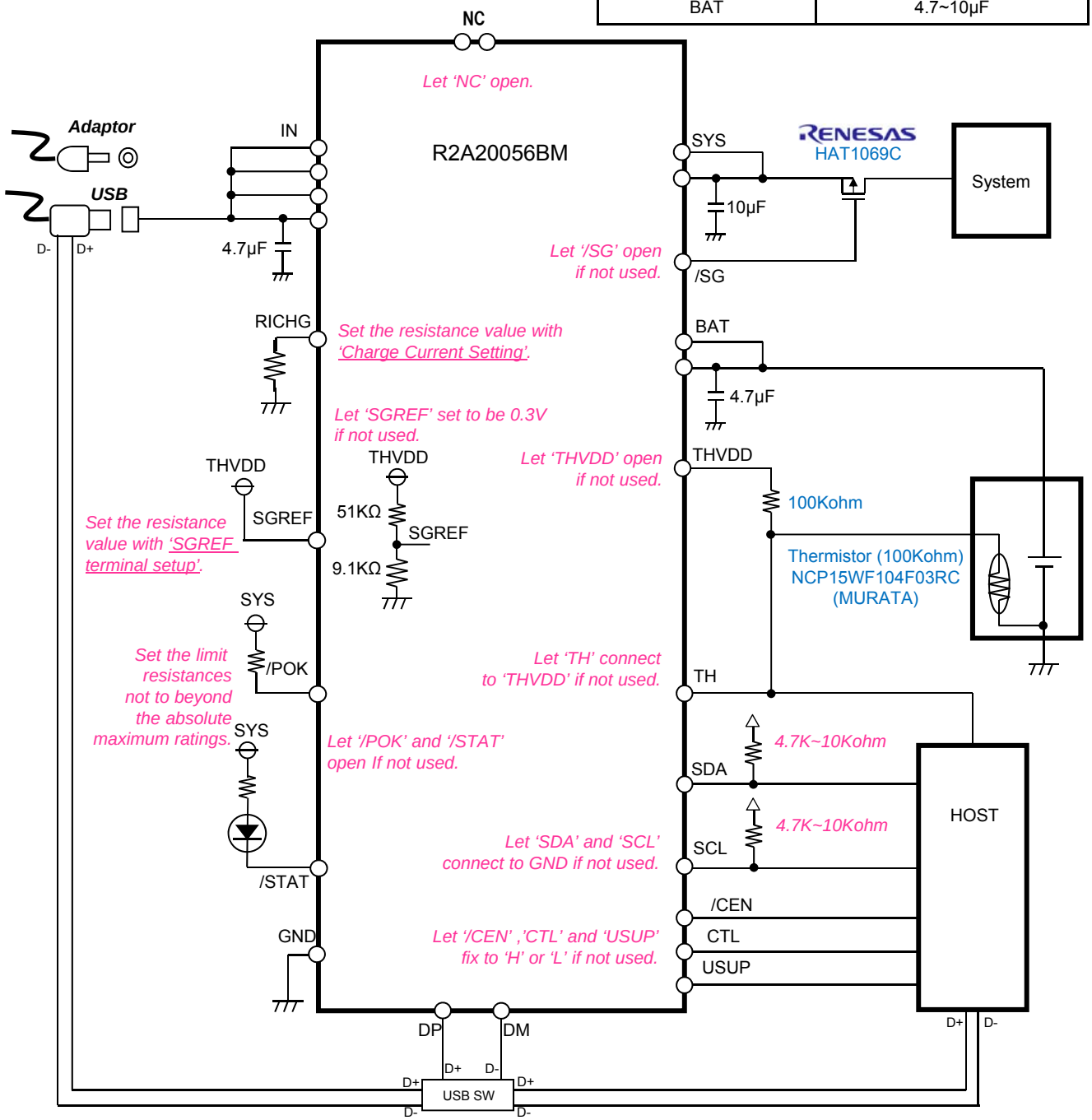


SCL,SDA : 'L'
=> Miss-detecting as 'START CONDITION'

No 'ACK'

Typical Application Circuit

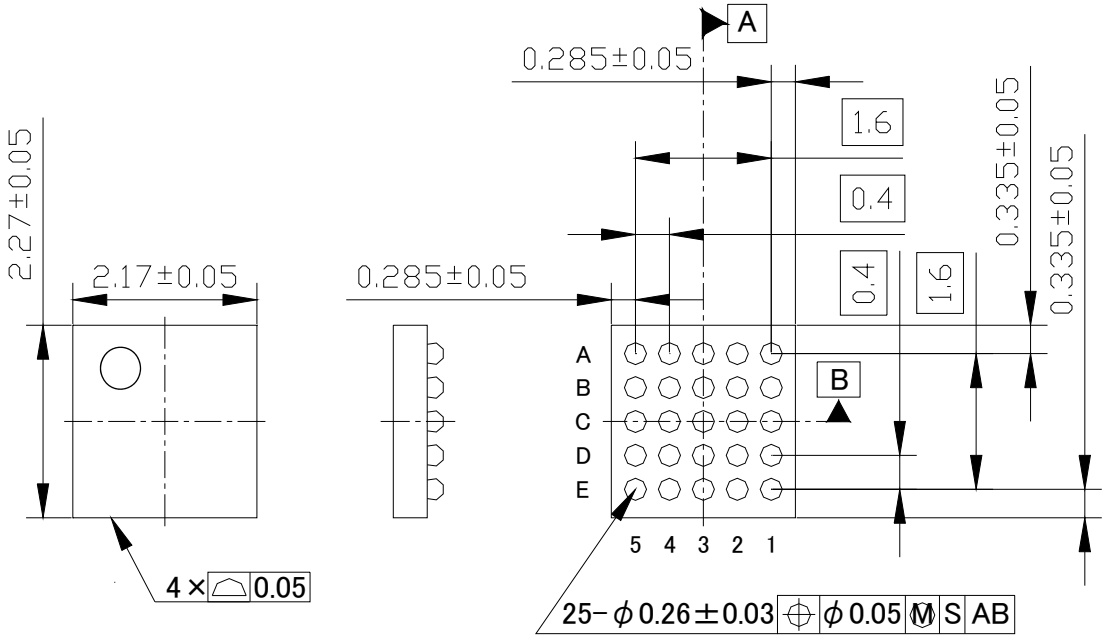
Terminal Name	Recommended Capacitance
IN	4.7~10µF
SYS	10µF
BAT	4.7~10µF

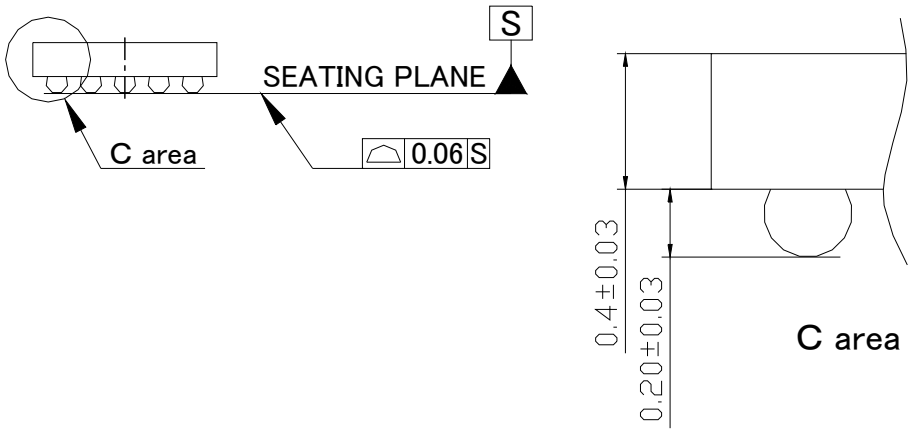


Port is detected by 'DP' and 'DM' terminals.
Set the port setting as the desired current limit value if not used.
Usage Example) SDP : 20Kohm pull-down resistance with 'DP' and 'DM'
DCP : Connect 'DP' and 'DM' to each other

Package dimensions

Unit:mm





Usage Note

Please do not connect ‘SYS’ terminal to GND.
If ‘SYS’ terminal is connected with GND in battery connection mode, large currents flow from ‘BAT’ to ‘SYS’ through the body diode in MOS-FET between BAT and SYS. If large current continues to flow, it causes power dissipation in the IC to increase. The IC will then heat up and may damage the IC. The heat may also cause the IC to burn.

If the battery completion is detected at ‘FULMD’=‘1’ (ADR=02H Bit=2), ‘FULL’ (ADR=03H Bit=4) becomes ‘1’ but charging continues. Timer also continues after ‘FULL’ becomes ‘1’.So charging stops after quick charge timer ends even at ‘FULMD’=‘1’. Timer can be stopped by ‘COUNT STOP’ (ADR=01H Bit 4~6).

Trickle timer stops when the battery voltage is below V_{start}. When BAT is shorted, this timer also stops. NOBAT(ADR=03H, Bit5) indicates detecting the battery voltage below V_{start}. After NOBAT=‘1’ by detecting $V_{BAT} \leq V_{start}$, please stop charging with /CEN.

Please do not apply voltage and current exceeding the absolute maximum ratings. It may damage the IC.

Please use this device within the power dissipation not exceeding the allowable range of this package.

When the charging starts with no battery at low V_{IN} voltage, it has possibilities for oscillation to occur. Please don’t start to charge with no battery.

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