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April 1st, 2010
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1. Overview

The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) is a single-chip control MCU, fabricated using high-performance silicon gate CMOS technology, embedding the M16C/60 Series CPU core. The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) is housed in 42-pin and 48-pin plastic molded packages. With a 1M byte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) has a multiplier and DMAC adequate for office automation, communication devices and industrial equipment, and other high-speed processing applications.

1.1 Applications

Audio, cameras, office/communications/portable/ equipment, air-conditioning equipment, home appliances, etc.

1.2 Performance Outline

Table 1.1 and **1.2** outline performance overview of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T).

Table 1.1. M16C/26A Group(M16C/26A, M16C/26B, M16C/26T) Performance (48-Pin Package)

Item		Specification
CPU	Basic instructions	91 instructions
	Minimun instruction execution time	41.7 ns (f(BCLK) = 24MHz(4), Vcc = 4.2 to 5.5 V) (M16C/26B) 50 ns (f(BCLK) = 20MHz, Vcc = 3.0 to 5.5 V) (M16C/26A, M16C/26B, M16C/26T(T-ver.)) 100 ns (f(BCLK) = 10MHz, Vcc = 2.7 to 5.5 V) (M16C/26A , M16C/26B) 50 ns (f(BCLK) = 20MHz, Vcc = 4.2 to 5.5 V -40 to 105°C) (M16C/26T(V-ver.)) 62.5 ns (f(BCLK) = 16MHz, Vcc = 4.2 to 5.5 V -40 to 125°C) (M16C/26T(V-ver.))
	Operating mode	Single-chip mode
	Address space	1 Mbyte
	Memory capacity	See **1.4 Product Information**
Peripheral Function	I/O ports	39 I/O pins
	Multifunction timers	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase motor control timer
	Serial I/O	2 channels (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous, I2C bus(1) , or IEBus(2))
	A/D converter	10 bit A/D Converter : 1 circuit, 12 channels
	DMAC	2 channels
	CRC calcuration circuit	1 circuit (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupts	20 internal and 8 external sources, 4 software sources, Interrupt priority level: 7
	Clock generation circuit	4 circuits Main clock oscillation circuit(*), Sub-clock oscillation circuit(*) On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resister.
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function
	Voltage detection circuit	On-chip (M16C/26A, M16C/26B), not on-chip (M16C/26T)
Electrical Characteristics	Power supply voltage	Vcc = 4.2 to 5.5 V (f(BCLK) = 24 MHz)(4) (M16C/26B)
		Vcc = 3.0 to 5.5 V (f(BCLK) = 20 MHz) (M16C/26A, M16C/26B) Vcc = 2.7 to 5.5 V (f(BCLK) = 10 MHz)
		Vcc = 3.0 to 5.5 V (M16C/26T(T-ver.))
		Vcc = 4.2 to 5.5 V (M16C/26T(V-ver.))
	Power consumption	16 mA (Vcc = 5 V, f(BCLK) = 20 MHz) 25 µA (f(XCIN) = 32 KHz on RAM) 3 µA (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode) 0.7 µA (Vcc = 3 V, in stop mode)
Flash Memory Version	Programming /erasure voltage	2.7 to 5.5 V (M16C/26A, M16C/26B) 3.0 to 5.5 V (M16C/26T(T-ver.)) 4.2 to 5.5 V (M16C/26T(V-ver.))
	Programming /erasure endurance	100 times (all area) or 1,000 times (block 0 to 3) / 10,000 times (block A, block B)(3)
Operating Ambient Temperature		-20 to 85°C / -40 to 85°C (3) (M16C/26A , M16C/26B)
		-40 to 85°C (M16C/26T(T-ver.))
		-40 to 105°C / -40 to 125°C (M16C/26T(V-ver.))
Package		48-pin plastic molded QFP

NOTES:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. See **Table 1.7 Product Code** for the program and erase endurance, and operating ambient temperature.
4. The PLL frequency synthesizer is used to run the M16C/26B at f(BCLK) = 24 MHz.

Table 1.2. Performance outline of M16C/26A group (M16C/26A, M16C/26B) (42-pin device)

	Item	Performance
CPU	Basic instructions	91 instructions
	Minimun instruction execution time	41.7 ns (f(BCLK) = 24 MHz (4), VCC = 4.2 to 5.5 V (M16C/26B) 50 ns (f(BCLK) = 20 MHz, Vcc = 3.0 to 5.5 V) (M16C/26A, M16C/26B) 100 ns (f(BCLK) = 10 MHz, Vcc = 2.7 to 5.5 V) (M16C/26A, M16C/26B)
	Operation mode	Single-chip mode
	Address space	1M byte
	Memory capacity	See **1.4 Product Information**
Peripheral function	Port	33 I/O pins
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 3 channels Three-phase motor control timer
	Serial I/O	1 channel (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous, I^2C bus(1) , or IEBus(2))
	A/D converter	10 bit A/D converter: 1 circuit, 10 channels
	DMAC	2 channels
	CRC calcuration circuit	1 circuits (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	18 internal and 8 external sources, 4 software sources, Interrupt priority level: 7
	Clock generation circuit	4 circuits Main clock(*), Sub-clock(*) On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resister.
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function
	Voltage detection circuit	On-chip
Electrical Characteristics	Supply voltage	Vcc = 4.2 to 5.5 V (f(BCLK) = 24 MHz)(4) (M16C/26B)
		Vcc = 3.0 to 5.5 V (f(BCLK) = 20 MHz) (M16C/26A, M16C/26B) Vcc = 2.7 to 5.5 V (f(BCLK) = 10 MHz)
	Power Consumption	16 mA (Vcc = 5 V, f(BCLK) = 20 MHz) 25 μA (f(XCIN) = 32 KHz on RAM) 3 μA (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode) 0.7 μA (Vcc = 3 V, in stop mode)
Flash memory	Programming/erasure voltage	2.7 to 5.5 V
	Programming/erasure endurance	100 times (all area) or 1,000 times (block 0 to 3) / 10,000 times (block A, block B)(3)
Operating Ambient Temperature		-20 to 85°C / -40 to 85°C (3)
Package		42-pin plastic molded SSOP

NOTES:
1. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. See **Table 1.7 Product Code** for the program and erase endurance, and operating ambient temperature.
4. The PLL frequency synthesizer is used to run the M16C/26B at f(BCLK) = 24 MHz.

1.3 Block Diagram

Figure 1.1 and **1.2** show block diagrams of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) 48-pin package and 42-pin package.

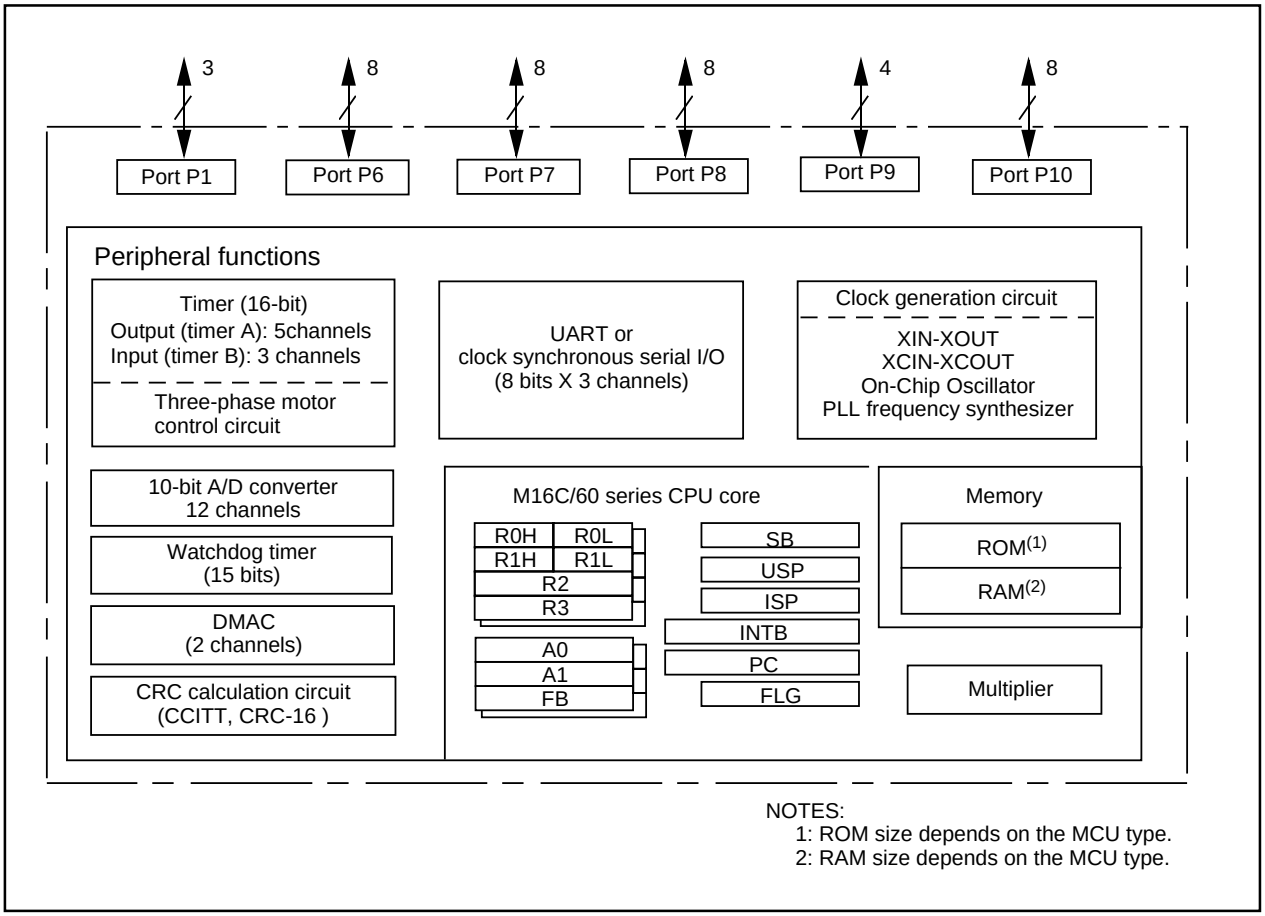


Figure 1.1 Block Diagram(48-pin Package)

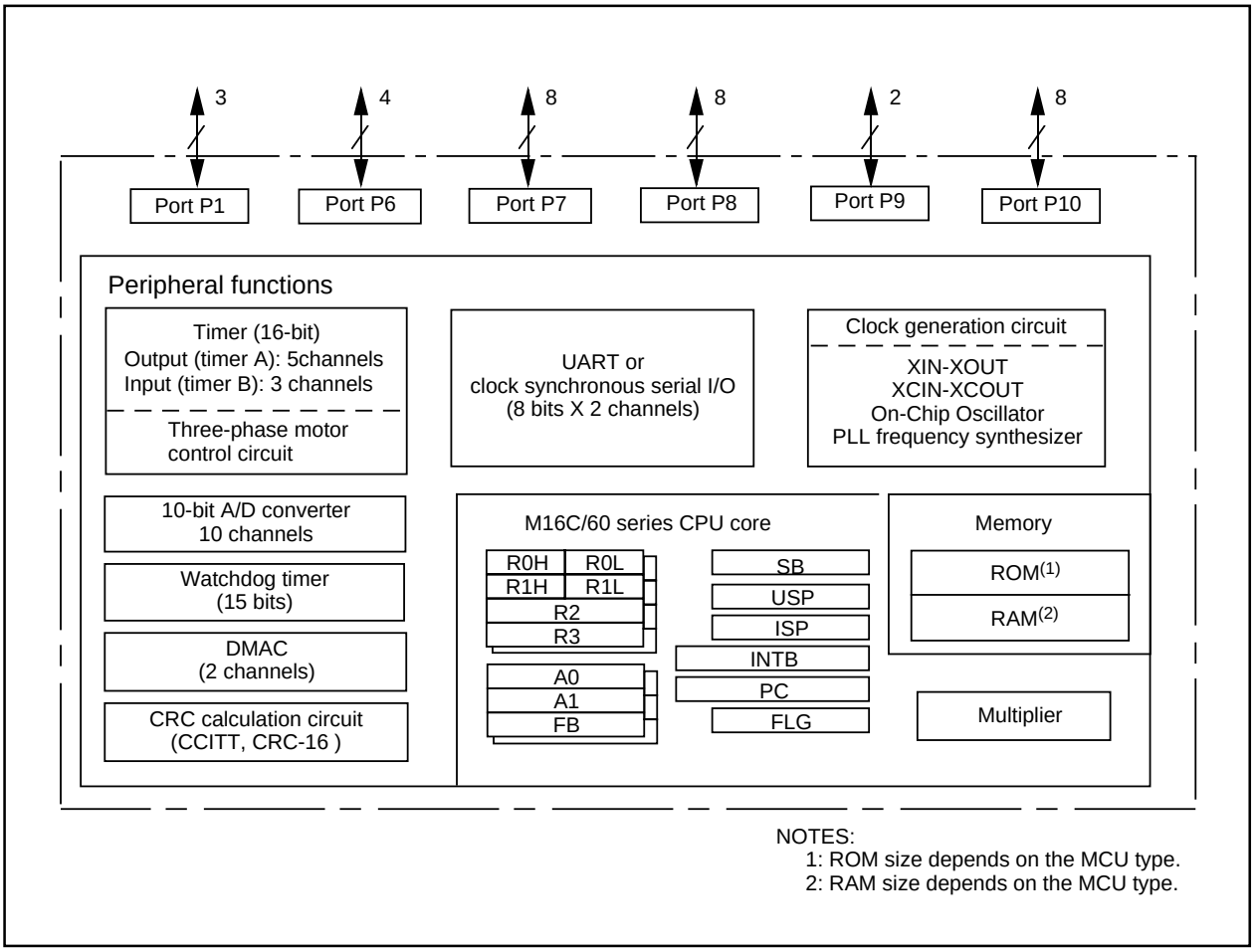


Figure 1.2 Block Diagram(42-pin Package)

1.4 Product List

Tables 1.3 to **1.6** lists product information, **Figure 1.3** shows a product numbering system, **Table 1.7** lists the product code, and **Figure 1.4** shows the marking.

Table 1.3 M16C/26A **Current as of Jul., 2006**

Type Number		ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30260F3AGP	(N)	24K + 4K	1K	PLQP0048KB-A (48P6Q-A)	Flash memory	U3, U5, U7, U9
M30260F6AGP	(N)	48K + 4K	2K			
M30260F8AGP	(N)	64K + 4K	2K			
M30263F3AFP	(N)	24K + 4K	1K	PRSP0042GA-B (42P2R)		U5, U9
M30263F6AFP	(N)	48K + 4K	2K			
M30263F8AFP	(N)	64K + 4K	2K			
M30260M3A-XXXGP	(N)	24K	1K	PLQP0048KB-A (48P6Q-A)	Mask ROM	U3, U5
M30260M6A-XXXGP	(N)	48K	2K			
M30260M8A-XXXGP	(N)	64K	2K			
M30263M3A-XXXFP	(N)	24K	1K	PRSP0042GA-B (42P2R)		U5
M30263M6A-XXXFP	(N)	48K	2K			
M30263M8A-XXXFP	(N)	64K	2K			

(N): New

Table 1.4 M16C/26B **Current as of Jul., 2006**

Type Number		ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30260F8BGP	(D)	64K + 4K	2K	PLQP0048KB-A (48P6Q-A)	Flash memory	U7
M30263F8BFP	(D)	64K + 4K	2K	PRSP0042GA-B (42P2R)		U9

(D): Under development

Table 1.5 M16C/26T T-ver. **Current as of Jul., 2006**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30260F3TGP	24K + 4K	1K	PLQP0048KB-A (48P6Q-A)	Flash memory	U3, U7
M30260F6TGP	48K + 4K	2K			
M30260F8TGP	64K + 4K	2K			

NOTE:
1. Please contact Renesas Technolog Corp. for details on Mask ROM version.

Table 1.6 M16C/26T V-ver. **Current as of Jul., 2006**

Type Number	ROM Capacity	RAM Capacity	Package	Remarks	Product Code
M30260F3VGP	24K + 4K	1K	PLQP0048KB-A (48P6Q-A)	Flash memory	U3, U7
M30260F6VGP	48K + 4K	2K			
M30260F8VGP	64K + 4K	2K			

NOTE:
1. Please contact Renesas Technolog Corp. for details on Mask ROM version.

Type No. M 3 0 2 6 0 M 8 A - XXX G P - U3

Product code:
See **Tables 1.7 to 1.10**

Package type:
GP: PLQP0048KB-A (48P6Q) (M16C/26A, M16C/26B, M16C/26T)
FP: PRSP0042GA-B (42P2R) (M16C/26A, M16C/26B)

ROM number:
ROM number is omitted in flash memory version

Version:
A : M16C/26A
B : M16C/26B
T : M16C/26T T-ver.
V : M16C/26T V-ver.

ROM / RAM capacity:
3: (24K+4K) bytes (Note 1) / 1K bytes
6: (48K+4K) bytes (Note 1) / 2K bytes
8: (64K+4K) bytes (Note 1) / 2K bytes
Note 1: Only flash memory version exists in "+4K bytes"

Memory type:
M: Mask ROM version
F: Flash memory version

Pin count (The value itself has no specific meaning)

M16C/26A Group

M16C Family

Figure 1.3 Product Numbering System

Table 1.7 Product Code (Flash Memory Version) - M16C/26A, M16C/26B

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead free	100	0 to 60ºC	100	0 to 60ºC	-40 to 85ºC
U5						-20 to 85ºC
U7		1,000		10,000	-40 to 85ºC	-40 to 85ºC
U9					-20 to 85ºC	-20 to 85ºC

Table 1.8 Product Code (Mask ROM Version - M16C/26A)

Product Code	Package	Operating Ambient Temperature
U3	Lead free	-40ºC to 85ºC
U5		-20ºC to 85ºC

NOTE:

1. The lead contained products, D3, D5, D7, and D9 are put together with U3, U5, U7, and U9 respectively. Lead-free products can be mounted by both conventional Sn-Pb paste and Lead-free paste (Sn-Ag-Cu plating).

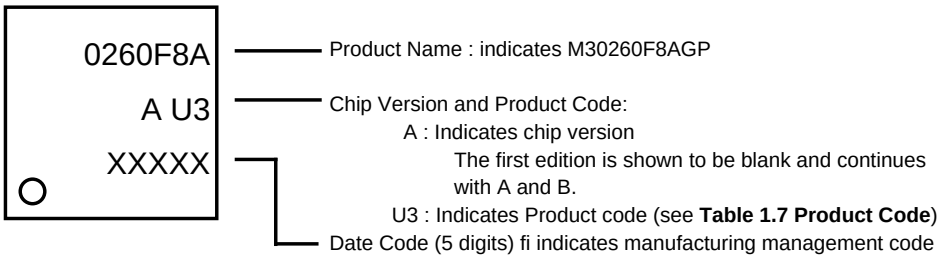
Table 1.9 Product Code (Flash Memory Version) - M16C/26T T-ver.

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temerature
		Programming and erasure endurance	Temperature range	Programming and erasure endurance	Temperature range	
U3	Lead free	100	0ºC to 60ºC	100	-40ºC to 85ºC	-40ºC to 85ºC
U7		1,000		10,000		

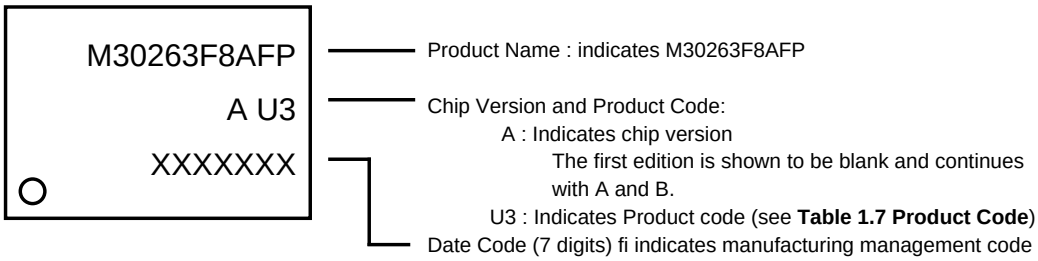
Table 1.10 Product Code (Flash Memory Version) - M16C/26T V-ver.

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temerature
		Programming and erasure endurance	Temperature range	Programming and erasure endurance	Temperature range	
U3	Lead free	100	0ºC to 60ºC	100	-40ºC to 125ºC	-40ºC to 125ºC
U7		1,000		10,000		

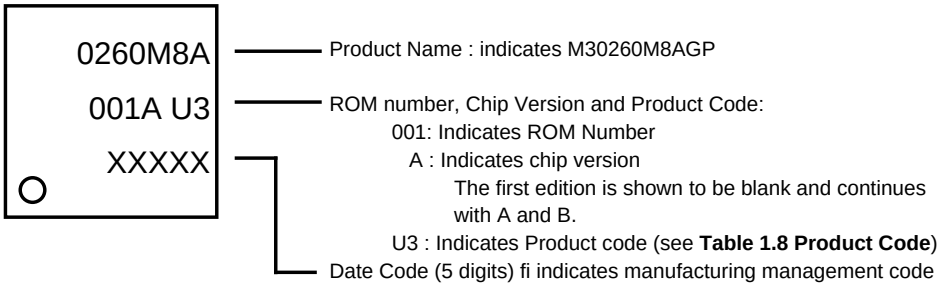
(1) Flash memory version, PLQP0048KB-A (48P6Q), M16C/26A, M16C/26B



(2) Flash memory version, PRSP0042GA-B (42P2R), M16C/26A, M16C/26B



(3) MASK ROM version, PLQP0048KB-A (48P6Q), M16C/26A



(4) MASK ROM version, PRSP0042GA-B (42P2R), M16C/26A

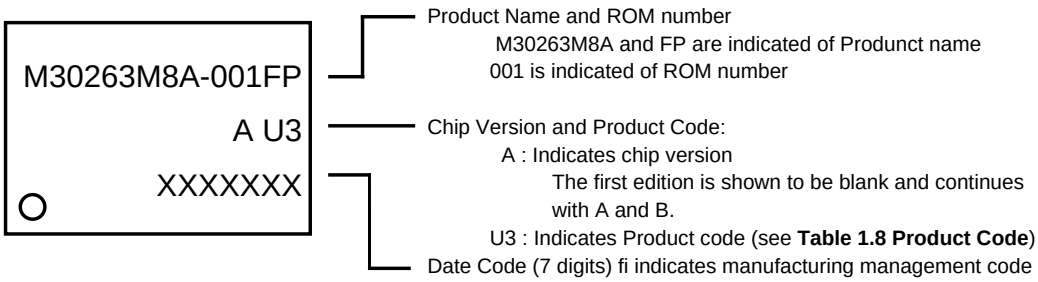
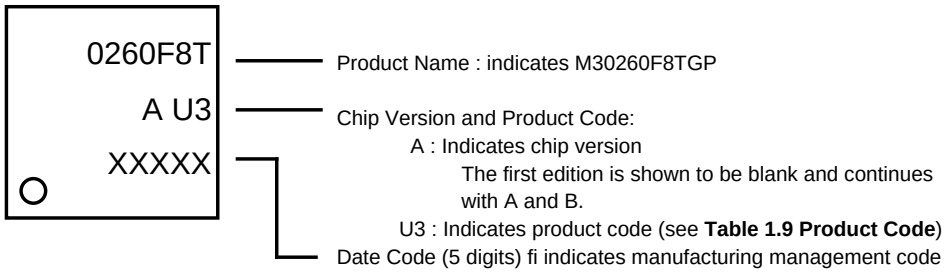


Figure 1.4 Marking Diagram (M16C/26A , M16C/26B)

(1) Flash memory version, PLQP0048KB-A (48P6Q), M16C/26T T-ver.



(2) Flash memory version, PLQP0048KB-A (48P6Q), M16C/26T V-ver.

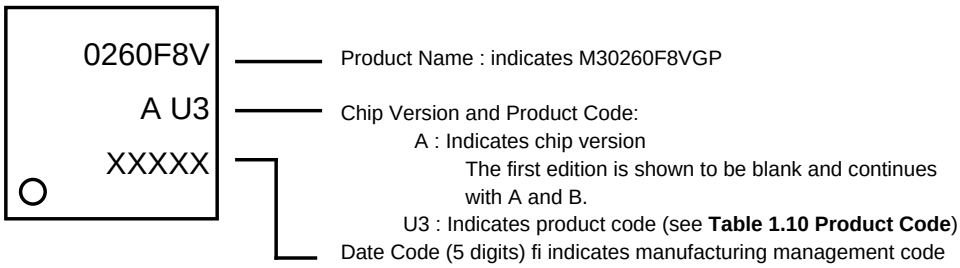


Figure 1.5 Marking Diagram (M16C/26T)

1.5 Pin Assignments

Figures 1.6 and **1.7** show the Pin Assignments (top view).

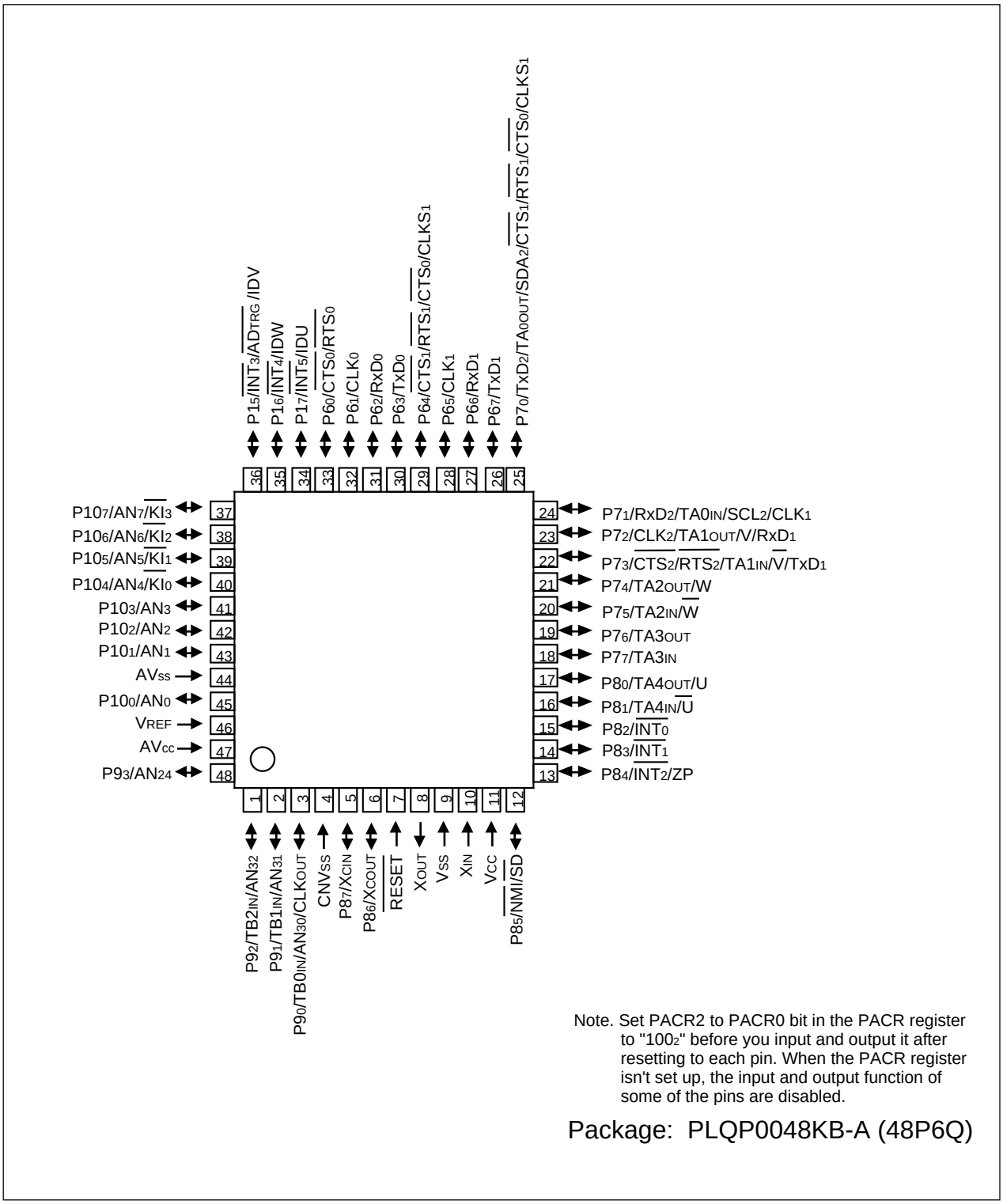
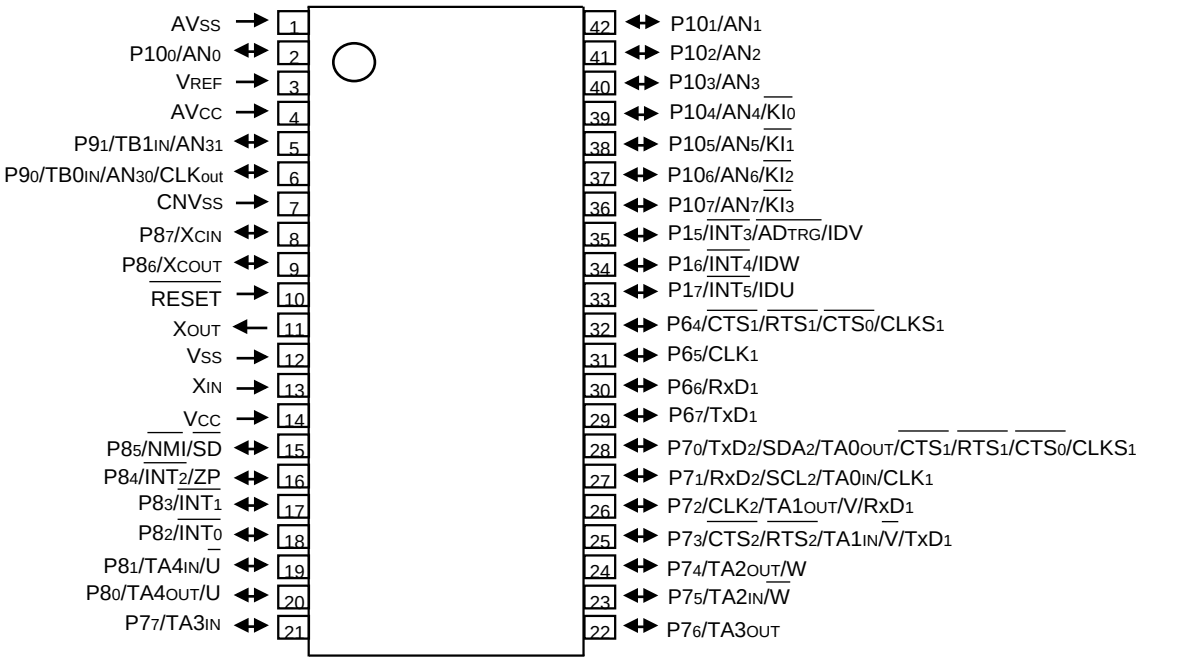


Figure 1.6 Pin Assignment for 48-Pin Package (Top View)

Table 1.11 Pin Characteristics for 48-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin
1		$P9_2$		TB_{2IN}		$AN3_2$
2		$P9_1$		TB_{1IN}		$AN3_1$
3		$P9_0$		TB_{0IN}	CLK_{OUT}	$AN3_0$
4	CNV_{SS}					
5	X_{CIN}	$P8_7$				
6	X_{COUT}	$P8_6$				
7	$\overline{RESET}$					
8	X_{OUT}					
9	V_{SS}					
10	X_{IN}					
11	V_{CC}					
12		$P8_5$	$\overline{NMI}$	$\overline{SD}$		
13		$P8_4$	$\overline{INT_2}$	ZP		
14		$P8_3$	$\overline{INT_1}$			
15		$P8_2$	$\overline{INT_0}$			
16		$P8_1$		TA_{4IN} / $\overline{U}$		
17		$P8_0$		TA_{4OUT} / U		
18		$P7_7$		TA_{3IN}		
19		$P7_6$		TA_{3OUT}		
20		$P7_5$		TA_{2IN} / $\overline{W}$		
21		$P7_4$		TA_{2OUT} / W		
22		$P7_3$		TA_{1IN} / $\overline{V}$	$\overline{CTS_2}$ / $\overline{RTS_2}$ / TxD_1	
23		$P7_2$		TA_{1OUT} / V	CLK_2 / RxD_1	
24		$P7_1$		TA_{0IN}	RxD_2 / SCL_2 / CLK_1	
25		$P7_0$		TA_{0OUT}	TxD_2 / SDA_2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $CLKS_1$	
26		$P6_7$			TxD_1	
27		$P6_6$			RxD_1	
28		$P6_5$			CLK_1	
29		$P6_4$			$\overline{RTS_1}$ / $\overline{CTS_1}$/ $\overline{CTS_0}$ / $CLKS_1$	
30		$P6_3$			TxD_0	
31		$P6_2$			RxD_0	
32		$P6_1$			CLK_0	
33		$P6_0$			$\overline{RTS_0}$ / $\overline{CTS_0}$	
34		$P1_7$	$\overline{INT_5}$	IDU		
35		$P1_6$	$\overline{INT_4}$	IDW		
36		$P1_5$	$\overline{INT_3}$	IDV		$\overline{AD_{TRG}}$
37		$P10_7$	$\overline{KI_3}$			AN_7
38		$P10_6$	$\overline{KI_2}$			AN_6
39		$P10_5$	$\overline{KI_1}$			AN_5
40		$P10_4$	$\overline{KI_0}$			AN_4
41		$P10_3$				AN_3
42		$P10_2$				AN_2
43		$P10_1$				AN_1
44	AV_{SS}					
45		$P10_0$				AN_0
46	V_{REF}					
47	AV_{CC}					
48		$P9_3$				$AN2_4$



Note. Set PACR2 to PACR0 bit in the PACR register to "001$_2$" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PRSP0042GA-B (42P2R)

Figure 1.7 Pin Assignment for 42-Pin Package (Top View)

Table 1.12 Pin Characteristics for 42-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin
1	AVss					
2		$P10_0$				AN_0
3	V_{REF}					
4	AVcc					
5		$P9_1$		TB_{1IN}		$AN3_1$
6		$P9_0$		TB_{0IN}	CLK_{OUT}	$AN3_0$
7	CNVss					
8	X_{CIN}	$P8_7$				
9	X_{COUT}	$P8_6$				
10	$\overline{RESET}$					
11	X_{OUT}					
12	Vss					
13	X_{IN}					
14	Vcc					
15		$P8_5$	$\overline{NMI}$	$\overline{SD}$		
16		$P8_4$	$\overline{INT_2}$	ZP		
17		$P8_3$	$\overline{INT_1}$			
18		$P8_2$	$\overline{INT_0}$			
19		$P8_1$		TA_{4IN} / $\overline{U}$		
20		$P8_0$		TA_{4OUT} / U		
21		$P7_7$		TA_{3IN}		
22		$P7_6$		TA_{3OUT}		
23		$P7_5$		TA_{2IN} / $\overline{W}$		
24		$P7_4$		TA_{2OUT} / W		
25		$P7_3$		TA_{1IN} / $\overline{V}$	$\overline{CTS_2}$ / $\overline{RTS_2}$ / TxD_1	
26		$P7_2$		TA_{1OUT} / V	CLK_2 / RxD_1	
27		$P7_1$		TA_{0IN}	RxD_2 / SCL_2 / CLK_1	
28		$P7_0$		TA_{0OUT}	TxD_2 / SDA_2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $CLKS_1$	
29		$P6_7$			TxD_1	
30		$P6_6$			RxD_1	
31		$P6_5$			CLK_1	
32		$P6_4$			$\overline{RTS_1}$ / $\overline{CTS_1}$/ $\overline{CTS_0}$ / $CLKS_1$	
33		$P1_7$	$\overline{INT_5}$	IDU		
34		$P1_6$	$\overline{INT_4}$	IDW		
35		$P1_5$	$\overline{INT_3}$	IDV		$\overline{ADTRG}$
36		$P10_7$	$\overline{KI_3}$			AN_7
37		$P10_6$	$\overline{KI_2}$			AN_6
38		$P10_5$	$\overline{KI_1}$			AN_5
39		$P10_4$	$\overline{KI_0}$			AN_4
40		$P10_3$				AN_3
41		$P10_2$				AN_2
42		$P10_1$				AN_1

1.6 Pin Description

Table 1.13 Pin Description (48-Pin and 42-Pin Packages)

Classification	Pin Name	I/O Type	Description
Power Supply	V_{CC}, V_{SS}	I	Apply 0V to the Vss pin. Apply following voltage to the Vcc pin. 2.7 to 5.5 V (M16C/26A, M16C/26B), 3.0 to 5.5 V (M16C/26T T-ver.), 4.2 to 5.5 V (M16C/26T V-ver.)
Analog Power Supply	AV_{CC} AV_{SS}	I	Supplies power to the A/D converter. Connect the AV_{CC} pin to V_{CC} and the AV_{SS} pin to V_{SS}
Reset Input	$\overline{RESET}$	I	The MCU is in a reset state when "L" is applied to the $\overline{RESET}$ pin
CNVSS	CNV_{SS}	I	Connect the CNV_{SS} pin to V_{SS}
Main Clock Input	X_{IN}	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between X_{IN} and X_{OUT}. To apply external clock, apply it to X_{IN} and leave X_{OUT} open. If X_{IN} is not used (for external oscillator or external clock), connect X_{IN} pin to V_{CC} and leave X_{OUT} open
Main Clock Output	X_{OUT}	O	
Sub Clock Input	X_{CIN}	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between X_{CIN} and X_{COUT}
Sub Clock Output	X_{COUT}	O	
Clock Output	CLK_{OUT}	O	Outputs the clock having the same frequency as f1, f_8, f_{32}, or f_C
$\overline{INT}$ Interrupt Input	$\overline{INT0}$ to $\overline{INT5}$	I	Input pins for the $\overline{INT}$ interrupt. $\overline{INT2}$ can be used for Timer A Z-phase function
$\overline{NMI}$ Interrupt Input	$\overline{NMI}$	I	$\overline{NMI}$ interrupt input pin. $\overline{NMI}$ cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{NMI}$ after setting it's direction register to "0" when the three-phase motor control is enabled
Key Input Interrupt	$\overline{KI0}$ to $\overline{KI3}$	I	Input pins for the key input interrupt
Timer A	$TA0_{OUT}$ to $TA4_{OUT}$	I/O	I/O pins for the timer A0 to A4
	$TA0_{IN}$ to $TA4_{IN}$	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	$TB0_{IN}$ to $TB1_{IN}$	I	Timer B0 to B1 input pins
Three-Phase Motor Control Timer Output	U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, $\overline{SD}$	I/O	I/O pins for the three-phase motor control timer
Serial I/O	$\overline{CTS1}$ to $\overline{CTS2}$	I	Input pins to control data transmission
	$\overline{RTS1}$ to $\overline{RTS2}$	O	Output pins to control data reception
	CLK1 to CLK2	I/O	Inputs and outputs the transfer clock
	RxD1 to RxD2	I	Inputs serial data
	TxD1 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
Reference Voltage Input	V_{REF}	I	Applies reference voltage to the A/D converter
A/D Converter	AN_0 to AN_7 $AN3_0$ to $AN3_1$	I	Analog input pins for the A/D converter
	$\overline{ADTRG}$	I	Input pin for an external A/D trigger
I/O Ports	$P1_5$ to $P1_7$	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 3-bit units
	$P6_4$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P10_0$ to $P10_7$ $P9_0$ to $P9_1$	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units

I : Input O : Output I/O : Input and output

Table 1.13 Pin Description (48-pin packages only) (Continued)

Classification	Pin Name	I/O Type	Description
Serial I/O	$\overline{CTS0}$	I	Inputs pin to control data transmission
	$\overline{RTS0}$	O	Output pin to control data reception
	CLK0	I/O	Inputs and outputs the transfer clock
	RxD0	I	Inputs serial data
	TxD0	O	Outputs serial data
Timer B	TB2IN	I	Timer B2 input pin
A/D Converter	$AN2_4$ $AN3_2$	I	Analog input pins for the A/D converter
I/O Ports	$P6_0$ to $P6_3$ $P9_2$ to $P9_3$	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The register bank is comprised of seven registers (R0, R1, R2, R3, A0, A1 and FB) out of 13 registers. There are two sets of register bank.

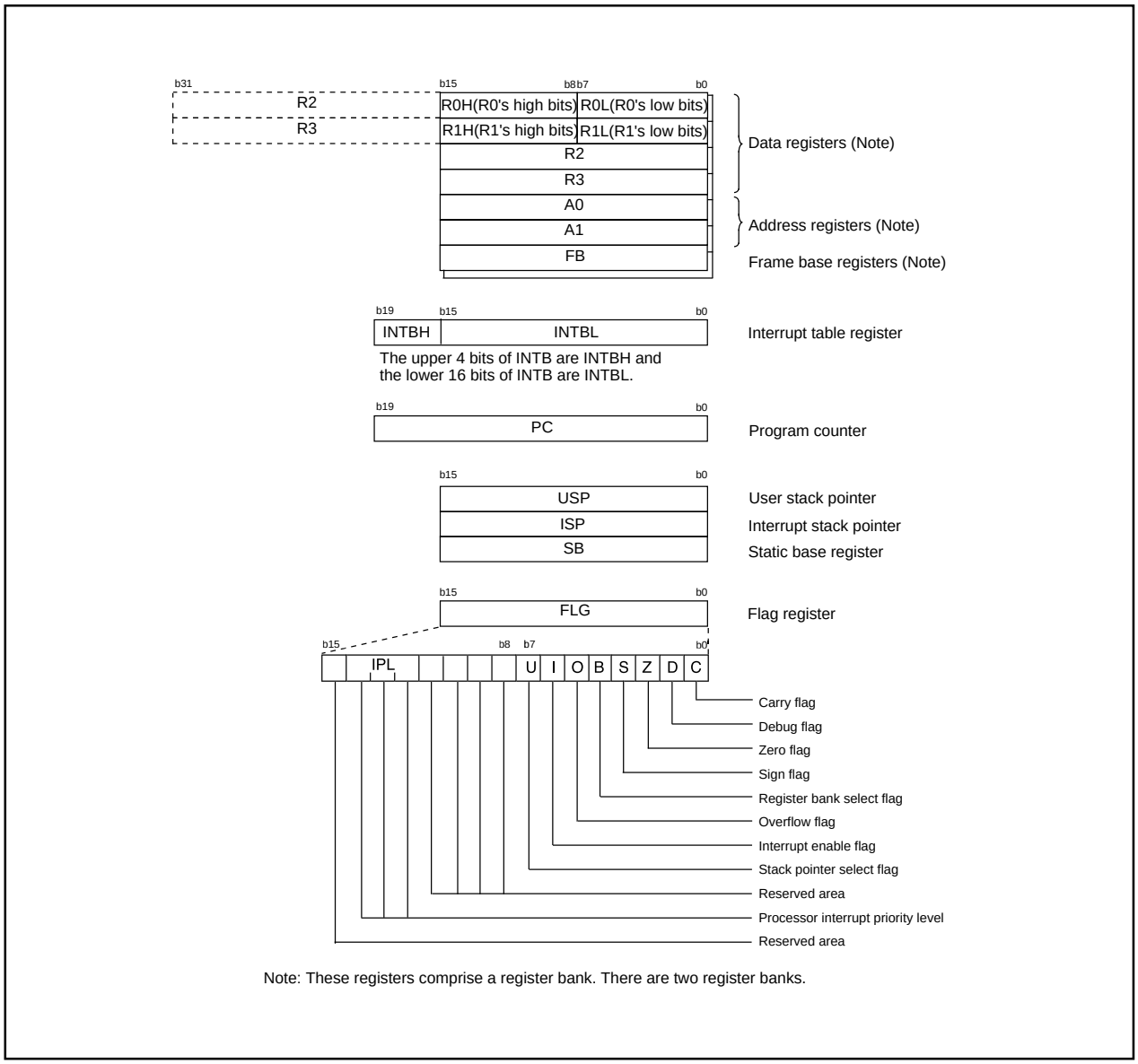


Figure 2.1. CPU Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1.

The I flag is cleared to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is undefined.

3. Memory

Figure 3.1 is a memory map of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T). The M16C/26A Group provides 1-Mbyte address space addresses 00000_{16} to $FFFFF_{16}$.

The internal ROM is allocated lower address, beginning with address $FFFFF_{16}$. For example, a 64-Kbyte internal ROM area is allocated in addresses $F0000_{16}$ to $FFFFF_{16}$. The flash memory version has two sets of 2-Kbyte internal ROM area, block A and block B, for data space. These blocks are allocated addresses $F000_{16}$ to $FFFF_{16}$.

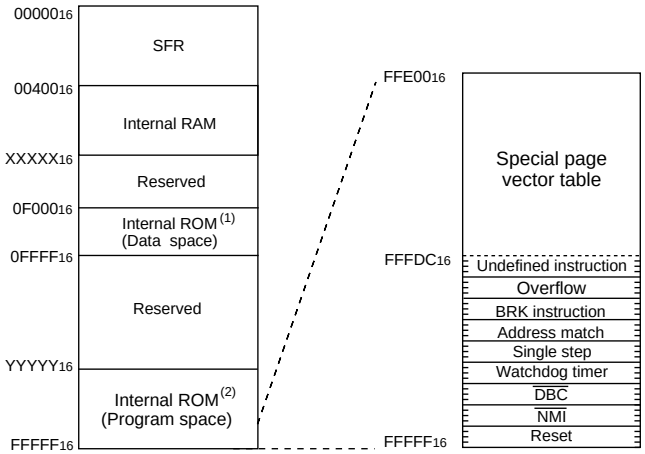
The fixed interrupt vectors are allocated addresses $FFFDC_{16}$ to $FFFFF_{16}$ and they store the start address of each interrupt routine.

The internal RAM is allocated higher addresses, beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM area is allocated in addresses 00400_{16} to $007FF_{16}$. The internal RAM is used for temporarily storing data. The area is also used as stacks when subroutines are called or interrupt requests are acknowledged.

The SFR is allocated addresses 00000_{16} to $003FF_{16}$. The peripheral function control registers are allocated here. All blank spaces within SFR location are reserved and cannot be accessed by users.

The special page vectors are allocated addresses $FFE00_{16}$ to $FFFDB_{16}$. They are used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M16C/60 and M16C/20 Series Software Manual** for details.

Internal RAM		Internal ROM	
Size	Address XXXXX_{16}	Size	Address $YYYYY_{16}$
1K bytes	$007FF_{16}$	24K bytes	$FA000_{16}$
2K bytes	$00BFF_{16}$	48K bytes	$F4000_{16}$
		64K bytes	$F0000_{16}$



NOTE:
1. Block A (2 Kbytes) and block B (2 Kbytes).
2. Do not write to the internal ROM in Mask ROM version.

Figure 3.1 Memory Map

4. Special Function Register (SFR)

Table 4.1 SFR Information(1)(1)

Address	Register	Symbol	After reset
0000_{16}			
0001_{16}			
0002_{16}			
0003_{16}			
0004_{16}	Processor mode register 0	PM0	00_{16}
0005_{16}	Processor mode register 1	PM1	00001000_2
0006_{16}	System clock control register 0	CM0	01001000_2(M16C/26A) 01101000_2(M16C/26T)
0007_{16}	System clock control register 1	CM1	00100000_2
0008_{16}			
0009_{16}	Address match interrupt enable register	AIER	$XXXXXX00_2$
$000A_{16}$	Protect register	PRCR	$XX000000_2$
$000B_{16}$			
$000C_{16}$	Oscillation stop detection register(2)	CM2	$0X000000_2$
$000D_{16}$			
$000E_{16}$	Watchdog timer start register	WDTS	XX_{16}
$000F_{16}$	Watchdog timer control register	WDC	$00XXXXXX_2$ (3)
0010_{16} 0011_{16} 0012_{16}	Address match interrupt register 0	RMAD0	00_{16} 00_{16} $X0_{16}$
0013_{16}			
0014_{16} 0015_{16} 0016_{16}	Address match interrupt register 1	RMAD1	00_{16} 00_{16} $X0_{16}$
0017_{16}			
0018_{16}			
0019_{16}	Voltage detection register 1 (4, 5)	VCR1	00001000_2
$001A_{16}$	Voltage detection register 2 (4, 5)	VCR2	00_{16}
$001B_{16}$			
$001C_{16}$	PLL control register 0	PLC0	$0001X010_2$
$001D_{16}$			
$001E_{16}$	Processor mode register 2	PM2	$XXX00000_2$
$001F_{16}$	Low voltage detection interrupt register(5)	D4INT	00_{16}
0020_{16} 0021_{16} 0022_{16}	DMA0 source pointer	SAR0	XX_{16} XX_{16} XX_{16}
0023_{16}			
0024_{16} 0025_{16} 0026_{16}	DMA0 destination pointer	DAR0	XX_{16} XX_{16} XX_{16}
0027_{16}			
0028_{16} 0029_{16}	DMA0 transfer counter	TCR0	XX_{16} XX_{16}
$002A_{16}$			
$002B_{16}$			
$002C_{16}$	DMA0 control register	DM0CON	$00000X00_2$
$002D_{16}$			
$002E_{16}$			
$002F_{16}$			
0030_{16} 0031_{16} 0032_{16} 0033_{16}	DMA1 source pointer	SAR1	XX_{16} XX_{16} XX_{16}
0034_{16} 0035_{16} 0036_{16}	DMA1 destination pointer	DAR1	XX_{16} XX_{16} XX_{16}
0037_{16}			
0038_{16} 0039_{16}	DMA1 transfer counter	TCR1	XX_{16} XX_{16}
$003A_{16}$			
$003B_{16}$			
$003C_{16}$	DMA1 control register	DM1CON	$00000X00_2$
$003D_{16}$			
$003E_{16}$			
$003F_{16}$			

NOTES:
1. The blank spaces are reserved. No access is allowed.
2. Bits CM27, CM21, and CM20 do not change at oscillation stop detection reset.
3. The WDC5 bit is 0 (cold start) immediately after power-on. It can only be set to 1 by program. The WDC5 bit cannot be used in M16C/26T.
4. The VCR1 and VCR2 registers do not change at software reset, watchdog timer reset, and oscillation stop detection reset.
5. Registers VCR1, VCR2, and D4INT cannot be used in M16C/26T.

X : Undefined

Table 4.2 SFR Information(2)(1)

Address	Register	Symbol	After reset
0040_{16}			
0041_{16}			
0042_{16}			
0043_{16}			
0044_{16}	INT3 interrupt control register	INT3IC	$XX00X000_2$
0045_{16}			
0046_{16}			
0047_{16}			
0048_{16}	INT5 interrupt control register	INT5IC	$XX00X000_2$
0049_{16}	INT4 interrupt control register	INT4IC	$XX00X000_2$
$004A_{16}$	UART2 Bus collision detection interrupt control register	BCNIC	$XXXXX000_2$
$004B_{16}$	DMA0 interrupt control register	DM0IC	$XXXXX000_2$
$004C_{16}$	DMA1 interrupt control register	DM1IC	$XXXXX000_2$
$004D_{16}$	Key input interrupt control register	KUPIC	$XXXXX000_2$
$004E_{16}$	A/D conversion interrupt control register	ADIC	$XXXXX000_2$
$004F_{16}$	UART2 transmit interrupt control register	S2TIC	$XXXXX000_2$
0050_{16}	UART2 receive interrupt control register	S2RIC	$XXXXX000_2$
0051_{16}	UART0 transmit interrupt control register	S0TIC	$XXXXX000_2$
0052_{16}	UART0 receive interrupt control register	S0RIC	$XXXXX000_2$
0053_{16}	UART1 transmit interrupt control register	S1TIC	$XXXXX000_2$
0054_{16}	UART1 receive interrupt control register	S1RIC	$XXXXX000_2$
0055_{16}	TimerA0 interrupt control register	TA0IC	$XXXXX000_2$
0056_{16}	TimerA1 interrupt control register	TA1IC	$XXXXX000_2$
0057_{16}	TimerA2 interrupt control register	TA2IC	$XXXXX000_2$
0058_{16}	TimerA3 interrupt control register	TA3IC	$XXXXX000_2$
0059_{16}	TimerA4 interrupt control register	TA4IC	$XXXXX000_2$
$005A_{16}$	TimerB0 interrupt control register	TB0IC	$XXXXX000_2$
$005B_{16}$	TimerB1 interrupt control register	TB1IC	$XXXXX000_2$
$005C_{16}$	TimerB2 interrupt control register	TB2IC	$XXXXX000_2$
$005D_{16}$	INT0 interrupt control register	INT0IC	$XX00X000_2$
$005E_{16}$	INT1 interrupt control register	INT1IC	$XX00X000_2$
$005F_{16}$	INT2 interrupt control register	INT2IC	$XX00X000_2$
0060_{16}			
0061_{16}			
0062_{16}			
0063_{16}			
0064_{16}			
0065_{16}			
0066_{16}			
0067_{16}			
0068_{16}			
0069_{16}			
$006A_{16}$			
$006B_{16}$			
$006C_{16}$			
$006D_{16}$			
$006E_{16}$			
$006F_{16}$			
0070_{16}			
0071_{16}			
0072_{16}			
0073_{16}			
0074_{16}			
0075_{16}			
0076_{16}			
0077_{16}			
0078_{16}			
0079_{16}			
$007A_{16}$			
$007B_{16}$			
$007C_{16}$			
$007D_{16}$			
$007E_{16}$			
$007F_{16}$			

NOTE:
1. Blank spaces are reserved. No access is allowed.

X: Undefined

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After reset
0080_{16}			
0081_{16}			
0082_{16}			
0083_{16}			
0084_{16}			
0085_{16}			
0086_{16}			
≈			≈
$01B0_{16}$			
$01B1_{16}$			
$01B2_{16}$			
$01B3_{16}$	Flash memory control register 4 (Note 2)	FMR4	01000000_2
$01B4_{16}$			
$01B5_{16}$	Flash memory control register 1 (Note 2)	FMR1	$000XXX0X_2$
$01B6_{16}$			
$01B7_{16}$	Flash memory control register 0 (Note 2)	FMR0	01_{16}
$01B8_{16}$			
$01B9_{16}$			
$01BA_{16}$			
$01BB_{16}$			
$01BC_{16}$			
$01BD_{16}$			
$01BE_{16}$			
$01BF_{16}$			
≈			≈
0250_{16}			
0251_{16}			
0252_{16}			
0253_{16}			
0254_{16}			
0255_{16}			
0256_{16}			
0257_{16}			
0258_{16}			
0259_{16}			
$025A_{16}$	Three phase protect control register	TPRC	00_{16}
$025B_{16}$			
$025C_{16}$	On-chip oscillator control register	ROCR	00000101_2
$025D_{16}$	Pin assignment control register	PACR	00_{16}
$025E_{16}$	Peripheral clock select register	PCLKR	00000011_2
$025F_{16}$			
≈			≈
0330_{16}			
0331_{16}			
0332_{16}			
0333_{16}			
0334_{16}			
0335_{16}			
0336_{16}			
0337_{16}			
0338_{16}			
0339_{16}			
$033A_{16}$			
$033B_{16}$			
$033C_{16}$			
$033D_{16}$			
$033E_{16}$	NMI digital debounce register	NDDR	FF_{16}
$033F_{16}$	Port1_7 digital debounce register	P17DDR	FF_{16}

NOTES:
1. Blank spaces are reserved. No access is allowed.
2. This register is included in the flash memory version.

X: Undefined

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After reset
0340_{16}			
0341_{16}			
0342_{16} 0343_{16}	Timer A1-1 register	TA11	XX_{16} XX_{16}
0344_{16} 0345_{16}	Timer A2-1 register	TA21	XX_{16} XX_{16}
0346_{16} 0347_{16}	Timer A4-1 register	TA41	XX_{16} XX_{16}
0348_{16}	Three phase PWM control register 0	INVC0	00_{16}
0349_{16}	Three phase PWM control register 1	INVC1	00_{16}
$034A_{16}$	Three phase output buffer register 0	IDB0	$3F_{16}$
$034B_{16}$	Three phase output buffer register 1	IDB1	$3F_{16}$
$034C_{16}$	Dead time timer	DTT	XX_{16}
$034D_{16}$	Timer B2 Interrupt occurrence frequency set counter	ICTB2	XX_{16}
$034E_{16}$	Position-data-retain function control register	PDRF	$XXXX0000_2$
$034F_{16}$			
0350_{16}			
0351_{16}			
0352_{16}			
0353_{16}			
0354_{16}			
0355_{16}			
0356_{16}			
0357_{16}			
0358_{16}	Port function control register	PFCR	00111111_2
0359_{16}			
$035A_{16}$			
$035B_{16}$			
$035C_{16}$			
$035D_{16}$			
$035E_{16}$	Interrupt request cause select register 2	IFSR2A	$XXXXXXX0_2$
$035F_{16}$	Interrupt request cause select register	IFSR	00_{16}
0360_{16}			
0361_{16}			
0362_{16}			
0363_{16}			
0364_{16}			
0365_{16}			
0366_{16}			
0367_{16}			
0368_{16}			
0369_{16}			
$036A_{16}$			
$036B_{16}$			
$036C_{16}$			
$036D_{16}$			
$036E_{16}$			
$036F_{16}$			
0370_{16}			
0371_{16}			
0372_{16}			
0373_{16}			
0374_{16}	UART2 special mode register 4	U2SMR4	00_{16}
0375_{16}	UART2 special mode register 3	U2SMR3	$000X0X0X_2$
0376_{16}	UART2 special mode register 2	U2SMR2	$X0000000_2$
0377_{16}	UART2 special mode register	U2SMR	$X0000000_2$
0378_{16}	UART2 transmit/receive mode register	U2MR	00_{16}
0379_{16}	UART2 bit rate register	U2BRG	XX_{16}
$037A_{16}$ $037B_{16}$	UART2 transmit buffer register	U2TB	XXXXXXXX_2 XXXXXXXX_2
$037C_{16}$	UART2 transmit/receive control register 0	U2C0	00001000_2
$037D_{16}$	UART2 transmit/receive control register 1	U2C1	00000010_2
$037E_{16}$ $037F_{16}$	UART2 receive buffer register	U2RB	XXXXXXXX_2 XXXXXXXX_2

NOTE:
1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.5 SFR Information(5)(1)

Address	Register	Symbol	After reset
0380_{16}	Count start flag	TABSR	00_{16}
0381_{16}	Clock prescaler reset flag	CPSRF	$0XXXXXXX_2$
0382_{16}	One-shot start flag	ONSF	00_{16}
0383_{16}	Trigger select register	TRGSR	00_{16}
0384_{16}	Up-dowm flag	UDF	00_{16}
0385_{16}			
0386_{16} 0387_{16}	Timer A0 register	TA0	XX_{16} XX_{16}
0388_{16} 0389_{16}	Timer A1 register	TA1	XX_{16} XX_{16}
$038A_{16}$ $038B_{16}$	Timer A2 register	TA2	XX_{16} XX_{16}
$038C_{16}$ $038D_{16}$	Timer A3 register	TA3	XX_{16} XX_{16}
$038E_{16}$ $038F_{16}$	Timer A4 register	TA4	XX_{16} XX_{16}
0390_{16} 0391_{16}	Timer B0 register	TB0	XX_{16} XX_{16}
0392_{16} 0393_{16}	Timer B1 register	TB1	XX_{16} XX_{16}
0394_{16} 0395_{16}	Timer B2 register	TB2	XX_{16} XX_{16}
0396_{16}	Timer A0 mode register	TA0MR	00_{16}
0397_{16}	Timer A1 mode register	TA1MR	00_{16}
0398_{16}	Timer A2 mode register	TA2MR	00_{16}
0399_{16}	Timer A3 mode register	TA3MR	00_{16}
$039A_{16}$	Timer A4 mode register	TA4MR	00_{16}
$039B_{16}$	Timer B0 mode register	TB0MR	$00XX0000_2$
$039C_{16}$	Timer B1 mode register	TB1MR	$00XX0000_2$
$039D_{16}$	Timer B2 mode register	TB2MR	$00XX0000_2$
$039E_{16}$	Timer B2 special mode register	TB2SC	$X0000000_2$
$039F_{16}$			
$03A0_{16}$	UART0 transmit/receive mode register	U0MR	00_{16}
$03A1_{16}$	UART0 bit rate register	U0BRG	XX_{16}
$03A2_{16}$ $03A3_{16}$	UART0 transmit buffer register	U0TB	XXXXXXXX_2 XXXXXXXX_2
$03A4_{16}$	UART0 transmit/receive control register 0	U0C0	00001000_2
$03A5_{16}$	UART0 transmit/receive control register 1	U0C1	00000010_2
$03A6_{16}$ $03A7_{16}$	UART0 receive buffer register	U0RB	XXXXXXXX_2 XXXXXXXX_2
$03A8_{16}$	UART1 transmit/receive mode register	U1MR	00_{16}
$03A9_{16}$	UART1 bit rate register	U1BRG	XX_{16}
$03AA_{16}$ $03AB_{16}$	UART1 transmit buffer register	U1TB	XXXXXXXX_2 XXXXXXXX_2
$03AC_{16}$	UART1 transmit/receive control register 0	U1C0	00001000_2
$03AD_{16}$	UART1 transmit/receive control register 1	U1C1	00000010_2
$03AE_{16}$ $03AF_{16}$	UART1 receive buffer register	U1RB	XXXXXXXX_2 XXXXXXXX_2
$03B0_{16}$	UART transmit/receive control register 2	UCON	$X0000000_2$
$03B1_{16}$			
$03B2_{16}$			
$03B3_{16}$			
$03B4_{16}$ $03B5_{16}$	CRC snoop address register	CRCSAR	XX_{16} $00XXXXXX_2$
$03B6_{16}$	CRC mode register	CRCMR	$0XXXXXX0_2$
$03B7_{16}$			
$03B8_{16}$	DMA0 request cause select register	DM0SL	00_{16}
$03B9_{16}$			
$03BA_{16}$	DMA1 request cause select register	DM1SL	00_{16}
$03BB_{16}$			
$03BC_{16}$ $03BD_{16}$	CRC data register	CRCD	XX_{16} XX_{16}
$03BE_{16}$	CRC input register	CRCIN	XX_{16}
$03BF_{16}$			

NOTE:
1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.6 SFR Information(6)(1)

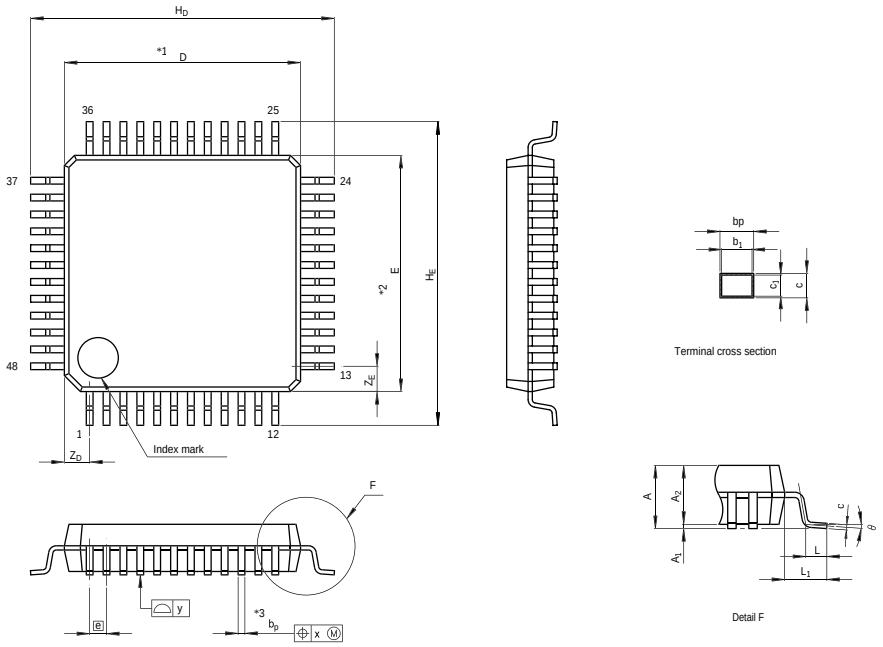
Address	Register	Symbol	After Reset
$03C0_{16}$ $03C1_{16}$	A/D register 0	AD0	XXXXXXXX_2 XXXXXXXX_2
$03C2_{16}$ $03C3_{16}$	A/D register 1	AD1	XXXXXXXX2 XXXXXXXX_2
$03C4_{16}$ $03C5_{16}$	A/D register 2	AD2	XXXXXXXX_2 XXXXXXXX_2
$03C6_{16}$ $03C7_{16}$	A/D register 3	AD3	XXXXXXXX_2 XXXXXXXX_2
$03C8_{16}$ $03C9_{16}$	A/D register 4	AD4	XXXXXXXX_2 XXXXXXXX_2
$03CA_{16}$ $03CB_{16}$	A/D register 5	AD5	XXXXXXXX_2 XXXXXXXX_2
$03CC_{16}$ $03CD_{16}$	A/D register 6	AD6	XXXXXXXX_2 XXXXXXXX_2
$03CE_{16}$ $03CF_{16}$	A/D register 7	AD7	XXXXXXXX_2 XXXXXXXX_2
$03D0_{16}$			
$03D1_{16}$			
$03D2_{16}$	A/D trigger control register	ADTRGCON	00_{16}
$03D3_{16}$	A/D status register 0	ADSTAT0	$00000X00_2$
$03D4_{16}$	A/D control register 2	ADCON2	00_{16}
$03D5_{16}$			
$03D6_{16}$	A/D control register 0	ADCON0	$00000XXX_2$
$03D7_{16}$	A/D control register 1	ADCON1	00_{16}
$03D8_{16}$			
$03D9_{16}$			
$03DA_{16}$			
$03DB_{16}$			
$03DC_{16}$			
$03DD_{16}$			
$03DE_{16}$			
$03DF_{16}$			
$03E0_{16}$			
$03E1_{16}$	Port P1 register	P1	XX_{16}
$03E2_{16}$			
$03E3_{16}$	Port P1 direction register	PD1	00_{16}
$03E4_{16}$			
$03E5_{16}$			
$03E6_{16}$			
$03E7_{16}$			
$03E8_{16}$			
$03E9_{16}$			
$03EA_{16}$			
$03EB_{16}$			
$03EC_{16}$	Port P6 register	P6	XX_{16}
$03ED_{16}$	Port P7 register	P7	XX_{16}
$03EE_{16}$	Port P6 direction register	PD6	00_{16}
$03EF_{16}$	Port P7 direction register	PD7	00_{16}
$03F0_{16}$	Port P8 register	P8	XX_{16}
$03F1_{16}$	Port P9 register	P9	XXXXXXXX_2
$03F2_{16}$	Port P8 direction register	PD8	00_{16}
$03F3_{16}$	Port P9 direction register	PD9	$XXXX0000_2$
$03F4_{16}$	Port P10 register	P10	XX_{16}
$03F5_{16}$			
$03F6_{16}$	Port P10 direction register	PD10	00_{16}
$03F7_{16}$			
$03F8_{16}$			
$03F9_{16}$			
$03FA_{16}$			
$03FB_{16}$			
$03FC_{16}$	Pull-up control register 0	PUR0	00_{16}
$03FD_{16}$	Pull-up control register 1	PUR1	00_{16}
$03FE_{16}$	Pull-up control register 2	PUR2	00_{16}
$03FF_{16}$	Port control register	PCR	00_{16}

NOTE:
1. Blank spaces are reserved. No access is allowed.

X: Undefined

Package

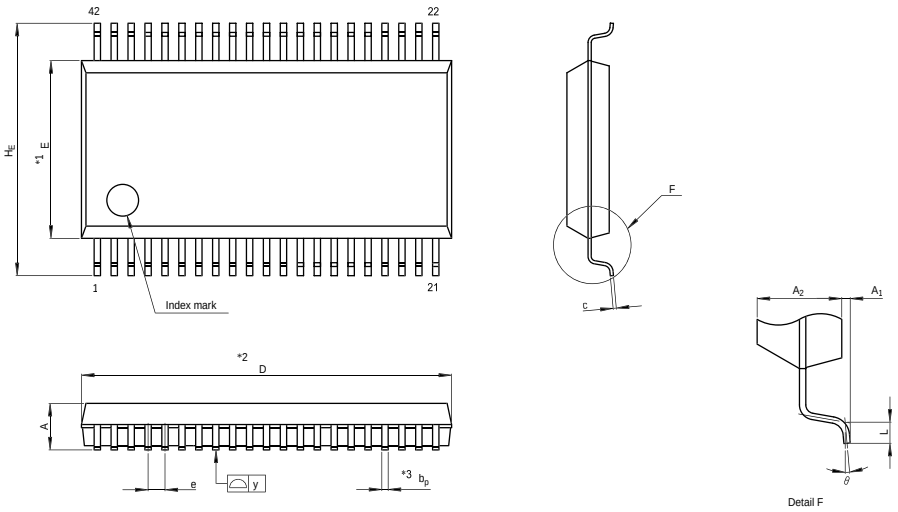
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0º	—	8º
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SSOP42-8.4x17.5-0.80	PRSP0042GA-B	42P2R-E	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	17.3	17.5	17.7
E	8.2	8.4	8.6
A_2	—	2.0	—
A	—	—	2.4
A_1	0.05	—	—
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0º	—	10º
H_E	11.63	11.93	12.23
e	0.65	0.8	0.95
y	—	—	0.15
L	0.3	0.5	0.7

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