

IA88C00

Microcontroller

Data Sheet

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Please Note

Included under Ordering Information on page 68 are enhanced RoHS-compliant versions of the IA88C00. However, standard packaged or non RoHS-compliant versions of the IA88C00 microcontroller are still available.

Features

- Fully Form, Fit and Function Compatible with the Super8 (Z88C00)
- Available in 48-, and 68-pin packages
- Fully Compatible with the Super8 Instruction Set
- Rich Program Register Set
- 128 Kbytes external program address space
- Built-in Direct Memory Access (DMA)
- Two Programmable 16-bit counter/timers with 8-bit prescalers
- Up to 32 General Purpose I/O Lines including special handshake functionality
- Robust Interrupt structure
- Watch-Dog Timer

General Description

The IA88COO is a form, fit and function replacement for the original Zilog® Z88C00 microcontroller. Innovasic Semiconductor produces replacement ICs using its MILES™, or Managed IC Lifetime Extension System, cloning technology. This technology produces replacement ICs far more complex than "emulation" while ensuring they are compatible with the original IC. MILES™ captures the design of a clone so it can be produced even as silicon technology advances. MILES™ also verifies the clone against the original IC so that even the "undocumented features" are duplicated.

This Data Sheet documents all necessary engineering information about the IA88COO including functional and I/O descriptions, electrical characteristics, and applicable timing.

The function block diagram of the IA88C00 is shown in Figure 1. The device is available in a 48-pin DIP (Figure 2) and a 68-pin PLCC package (Figure 3). The pin functions of the IA88COO are outlined in Figure 6. Pin Functions.

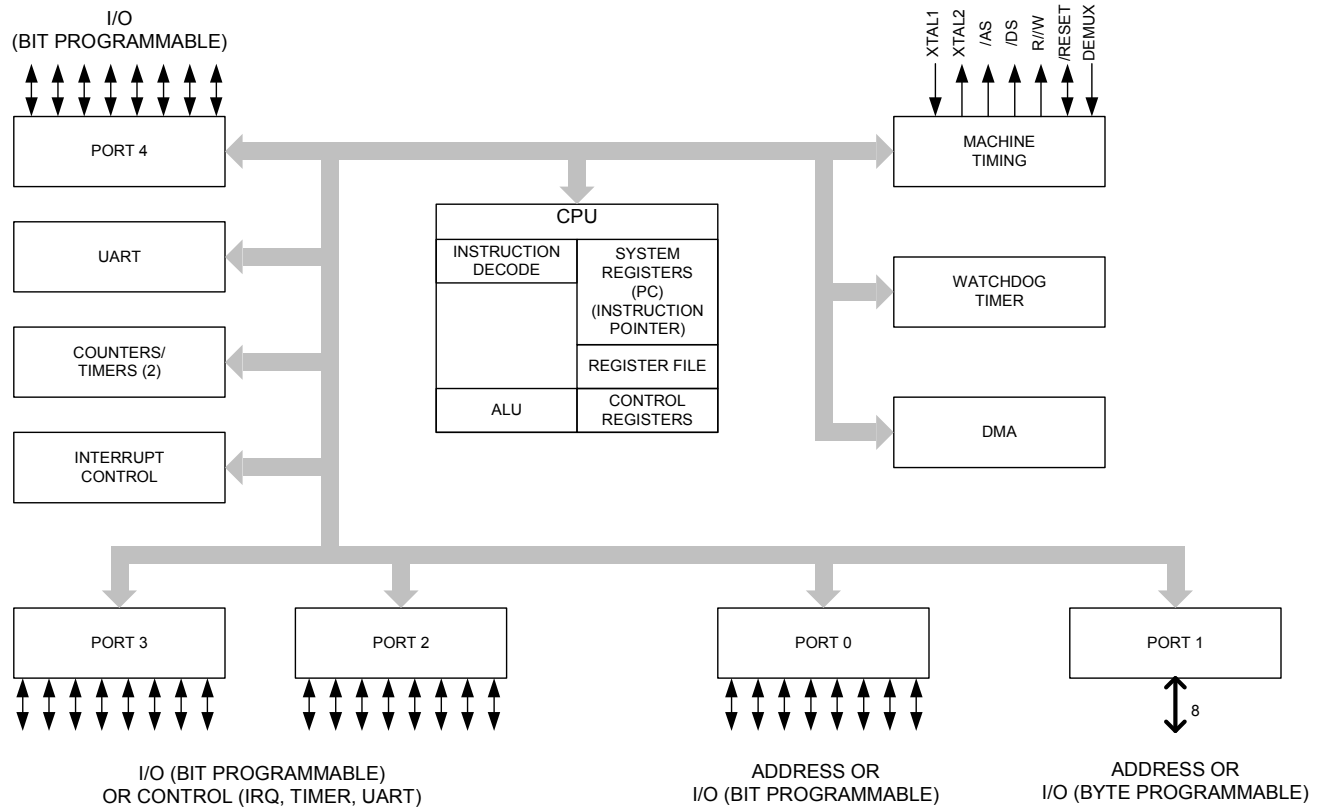


Figure 1. Functional Block Diagram

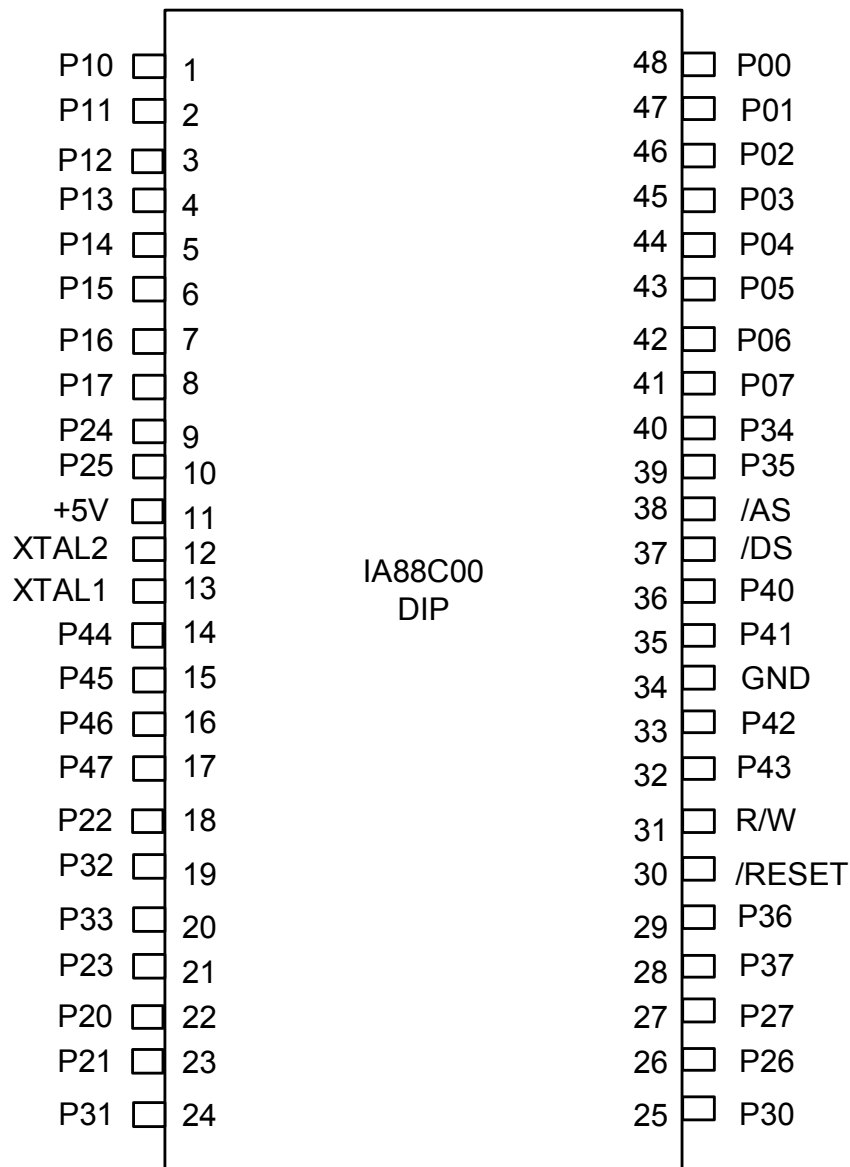


Figure 2. 48-Lead DIP Package

Figure 3. 48-Lead DIP Pin Assignments

| Pin # | Symbol | Function | Direction |
|-------|--------|------------------------------|--------------|
| 1-8 | P10-17 | Port 1, pins 0,1,3,4,5,6,7 | In/Output |
| 9-10 | P24-25 | Port 2, pins 4,5 | In/Output |
| 11 | Vcc | Power Supply | Input |
| 12 | XTAL2 | Crystal Oscillator | Output |
| 13 | XTAL1 | Crystal Oscillator | Output |
| 14-17 | P44-47 | Port 4, pins 4,5,6,7 | Input/Output |
| 18 | P22 | Port 2, pin 2 | Input/Output |
| 19-20 | P32-21 | Port 2, pins 2,3 | Input/Output |
| 21-23 | P23-21 | Port 2, pins 3,0,1 | Input/Output |
| 24-25 | P31-30 | Port 3, pins 1,0 | Input/Output |
| 26-27 | P26-27 | Port 2, pins 6,7 | Input/Output |
| 28-29 | P37-36 | Port 3, pins 7,6 | In/Output |
| 30 | /RESET | RESET | Input |
| 31 | R/W | READ/WRITE | Output |
| 32-33 | P43-42 | Port 4, pins 3,2 | In/Output |
| 34 | GND | Ground | Input |
| 35-36 | P41-40 | Port 4, pins 1,0 | In/Output |
| 37 | /DS | Data Strobe | Output |
| 38 | /AS | Address Strobe | Output |
| 39-40 | P35-34 | Port 3, pins 5,4 | In/Output |
| 41-48 | P07-00 | Port 0, pins 7,6,5,4,3,2,1,0 | In/Output |

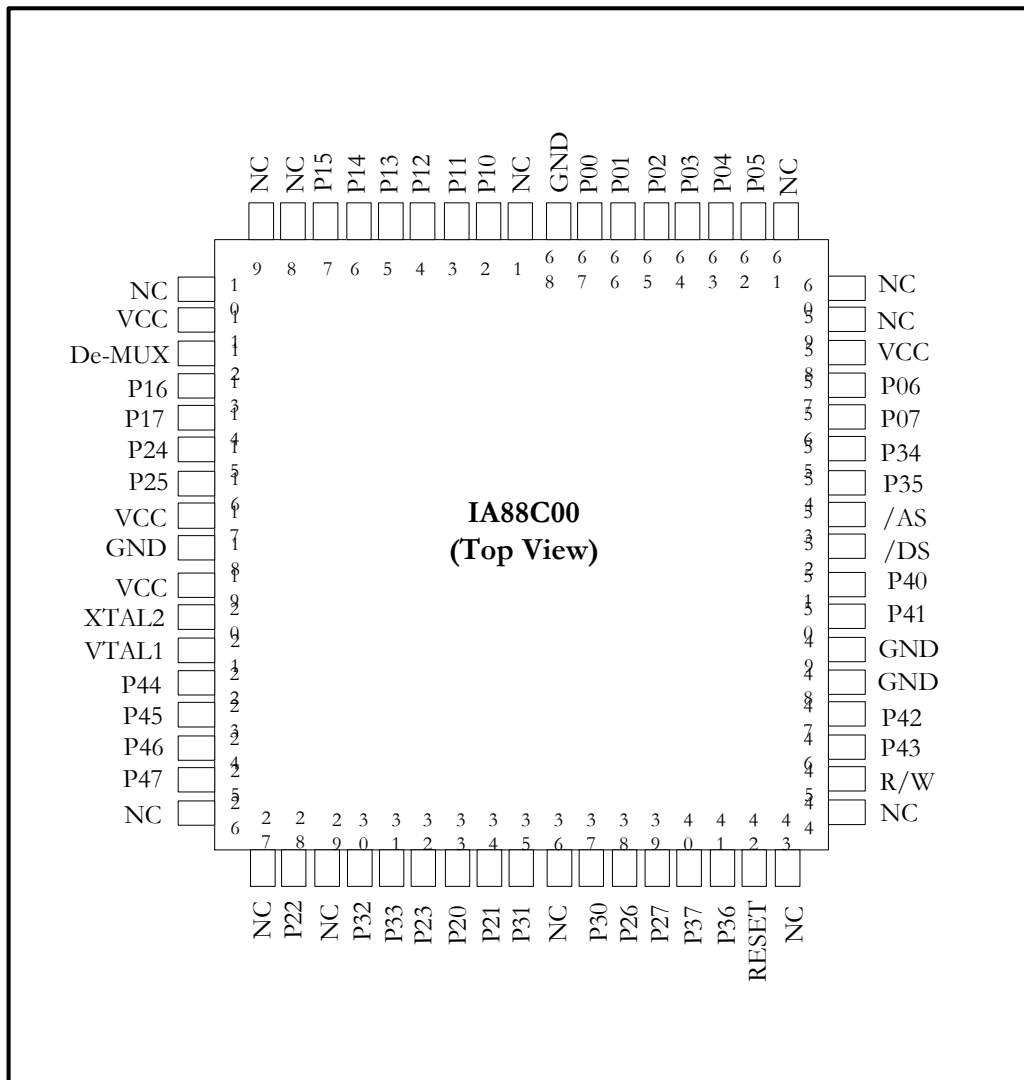


Figure 4. 68-Lead PLCC Package

Figure 5. 68-Lead PLCC-Pin Assignments

| Pin # | Symbol | Function | Direction |
|-------|--------|--------------------------|-----------|
| 1 | NC | Note Connected | |
| 2-7 | P10-15 | Port 1, pins 0,1,2,3,4,5 | In/Output |
| 8-10 | NC | Not Connected | |
| 11 | Vcc | Power Supply | Input |
| 12 | De-Mux | De-multiplex Pin | Input |
| 13-14 | P16-17 | Port 1, pins 6,7 | In/Output |
| 15-16 | P24-25 | Port 2, pins 4,5 | In/Output |
| 17 | Vcc | Power Supply | Input |
| 18 | GND | Ground | Input |
| 19 | Vcc | Power Supply | Input |
| 20 | XTAL2 | Crystal Oscillator | In/Output |
| 21 | XTAL1 | Crystal Oscillator | In/Output |
| 22-25 | P44-47 | Port 4, points 4,5,6,7 | In/Output |
| 26-27 | NC | Not Connected | |
| 28 | P22 | Port 2, pin 2 | In/Output |
| 29 | NC | Not Connected | |
| 30-31 | P32-33 | Port 3, pins 2,3 | In/Output |
| 32-34 | P23-21 | Port 2, pins 3,0,1 | In/Output |
| 35 | P31 | Port 3, pin 1 | In/Output |
| 36 | NC | Not Connected | |
| 37 | P30 | Port 3, pin 0 | In/Output |
| 38-39 | P26-27 | Port 2, pins 6,7 | In/Output |
| 40-41 | P37-36 | Port 3, pins 7,6 | In/Output |
| 42 | /RESET | RESET | Input |
| 43-44 | NC | Not Connected | |
| 45 | R/W | READ/WRITE | Output |
| 46-47 | P43-42 | Port 4, pins 3,2 | In/Output |
| 48-49 | GND | Ground | Input |
| 50-51 | P41-40 | Port 4, pins 1,0 | In/Output |
| 52 | /DS | Data Strobe | Output |
| 53 | /AS | Address Strobe | Output |
| 54-55 | P43-42 | Port 3, pins 5,4,3,2 | In/Output |
| 56-57 | P07-06 | Port 0, pins 7,6 | In/Output |
| 58 | Vcc | Power Supply | Input |
| 59-61 | NC | Not Connected | |
| 62-65 | P05-02 | Port 0, pins 5,4,3,2 | In/Output |
| 66 | GND | Ground | Input |

| | | | |
|----|-----|---------------|--------------|
| 67 | NC | Not Connected | Input/Output |
| 68 | GND | Ground | Input |

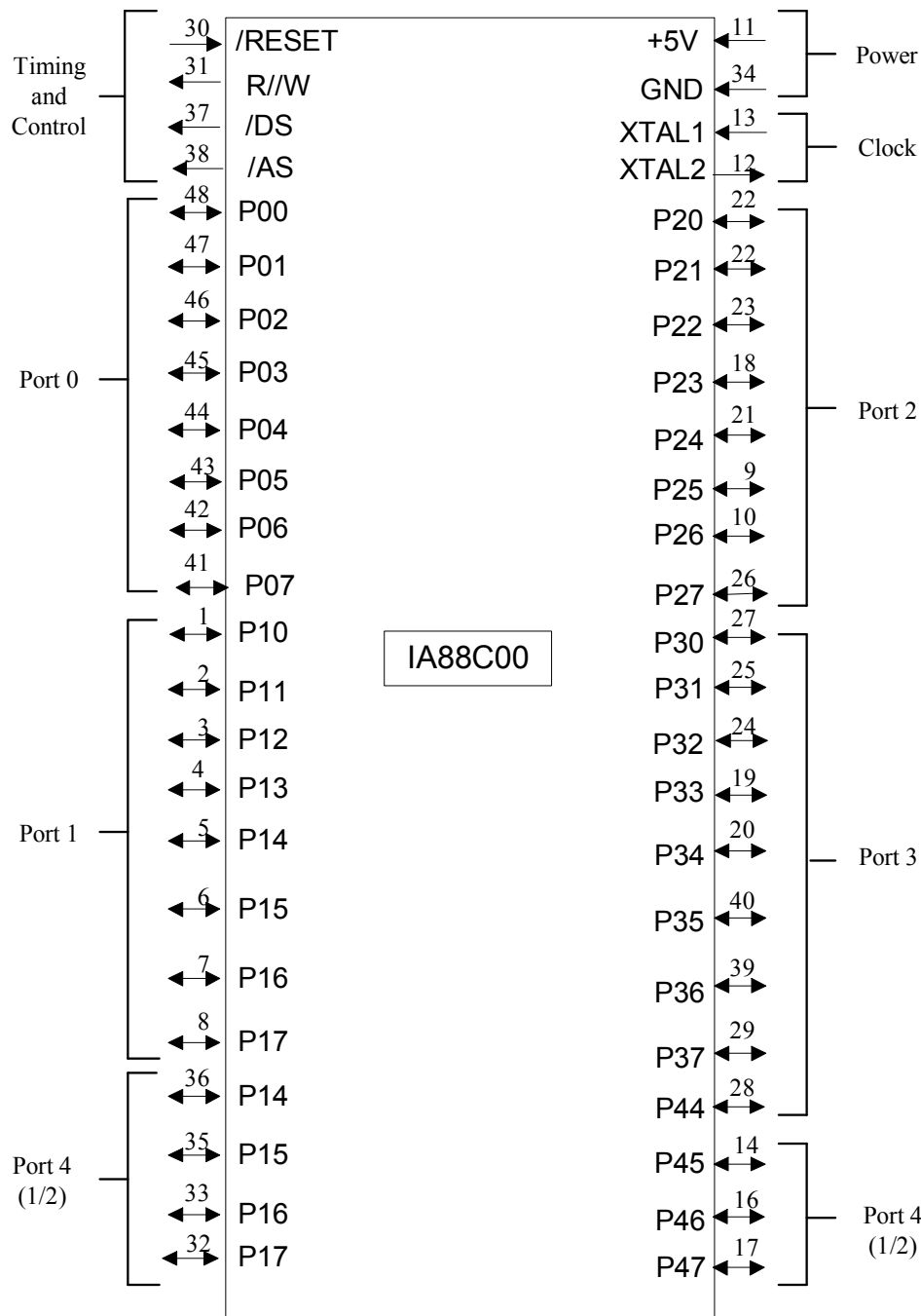


Figure 6. Pin Functions

Architecture

IA88C00 maintains program model compatibility with the Super8 architecture, including 268 general purpose registers and 57 registers for control and mode functions.

The instruction set, is also fully binary compatible supporting all instructions, including multiply and divide instructions and provisions for BCD operations.

The peripheral set maintains register/ program model compatibility. Robust serial communications are provided by an on-board UART. Counter/timers are provided for time-sensitive/control loop applications. A watchdog timer is provided for processor sanity.

Pin Descriptions

/AS Address Strobe The rising edge of this output indicates that address, R/W, and DM (when
(*output, active Low*) appropriate) are valid.

/DS Data Strobe The leading edge of this signal indicates that data is valid during a write cycle.
(*output, active Low*) The trailing edge of this signal is used to latch data into the IA88C00 during a read cycle.

P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, Port I/O Lines (*input/output*) Input/Output Ports configured under program control. Specific functions include:

Port 1 serves as the multiplexed address/data port. It serves as the data bus de-multiplexed mode, and **Port 0** pins can be used as additional address lines or general purpose I/O.

Ports 2 and 3 provide support for interrupts, the UART and the timers. Alternatively, they can be programmed as general purpose I/O.

Port 4 is used for general I/O or as the lower address byte in de-mux mode.

/RESET (*input, active Low*) Reset input. Reset vector is address 0020H.

R/W Read/Write When high, the current bus operation is a read. When low, the current bus
(*output*) operation is a write.

XTAL1, XTAL2 Crystal inputs for the internal oscillator.
(*Crystal oscillator input*)

All port pins are configured as inputs (high impedance) during RESET, except for Port 1 and Port 0. Port 1 is configured as a multiplexed address/ data bus. Port 0 pins P00-P04 are configured as address out. And pins P05-P07 are configured as inputs.

Registers

The IA88C00 supports a 256-byte register address space. Addresses 00H-BFH contain two sets of registers. Set one contains control registers that are only accessible by register direct commands. Set two contains data registers that are only available via register indirect, indexed, stack and DMA commands,

Note that address space E0H to FFH in Set one is further divided into two banks. The state of bank select bit in the Flag register determines which bank is accessed.

The register space is shown in Figure 7.

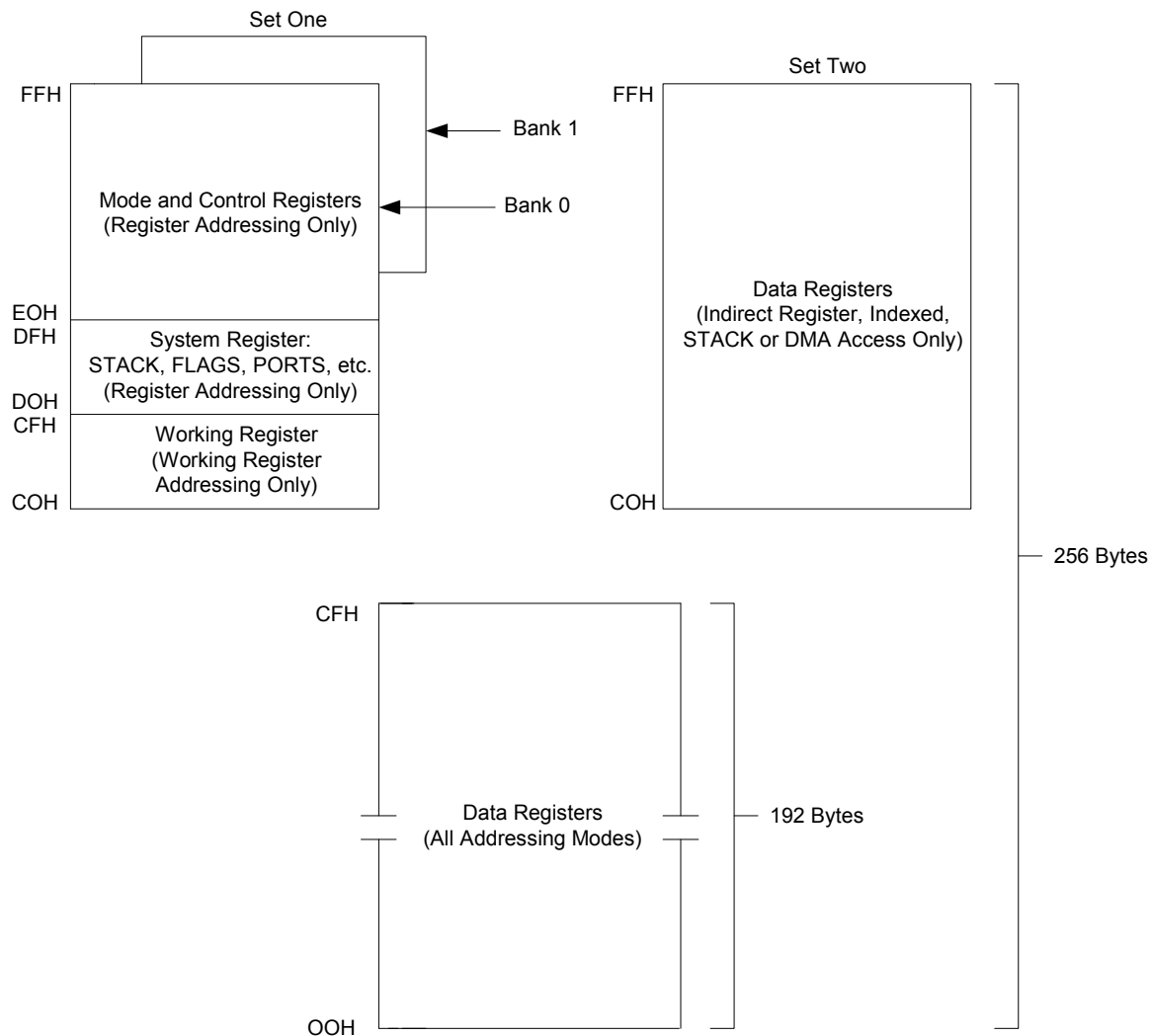


Figure 7. IA88C00Registers

Working Register Window

Working registers are those registers found within a moveable 8-register section of the register space. These moveable 8-register sections are defined by register pointers RP0 and RP1, which are control registers R214 and R215.

Short 4-bit addresses are used to access working registers. The process of accessing working registers, shown in a section of Figure 7, occurs as follows:

- The process results in linking together the five bits from the register pointer to the three bits from the address to form an 8-bit address. The three bits from the address will always point to an address within the same eight registers, as long as the address in the register pointer remains unchanged.

Using full 8-bit addressing allows the working registers to be accessed. The lower nibble is used similarly to the 4-bit addressing described above when an 8-bit logical address in the range 192 to 207 (C0 to CF) is specified. This is shown in section b. of Figure 8.



Physical registers 192 to 207 can be accessed only when selected by a register pointer. This is because any direct access to logical addresses 192 to 207 involves the register pointers. After a reset, RP0 points to R192 and RP1 points to R200.

Register List

Figure 9 displays the IA88C00 registers. For more details, see the registers presented under Mode and Control Registers.

Figure 9. IA88C00 Registers

| Decimal | Address | Hexadecimal | Mnemonic | Function |
|-----------------------------------|---------|-----------------|---------------------------------|-------------------------------------|
| General Purpose Registers | | | | |
| 00-192 | | 00-BF | - | General purpose (all address modes) |
| 192-207 | | 00-CF | - | Working Register (direct only) |
| 192-255 | | C0-FF | - | General purpose (indirect only) |
| Mode and Control Registers | | | | |
| 208 | | D0 | P0 | Port 0 I/O bits |
| 209 | | D1 | P1 | Port 1 (I/O only) |
| 210 | | D2 | P2 | Port 2 |
| 211 | | D3 | P3 | Port 3 |
| 212 | | D4 | P4 | Port 4 |
| 213 | | D5 | FLAGS | System Flags Register |
| 214 | | D6 | RP0 | Register Pointer 0 |
| 215 | | D7 | RP1 | Register Pointer 1 |
| 216 | | D8 | SPH | Stack Pointer Low Byte |
| 217 | | D9 | SPL | Stack Pointer High Byte |
| 218 | | DA | IPH | Instruction Pointer High Byte |
| 219 | | DB | IPL | Instruction Pointer Low Byte |
| 220 | | DC | IRQ | Interrupt Request |
| 221 | | DD | IMR | Interrupt Mask Register |
| 222 | | DE | SYM | System Mode Register |
| 223 | | DF | HMR | Hall Mode Register |
| 224 | | E0 | Bank 0 COCT | CTR 0 Control |
| | | Bank 1 COM | CTR 0 Mode | |
| 225 | | E1 | Bank 0 C1CT | CTR 1 Control |
| | | Bank 1 C1M | CTR 1 Mode | |
| 226 | | E2 | Bank 0 COCH | CTR 0 Capture Register, bits 8-15 |
| | | Bank 1 COTCH | CTR 0 Timer Constant, bits 8-15 | |
| 227 | | E3 | Bank 0 COCL | CTR 0 Capture Register, bits 0-7 |
| | | Bank 1 COTCL | CTR 0 Time Constant, bits 0-7 | |
| 228 | | E4 | Bank 0 C1CH | CTR 1 Capture Register, bits 8-15 |
| | | Bank 1 C1TCH | CTR 1 Time Constant, bits 8-15 | |
| 229 | | E5 | Bank 0 C1CL | CTR 1 Capture Register, bits 0-7 |
| | | Bank 1 C1TCL | CTR 1 Time Constant, bits 0-7 | |
| 230 | | E6 | Bank 0 CTPRS | Counter Prescaler |
| 230 | | E6 | Bank 1 WDTSMR | Watch-Dog/Stop Mode Register |
| 235 | | EB | Bank 0 UTC | UART Transmit Control |

| | | | | |
|-----|----|--------|-------|-------------------------------------|
| 236 | EC | Bank 0 | URC | UART Receive Control |
| 237 | ED | Bank 0 | UIE | UART Interrupt Enable |
| 238 | EE | Bank 0 | UTI | Transmit Interrupt Register |
| 239 | EF | Bank 0 | UIO | UART Data |
| 240 | F0 | Bank 0 | POM | Port 0 Mode |
| | | Bank 1 | DCH | DMA Count, bits 8-15 |
| 241 | F1 | Bank 0 | PM | Port Mode Register |
| | | Bank 0 | DCL | DMA Count, bits 0-7 |
| 244 | F4 | Bank 0 | H0C | Handshake Channel 0 Control |
| 245 | F5 | Bank 0 | H1C | Handshake Channel 1 Control |
| 246 | F6 | Bank 0 | P4D | Port 4 Direction |
| 247 | F7 | Bank 0 | P4OD | Port 4 Open Drain |
| 248 | F8 | Bank 0 | P2AM | Port 2/3 A Mode |
| | | Bank 1 | UBGH | UART Baud Rate Generator, bits 8-15 |
| 249 | F9 | Bank 0 | P2BM | Port 2/3 B Mode |
| | | Bank 1 | UBGL | UART Baud Rate Generator, bits 0-7 |
| 250 | FA | Bank 0 | P2CM | Port 2/3 C Mode |
| | | Bank 1 | UMA | UART Mode A |
| 251 | FB | Bank 0 | P2DM | Port 2/3 D Mode |
| | | Bank 1 | UMB | UART Mode B |
| 252 | FC | Bank 0 | P2AIP | Port 2/3 A Interrupt Pending |
| 253 | FD | Bank 0 | P2BIP | Port 2/3 B Interrupt Pending |
| 254 | FE | Bank 0 | EMT | External Memory Timing |
| | | Bank 1 | WUMCH | Wake-up Match Register |
| 255 | FF | Bank 0 | IPR | Interrupt Priority Register |
| | | Bank 0 | WUMSK | Wake-up Mask Register |

Mode and Control Registers

Figure 10. R213 (D5) Flags System Flags Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-------|------|------|----------|----------------|------------|----------------|------|
| | Carry | Zero | Sign | Overflow | Decimal Adjust | Half-Carry | Fast Interrupt | Bank |
| Initial Value | ? | ? | ? | ? | ? | ? | ? | ? |
| Read/Write | R | R | R | R | R | R | R | R/W |

The flag register contains eight bits that describe the current status of the processor. Four of these bits can be tested and used with conditional jump instructions. Two others are used for BCD arithmetic. Also contained in the flag register are the Bank Address bit and the Fast Interrupt Status bit.

Bit 7: Carry Flag - This is set to 1 if the result from an arithmetic operation generates carry out of, or borrow into, bit 7.

Bit 6: Zero Flag - For arithmetic and logical operations, this flag is set to 1 if the result of the operation is 0. For operations that test bits in a register, the 0 bit is set to 1 if the result is 0. For rotate and shift operations, this bit is set to 1 if the result is 0.

Bit 5: Sign Flag - Following arithmetic, logical, rotate or shift operations, this bit identifies the state of the MSB of the result. A 0 indicates a positive number and a 1 indicates a negative number.

Bit 4: Overflow Flag - This flag is set to 1 when the result of a two's-complement operation was greater than 127 or less than -128. It is also cleared to 0 during logical operations.

Bit 3: Decimal Adjust - This bit is used to specify what type of instruction was executed last during BCD operations, so a subsequent decimal adjust operation can function correctly. This bit is not usually accessible to programmers and cannot be used as a test condition.

Bit 2: Half-Carry Flag - This bit is set to 1 whenever an addition generates a carry out of bit 3, or when a subtraction borrows out of bit 4. This bit is used by the Decimal Adjust (DA) instruction to convert the binary result of a previous addition or subtraction into the correct decimal (BCD) result. This flag and the Decimal Adjust flag are not usually accessed by users.

Bit 1: Fast Interrupt Status - This bit is set during a fast interrupt cycle and reset during the IRET following interrupt servicing. When set, this bit inhibits all interrupts and causes the fast interrupt return to be executed when the IRET instruction is fetched.

Bit 0: Bank Address - This bit is used to select one of the register banks (0 or 1) between (decimal) addresses 224 and 255. It is cleared by the SB0 instruction and set by the SB1 instruction.

Figure 11. R214 (D6) RP0 Register Pointer 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|----------|----------|----------|
| | RP7 | RP6 | RP5 | RP4 | RP3 | Not Used | Not Used | Not Used |
| Initial Value | 1 | 1 | 0 | 0 | 0 | - | - | - |
| Read/Write | R/W | R/W | R/W | R/W | R/W | - | - | - |

Register Pointer 0 (RP0) defines a moveable, 8-register section of the register space. The registers within these spaces are called working registers. RP0 is used in addressing modes where the register operand is expressed as a 4-bit address.

At reset, RP0 points to R192.

Figure 12. R215 (O7) RP1 Register Pointer 1

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|----------|----------|----------|
| | RP7 | RP6 | RP5 | RP4 | RP3 | Not Used | Not Used | Not Used |
| Initial Value | ? | ? | ? | ? | ? | ? | ? | ? |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Register Pointer 1 (RP1) defines a moveable, 8-register section of the register space. The registers within these spaces are called working registers. RP1 is used in addressing modes where the register operand is expressed as a 4-bit address.

At reset, RP0 points to R200.

Figure 13. R216 (D8) SPH Stack Pointer

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|------|------|------|------|------|------|-----|-----|
| | SP15 | SP14 | SP13 | SP12 | SP11 | SP10 | SP9 | SP8 |
| Initial Value | | | | | | | | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Stack operations are supported in the register file or in data memory. Bit 1 in the external Memory Timing register (R254B0) selects between the two.

Register pair R216-R217 forms the Stack Pointer used for all stack operations. R216 is the MSB and R217 is the LSB.

The Stack Pointer always points to data stored on the tip of the stack. The address is decremented prior to a PUSH and incremented after a POP.

The stack is also used as a return stack for CALLS and interrupts. During a CALL, the contents of the PC are saved on the stack to be restored later. Interrupts cause the contents of the PC and FLAGS to be saved on the stack for recovery by IRET when the interrupt is finished.

When configured for internal stack (using the register file), R217 contains the Stack Pointer. R216 can be used as a general purpose register. However, its contents will be changed if an overflow or underflow occurs as the result of incrementing or decrementing the stack address during normal stack operations.

A user-defined stack can be implemented in both the register file and program or data memory. These can be made to increment or decrement on a push by the choice of opcodes. For example, to implement a stack that goes from Low addresses to High addresses in the register file, use PUSHUI and POPUD. For a stack that goes from High address to Low addresses in data memory, use LDEI for POP and LDEPD for PUSH.

Figure 14. R217 (D9) SPL Stack Pointer

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 |
| Initial Value | | | | | | | | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Stack operations are supported in the register file or in data memory. Bit 1 in the external Memory Timing register (R254B0) selects between the two.

Register pair R216-R217 forms the Stack Pointer used for all stack operations. R216 is the MSB and R217 is the LSB.

The Stack Pointer always points to data stored on the tip of the stack. The address is decremented prior to a PUSH and incremented after a POP.

The Stack is also used as a return stack for CALLS and interrupts. During a CALL, the contents of the PC are saved on the stack to be restored later. Interrupts cause the contents of the PC and FLAGS to be saved on the stack for recovery by IRET when the interrupt is finished.

When configured for internal stack (using the register file), R217 contains the Stack Pointer. R216 can be used as a general purpose register. However, its contents will be changed if an overflow or underflow occurs as the result of incrementing or decrementing the stack address during normal stack operations.

A user-defined stack can be implemented in both the register file and program or data memory. These can be made to increment or decrement on a push by the choice of opcodes. For example, to implement a stack that goes from Low addresses to High addresses in the register file, use PUSHUI and POPUD. For a stack that goes from High address to Low addresses in data memory, use LDEI for POP and LDEPD for PUSH.

Figure 15. Instruction Pointer High (IPH), R218

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|------|------|------|------|------|------|-----|------|
| | IP15 | IP14 | IP13 | IP12 | IP11 | IP10 | IP9 | IPO8 |
| Initial Value | ? | ? | ? | ? | ? | ? | ? | ? |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

A special register called the Instruction Pointer (IP) provides hardware support for threaded-code languages. It consists of register-pair R218-R219 and contains memory addresses. The MSB is R218. Threaded-code languages deal with an imaginary higher-level machine within the existing hardware machine. The IP acts like the PC for that machine. The command NEXT passes control to or from the hardware machine to the imaginary machine. And the commands ENTER and EXIT are imaginary machine equivalents of real machine CALLS and RETURNS.

If the commands NEXT, ENTER and EXIT are not used, the IP can be used by the fast interrupt processing, as described in the interrupts section.

Figure 16. Instruction Pointer Low (IPL), R219

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 |
| Initial Value | ? | ? | ? | ? | ? | ? | ? | ? |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

A special register called the Instruction Pointer (IP) provides hardware support for threaded-code languages. This register consists of register pair R218-R219 and contains memory addresses. The MSB is R218. Threaded-code languages deal with an imaginary higher-level machine within the existing hardware machine. The IP acts like the PC for that machine. The command NEXT passes control to or from the hardware machine to the imaginary machine. And the commands ENTER and EXIT are imaginary machine equivalents of real machine CALLS and RETURNS.

The IP can be used by the fast interrupt processing, as described in the interrupts section, if the commands NEXT, ENTER and EXIT are not used.

Figure 17. Interrupt Mask (IRM), R221

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|---------|---------|---------|---------|---------|---------|---------|---------|
| | Level 7 | Level 7 | Level 7 | Level 7 | Level 7 | Level 7 | Level 7 | Level 7 |
| Initial Value | ? | ? | ? | ? | ? | ? | ? | ? |
| Read/Write | R | R | R | R | R | R | R | R |

When an interrupt in one of the 8 levels occurs and the corresponding mask bit is not set, the level bit of the interrupt is set to 1. The interrupt structure contains 8 levels of interrupt, 16 vectors and 27 sources. Interrupt priority is assigned by level and controlled by the Interrupt Priority Register (IPR) ControlRegR255B0. Each level is masked (or enabled) according to the bits in the Interrupt Mask Register (IMR) SystemRegR221. Each bit of the Interrupt Mask register corresponds to one of the 8 levels of interrupts, IRQ register (SystemRegR220). When the corresponding bit in the Interrupt Mask register is set to one, that level interrupt is disabled.

Figure 18. System Mode Register (SYM), R222

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|----------|----------|----------|------|------|------|-----|-----|
| | Not Used | Not Used | Not Used | FIS2 | FSI1 | FSI0 | FSE | GIE |
| Initial Value | ? | ? | ? | ? | ? | ? | ? | ? |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The Fast Interrupt Select (FSI) selects which level interrupt can be treated as a fast interrupt. Fast Interrupt Enable (FSE), when set to 1, enables the selected level for fast interrupt. Global Interrupt Enable (GIE), when set to 1, enables interrupts in general.

Figure 19. Halt Mode Register (HMR), R223

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|----------|----------|----------|----------|-----|-----|-----|-----|
| | Not Used | Not Used | Not Used | Not Used | D3 | D2 | D1 | D0 |
| Initial Value | ? | ? | ? | ? | 1 | 1 | 1 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

D3 - CPU HALT mode - Writing a zero to this bit will invoke the HALT mode upon the execution of the WFI instruction. The UART and counters can be halted only if D3 is 0. During HALT the internal CPU clock is disabled, and no address strobe is generated. A hardware reset sets this bit to a 1.

D2 - Disable UART - Writing a zero to the bit will disable the UART. No interrupt request will be generated. A 1 will make the UART and its interrupt logic remain active in HALT mode. A hardware reset forces this bit to a 1.

D1 - Disable CT1 - Similar to CT0. When the counters are cascaded, the HALT mode 32-bit counter is determined by the logical state of D1. A hardware reset forces this bit to a 1.

D0 - Disable CT0 - Writing a zero to this bit will disable the CT0 in HALT mode. No interrupt request will be generated in this case. A 1 will keep the CT0 active. A hardware reset forces this bit to a 1.

Figure 20. Counter 0 Control Register (C0CT), R224 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | X | X | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

D0 - When this bit is set to 1, the counter/timer is enabled. Operation begins on the rising edge of the first processor clock period following the setting of this bit from a previously cleared value. Writing a 1 in this field when the previous value was 1 has no effect on the operation of the counter/timer. When this bit is cleared to 0, the counter/timer performs no operation during the next (and subsequent) processor clock periods. A hardware reset forces this bit to 0.

Both counters are clocked by the rising edge of the incoming signal on P26 or p36 after the counter is enabled. The maximum frequency of the external clock signal applied to P36 (or P26) equals the maximum Xtal frequency divided by 4. The maximum guaranteed Xtal frequency is 20 MHz, which implies a maximum counter frequency of 5 MHz.

D1 - Reset/End of Count Status - This bit is set to 1 each time the counter reaches 0. Writing a 1 to this bit resets it, while writing a 0 has no effect.

D2 - Zero Count Interrupt Enable - When this bit is set to 1, the counter/timer generates an interrupt request when it counts to 0. A hardware reset forces this bit to 0.

D3 - Software Capture - When this bit is set to 1, the current counter value is loaded into the capture register. This bit is automatically cleared following the capture.

D4 - Software Trigger - This bit is effectively "ORed" with the external rising-edge trigger input and can be used by the software to force a trigger signal. This bit produces a trigger signal regardless of the setting of the Input Pin Assignment field of the Mode register. This bit is automatically cleared following the trigger.

D5 - Load Counter - The contents of the Time Constant register are transferred to the Counter prescaler one clock period after this bit is set. This operation alone does not start the counter. This bit is automatically cleared following the load.

D6 - Count Up/Down - This bit determines the count direction if internal up/down control is specified in the Mode register. 1 indicates up; 0 indicates down.

D7 - Continuous/Single Cycle - When this bit is set to 1, the counter is reloaded with the time-constant value when the counter reaches the end of the terminal count. The terminal count for down counting is 0000, while the one for up counting is FFFF. When this bit is cleared to 0, no reloading occurs.

Figure 21. Counter 0 Mode, R224

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | X | X | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

D0 - When this bit is set to 1, the counter/timer is enabled. Operation begins on the rising edge of the first processor clock period following the setting of this bit from a previously cleared value. Writing a 1 in this field when the previous value was 1 has no effect on the operation of the counter/timer. When this bit is cleared to 0, the counter/timer performs no operation during the next (and subsequent) processor clock periods. A hardware reset forces this bit to 0.

Both counters are clocked by the rising edge of the incoming signal on P26 or p36 after the counter is enabled. The maximum frequency of the external clock signal applied to P36 (or P26) equals the maximum Xtal frequency divided by 4. The maximum guaranteed Xtal frequency is 20 MHz, which implies a maximum counter frequency of 5 MHz.

D1 - Reset/End of Count Status - This bit is set to 1 each time the counter reaches 0. Writing a 1 to this bit resets it, while writing a 0 has no effect.

D2 - Zero Count Interrupt Enable - When this bit is set to 1, the counter/timer generates an interrupt request when it counts to 0. A hardware reset forces this bit to 0.

D3 - Software Capture - When this bit is set to 1, the current counter value is loaded into the capture register. This bit is automatically cleared following the capture.

D4 - Software Trigger - This bit is effectively "ORed" with the external rising-edge trigger input and can be used by the software to force a trigger signal. This bit produces a trigger signal regardless of the setting of the Input Pin Assignment field of the Mode register. This bit is automatically cleared following the trigger.

D5 - Load Counter - The contents of the Time Constant register are transferred to the Counter prescaler one clock period after this bit is set. This operation alone does not start the counter. This bit is automatically cleared following the load.

D6 - Count Up/Down - This bit determines the count direction if internal up/down control is specified in the Mode register. 1 indicates up; 0 indicates down.

D7 - Continuous/Single Cycle - When this bit is set to 1, the counter is reloaded with the time-constant value when the counter reaches the end of the terminal count. The terminal count for down counting is 0000, while the one for up counting is FFFF. When this bit is cleared to 0, no reloading occurs.

Figure 22. Counter 0 Mode, R225

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | X | X | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

D0 - When this bit is set to 1, the counter/timer is enabled. Operation begins on the rising edge of the first processor clock period following the setting of this bit from a previously cleared value. Writing a 1 in this field when the previous value was 1 has no effect on the operation of the counter/timer. When this bit is cleared to 0, the counter/timer performs no operation during the next (and subsequent) processor clock periods. A hardware reset forces this bit to 0.

Both counters are clocked by the rising edge of the incoming signal on P26 or p36 after the counter is enabled. The maximum frequency of the external clock signal applied to P36(or P26) equals the maximum Xtal frequency divided by 4. The maximum guaranteed Xtal frequency is 20 MHz, which implies a maximum counter frequency of 5 MHz.

D1 - Reset/End of Count Status - This bit is set to 1 each time the counter reaches 0. Writing a 1 to this bit resets it, while writing a 0 has no effect.

D2 - Zero Count Interrupt Enable - When this bit is set to 1, the counter/timer generates an interrupt request when it counts to 0. A hardware reset forces this bit to 0.

D3 - Software Capture - When this bit is set to 1, the current counter value is loaded into the capture register. This bit is automatically cleared following the capture.

D4 - Software Trigger - This bit is effectively "ORed" with the external rising-edge trigger input and can be used by the software to force a trigger signal. This bit produces a trigger signal regardless of the setting of the Input Pin Assignment field of the Mode register. This bit is automatically cleared following the trigger.

D5 - Load Counter - The contents of the Time Constant register are transferred to the Counter prescaler one clock period after this bit is set. This operation alone does not start the Counter. This bit is automatically cleared following the load.

D6 - Count Up/Down - This bit determines the count direction if internal up/down control is specified in the Mode register. 1 indicates up; 0 indicates down.

D7 - Continuous/Single Cycle - When this bit is set to 1 the counter is reloaded with the time-constant value when the counter reaches the end of the terminal count. The terminal count for down counting is 0000, while the one for up counting is FFFF. When this bit is cleared to 0, no reloading occurs.

Figure 23. Counter 0 Capture Register (High Byte) (C0CH), R226 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | X | X | X | X | X | X | X | X |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

This 16-bit register pair is used to hold the counter value saved when using the "capture on external event" function. This register will capture at the rising edge of the I/O pin or when software capture is asserted. When the bi-value mode of operation is enabled, this register is used as a second Time Constant register and the counter is alternately loaded from each.

Figure 24. Counter 0 Capture Register (Low Byte) (C0CL), R227 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | X | X | X | X | X | X | X | X |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

This 16-bit register pair is used to hold the counter value saved when using the "capture on external event" function. This register will capture at the rising edge of the I/O pin or when software capture is asserted. When the bi-value mode of operation is enabled, this register is used as a second Time Constant register and the counter is alternately loaded from each.

Figure 25. Counter 1 Time Constant Register (High Byte) (C1CTH), R228 Bank 1

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | X | X | X | X | X | X | X | X |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

This 16-bit register pair holds the value that is automatically loaded into the counter/timer (1) when the counter/timer is enabled, (2) when the count reaches zero in continuous mode or (3) when the trigger is asserted in re-trigger mode. If capture on both edges is enabled, this register captures the contents of the counter on the falling edge of the I/O pin.

Figure 26. Counter 1 Capture Register (Low Byte) (C1CL), R229 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-------------|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | C1C7 – C1C0 | | | | | | | |
| Initial Value | X | X | X | X | X | X | X | X |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

This 16-bit register pair is used to hold the counter value saved when using the "capture on external event" function. This register will capture at the rising edge of the I/O pin or when software capture is asserted. When the bi-value mode of operation is enabled, this register is used as a second Time Constant register and the counter is alternately loaded from each.

Figure 27a. Counter 0 Prescaler (CTPRS), R230 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|----------|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | CT1 | | | Not Used | | CT0 | | |
| Initial Value | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

This register controls the source of the timer signal when in internal mode. An 8-bit prescaler for each counter is implemented. The control bit operate as follows:

| CT0/CT1 | Prescale |
|---------|----------|
| 000 | XTAL/2 |
| 001 | XTAL/4 |
| 010 | XTAL/8 |
| 011 | XTAL/16 |
| 100 | XTAL/32 |
| 101 | XTAL/64 |
| 110 | XTAL/128 |
| 111 | XTAL/256 |

Only the prescaler of CT1 is activated when the counters are cascaded.

Figure 28b. Watch Dog Timer and Stop Mode Recovery Register (WDT/SMR) R230 Bank0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|--------------|-----|------------|-------------|------------|--------|------------|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | WDT time-out | | WDT Enable | WDT in Stop | WDT Source | SMR On | SMR Source | |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

This register controls the Watchdog Timer time-out and Stop recovery mode.

D1, D0 Stop Mode Recovery source select.
Bit D0 and D1 determine the Stop Mode Recovery source.

| D1 | D0 | |
|----|----|--|
| 0 | 0 | Recovery from RESET only |
| 0 | 1 | Recovery from P22 and RESET |
| 1 | 0 | Recovery from P32 and RESET |
| 1 | 1 | Recovery from any input for Port 4 and RESET |

A hardware reset forces D0 and D1 to zero.

D2 Stop Recovery Edge

A 1 in this position indicates that a rising edge on any one of the recovery sources wakes the IA88C00 from Stop mode. A 0 indicates falling edge recovery. The reset value is 0.

D3 XTAL1/RC Select for WDT

When a zero is written to D3, the clock of the WDT is driven by the on-board RC oscillator. If D3 is set to 1, the WDT is driven by XTAL1. D3 has a zero reset value.

D4 WDT Enable During STOP or HALT

When this bit is set, WDT is enabled during STOP or HALT. In this case, recovery from STOP or HALT should be performed before the selected time-out. A 0 in this bit location disables the WDT while the IA88C00 is stopped or halted. A hardware reset forces this bit to a zero.

D5 WDT

The Watch-Dog Timer is initially enabled by writing a 1 to D5 and retriggered on subsequent writings to the same bit. Reset value = 0. Writing a 0 to this bit has no effect. Once a 1 is written to D5, it persists until a hardware reset occurs.

D6, D7 WDT Time-Out

Two sets of four different time-out values can be selected, depending on the logical state of these bits. A normal reset signal must be active low during 5 XTAL clock periods. Using the reset signal input to recover from STOP mode requires 10 XTAL clock periods. This is so that XTAL oscillation starts up and stabilizes, generating a good oscillator output level.

The reset pin is held low in source during WDT timer time-out to accomplish a system reset with other peripherals of the Super8. When the reset pin is held low, the capability of sink current via the reset pin should be considered. (See DC Characteristics.)

Figure 29. UART Transmit Control (UTC), R235 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

This register contains the status and command bits needed to control the transmit sections of the UART.

0 - TDMAENB - Transmit DMA Enable - When this bit is set to 1, the DMA function for the UART transmit section is enabled. If this bit is set and the Transmit Buffer Empty signal becomes true, a DMA request is made. When the DMA channel gains control of the bus, it transfers bytes from the external memory or the register file to the UART transmit section. A hardware reset forces this bit to 0.

D1 - TBE - Transmit Buffer Empty - This status bit is set to 1 whenever the transmit buffer is empty. It is cleared to 0 when a data byte is written in the transmit buffer. A hardware reset forces this bit to 1.

D2 - ZC - Zero Count - This status bit is set to 1 and latched when the counter in the baud-rate generator reaches the count of 0. This bit can be cleared to 0 by writing a 1 to this bit position. A hardware reset forces this bit to 0.

D3 - TENB - Transmit Enable - Data is not transmitted until this bit is set to 1. When cleared to 0, the Transmit Data pin continuously outputs 1s unless Auto-Echo mode is selected. This bit should be cleared only after the desired transmission of data in the buffer is completed. A hardware reset forces this bit to 0.

D4 - WUEB - Wake-up Enable - If this bit is set to 1, wake-up mode is enabled for both the transmitter and the receiver. The transmitter adds a bit beyond those specified by the bits/character and the parity. This added bit has the value specified in the Transmit Wake-up Value (TWUVAL) in the UMA register (ControlRegR250B0). The receiver expects a Wake-Up bit value in the incoming data stream after the parity bit and compares this value with that specified in the Received Wake-Up value (RWVAL) bit in the UMA register. The resulting action depends on the configuration of the Wake-up feature.

D5 - STPBTS - Stop Bits - This bit determines the number of stop bits added to each character transmitted from the UART transmit section. If this bit is a 0, one stop bit is added. If this bit is a 1, two stop bits are added. The receiver always checks for at least one stop bit. A hardware reset forces this bit to 0.

D6 - SENBRK - Send Break - When set to 1, this bit forces the transmit section to continuously output 0s, beginning with the following transmit clock, regardless of any data being transmitted at the time. This bit functions whether or not the transmitter is enabled. When this bit is cleared to 0, the transmit section continues to send the contents of the Transmit Data Register. A hardware reset forces this bit to 0.

D7 - TXDTSSEL - Transmit Data Select - This bit has an effect only if port pin P31 is configured as an output. If this bit is set to 1, the serial data coming out of the transmit section is reflected on the P31 pin. If this bit is set to 0, P31 acts as a normal port and P31 data is reflected on the P31 pin. A hardware reset forces this bit to 0.

Figure 30. UART Receive Control (URC), R236 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |

D0 - RCA - Receive Character Available - This is a status bit that is set to a 1 when data is available in the receive buffer (UIOR). When the CPU reads the receive buffer, it automatically clears this bit to 0. A write to this position has no effect. A hardware reset forces this bit to 0.

D1 - RENB - Receive Enable - When this bit is set to 1, the receive operation begins. This bit should be set only after all other receive parameters are established and the receiver is completely initialized. A hardware reset clears this bit to 0.

D2 - PERR - Parity Error - This is a status bit. When parity is enabled, this bit is set to 1 and buffered with the character whose parity does not match the programmed parity (even/odd). This bit is latched so that once an error occurs, it remains set until it is cleared to 0 by writing a 1 to this bit position.

D3 - OVERR - Overrun Error - This status bit indicates that the receive buffer has not been read and another character has been received. Only the character that has been written over is flagged with this error. Once set, this bit remains set until cleared to 0 by writing a 1 to this bit position.

D4 - FERR - Framing Error - This is a status bit. If a framing error occurs (no stop bit where expected), this bit is set for the receive character in which the framing error occurred. This bit remains set until cleared to 0 by writing a 1 to this bit position.

D5 - BRKD - Break Detect - This is a status bit that is set at the beginning and the end of a break sequence in the receive data stream. It stays set to 1 until cleared to 0 by writing a 1 to this bit position. A break signal is a sequence of 0s. When all the required bits, parity bit, wake-up bit, and stop bits are 0x, the receiver immediately recognizes a break condition (not a framing error) and causes Break Detect (BRKD) to be set and an interrupt request. At the end of the break signal, a zero character is loaded into the Receive Data Register (UIOR) and Break Detect is set again, along with another interrupt request.

D6 - CCD - Control Character Detect - This status bit is set any time an ASCII control character is received in the receive data stream. It stays set until cleared to 0 by writing a 1 to this bit position. (An ASCII control character is any character that has bits 5 and 6 set to 0.)

D7 - WUD - Wake-Up Detect - This status bit is set any time a valid wake-up condition is detected at the receiver. It stays set until cleared to 0 by writing a 1 to this bit position. The wake-up condition can be satisfied in many possible ways by the Wake-up bit, Wake-up Match register, and Wake-Up Mask register.

Figure 31. UART Interrupt Enable (UIE), R237 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

D0 - RCAIE - Receive Character Available Interrupt Enable - If this bit is set to 1, a Receive Character Available status in the URC register will cause an interrupt request. In a DMA receive operation, if this bit is set to 1, an interrupt request will be issued only if an End-of-Process (EOP) of the DMA counter is also set. If it is not set, a Receive Character Available status causes no interrupt.

D1 - RDMAENB - Receive DMA Enable - When this bit is set to 1, the DMA function is enabled for the UART receiver. Whenever a Receive Character Available signal in the URC register is true, a DMA request will be made. When the DMA channel claims control of the bus, it transfers the received data to the register file or the external memory.

D2 - TIE - Transmit Interrupt Enable - If this bit is set to 1, a Transmit Buffer Empty signal in the UTC register will cause an interrupt request. In a DMA transmit operation, if this bit is set to 1, an interrupt request will be issued only if an End-of-Process (EOP) of the DMA counter is also set. If it is not set, a Transmit Buffer Empty signal causes no interrupt.

D3 - ZCIE - Zero Count Interrupt Enable - If this bit is set to 1, a baud-rate generator Zero Count status in the UTC register will cause an interrupt request.

D4 - REIE - Receive Error Interrupt Enable - If this bit is set to 1, any receiver error condition will cause an interrupt request. Possible receive error conditions include parity error, overrun error and framing error.

D5 - BRKIE - Break Interrupt Enable - If this bit is set to 1, a transition in either direction on the break signal will cause an interrupt request.

D6 - CCIE - Control Character Interrupt Enable - If this bit is set to 1, an ASCII Control Character Detect signal in the URC register will cause an interrupt.

D7 - WUIE - Wake-Up Interrupt Enable - If this bit is set to 1, any of the wake-up conditions that set the Wake-Up Detect bit (WUD) in the URC register will cause an interrupt request.

Figure 32. UART Transmit Interrupt Register, UTI R238 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/O | R/W |

The timing for the transmit buffer empty interrupt is software programmable. There are two different interrupt timings selectable with 1 bit.

Option 1: Interrupt is activated at the moment the contents of the TUIO register are transferred to the Tx FIFO.

Option 2: Interrupt is activated at the moment the last stop bit in the Tx FIFO is sent.

After loading the transmit shift register, UART control generates a buffer empty flag to indicate that TUIO is ready to be filled with new data.

A new flag will indicate when the transmit shift register is empty.

D0 - If this bit is zero, a high value of D2 in the UIE register will cause an interrupt on Transmit UIO empty. If this bit is set, a high value of D2 in the UIE register will cause an interrupt on transmit shift register empty. That is when the last stop bit is transmitted. This bit should be programmed prior to writing to the UIO register.

D1 - This flag is set when the transmit shift register is empty and is reset when a new value is loaded into the UIO. This flag will not be set during a send break.

Figure 33. Uart Data Register (UIO), R239 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | X | X | X | X | X | X | X | X |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/O | R/W |

Writing to this register automatically writes the data in the Transmit Data register (UIOT). A read from this register gets the data from the UART Receive Data register (UIOR).

Figure 34. Port 0 Mode Control Register (P0M), R240 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The Port 0 Mode register programs each bit of Port 0 as an address output (part of an external memory interface) or as an I/O bit. When a bit of this register is 1, the corresponding bit of Port 0 is defined as an address output. When 0, the corresponding bit of Port 0 is defined as an I/O bit. D0-D7 - P00-P07 Mode, 0 = I/O, 1 = Address.

Figure 35. Port Mode Register (pm), R241 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|----|----|----|----|----|----|----|----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | X | X | 1 | 0 | 0 | 0 | 0 | 1 |
| Read/Write | ? | ? | ? | ? | ? | ? | ? | ? |

The Port Mode register provides some additional mode control for Ports 0 and 1.

D0 - Port 0 Direction - If this bit is a 1, all bits of Port 0 configured as I/O will be inputs. If this bit is a 0, the I/O lines will be outputs.

D1 - Open-Drain Port 0 - If this bit is a 1, all bits of Port 0 configured as outputs will be open-drain outputs. If 0, they will be push-pull outputs. This bit has no effect on those bits not configured as outputs.

D2 - Open-Drain Port 1 - If Port 1 is configured as an output port and this bit is a 1, all of the port will be open-drain outputs. If this bit is a 0, they will be push-pull outputs. This bit has no effect if Port 1 is not configured as an output port or A/D 0-7.

D3 - Enable /DM - If this bit is a 1, Port 35 is configured as Data Memory output line /DM.

D4-D5 - This field selects the configuration of Port 1 as an output port, input port, or address/data port as part of the external memory interface.

Figure 36. Handshake 0 Control (H0C), R244 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | X | X | X | X | X | 0 | X | 0 |
| Read/Write | W/O | W/O | W/O | W/O | W/O | W/O | W/O | W/O |

This register controls Handshake Channel 0.

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D0 - Handshake Enable - When this bit is set to 1, the handshake function is enabled.

D1 - Port Select - This bit selects which port is controlled by Handshake Channel 0. When it is set to 1, Port 1 is selected and when it is cleared to 0, Port 4 is selected.

D2 - DMA Enable - When this bit is set to 1, the DMA function is enabled for Handshake Channel 0. When it is cleared to 0, the DMA function is not used by the handshake channel and may be used by the UART.

D3 - Mode - When this bit is set to 1, the "fully interlocked" mode is enabled. When it is cleared to 0, the "strobed" mode is enabled.

D4-D7 - Deskew Counter - This 4-bit field is used to select a count value from 1 to 16 (0000-1111). This value is the number of processor clocks used to generate the set-up and strobe when using the "strobed" mode, or the set-up when using the "fully-interlocked" mode.

Figure 37. Handshake 1 Control (H1C), R245 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | X | X | X | X | X | X | X | 0 |
| Read/Write | W/O | W/O | W/O | W/O | W/O | W/O | W/O | W/O |

This register controls Handshake Channel 1.

D0 - Handshake Enable - When this bit is set to 1, the handshake function is enabled.

D1 - Not Used.

D2 - Not Used.

D3 - Mode - When this bit is set to 1, the "fully interlocked" mode is enabled. When it is cleared to 0, the "strobed" mode is enabled.

D4-D7 - Deskew Counter - This 4-bit field is used to select a count value from 1 to 16 (0000-1111). This value is the number of processor clocks used to generate the set-up and strobe when using the "strobed" mode, or the set-up when using the "fully-interlocked" mode.

Figure 38. Port 4 Direction Control Register (P4D), R246 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The Port 4 Direction register defines the I/O direction of Port 4 on a bit basis. If a bit of this register is a 1, the corresponding bit of Port 4 is configured as an input line. If the bit is a 0, the corresponding bit of Port 4 is configured as an output line.

D0-D7 - P40-P47 Mode, 0 = Output, 1 = Input.

Figure 39. Port 4 Open-Drain (P4OD), R247 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|----|----|----|----|----|----|----|----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | ? | ? | ? | ? | ? | ? | ? | ? |

The Port 4 Open-Drain register defines the output driver type for Port 4. If a bit of Port 4 has been configured as an output and the corresponding bit in the Port 4 Open-Drain register is a 1, the Port 4 bit will have an open-drain output driver. If it is a 0, the Port 4 bit will have a push-pull output driver. If the bit of Port 4 has been configured as an input, the corresponding bit in the Port 4 Open-Drain register has no effect.

Figure 40. Port 4 Open-Drain (P4OD), R247 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | W/O | W/O | W/O | W/O | W/O | W/O | W/O | W/O |

The Port 2/3 A Mode, Port 2/3 B Mode, Port 2/3 C Mode and Port 2/3 D Mode registers control the modes of Ports 2 and 3. A separate 2-bit field for each of the bits of Ports 2 and 3 configures the bit as input or output. The field also controls whether the bit is enabled as an external interrupt source and selects the output as open-drain or push-pull.

Figure 41. Port 2/3 A Mode Register, R248 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | W/O | W/O | W/O | W/O | W/O | W/O | W/O | W/O |

The Port 2/3 A Mode, Port 2/3 B Mode, Port 2/3 C Mode and Port 2/3 D Mode registers control the modes of Ports 2 and 3. A separate 2-bit field for each of the bits of Ports 2 and 3 configures the bit as input or output. The field also controls whether the bit is enabled as an external interrupt source and selects the output as open-drain or push-pull.

Figure 42. Port 2/3 B Mode Register, R249 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | W/O | W/O | W/O | W/O | W/O | W/O | W/O | W/O |

The Port 2/3 A Mode, Port 2/3 B Mode, Port 2/3 C Mode and Port 2/3 D Mode registers control the modes of Ports 2 and 3. A separate 2-bit field for each of the bits of Ports 2 and 3 configures the bit as input or output. The field also controls whether the bit is enabled as an external interrupt source and selects the output as open-drain or push-pull.

Figure 43. Port 2/3 C Mode Register, R250 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | W/O | W/O | W/O | W/O | W/O | W/O | W/O | W/O |

The Port 2/3 A Mode, Port 2/3 B Mode, Port 2/3 C Mode and Port 2/3 D Mode registers control the modes of Ports 2 and 3. A separate 2-bit field for each of the bits of Ports 2 and 3 configures the bit as input or output. The field also controls whether the bit is enabled as an external interrupt source and selects the output as open-drain or push-pull.

Figure 44. Port 2/3 D Mode Register, R251 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | W/O | W/O | W/O | W/O | W/O | W/O | W/O | W/O |

The Port 2/3 A Mode, Port 2/3 B Mode, Port 2/3 C Mode and Port 2/3 D Mode registers control the modes of Ports 2 and 3. A separate 2-bit field for each of the bits of Ports 2 and 3 configures the bit as input or output. The field also controls whether the bit is enabled as an external interrupt source and selects the output as open-drain or push-pull.

Figure 45. Port 2/3 A Interrupt Pending Register (P2AIP), R252 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|----|----|----|----|----|----|----|----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | ? | ? | ? | ? | ? | ? | ? | ? |

Read Only (writeable for reset puposes)

The Port 2/3 A Interrupt Pending and Port 2/3 B Interrupt Pending registers represent the software interface to the negative edge-triggered flip-flops associated with external interrupt inputs. Each bit of these registers corresponds to an interrupt generated by an external source. When one of these registers is read, the value of each bit represents the state of the corresponding interrupt. When one of these registers is written to, a 1 in a bit position causes the corresponding edge-triggered flip-flop to be reset to 0. A 0 causes no action.

The software interfaces with these registers to poll the interrupts and also to reset pending interrupts as they are processed. Figure 45 shows the pin relationship.

Figure 46. Port 2/3 B Interrupt Pending Register (P2BIP), R253 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|----|----|----|----|----|----|----|----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | ? | ? | ? | ? | ? | ? | ? | ? |

Read Only (writeable for reset puposes)

The Port 2/3 A Interrupt Pending and Port 2/3 B Interrupt Pending registers represent the software interface to the negative edge-triggered flip-flops associated with external interrupt inputs. Each bit of these registers corresponds to an interrupt generated by an external source. When one of these registers is read, the value of each bit represents the state of the corresponding interrupt. When one of these registers is written to, a 1 in a bit position causes the corresponding edge-triggered flip-flop to be reset to 0. A 0 causes no action.

The software interfaces with these registers to poll the interrupts and also to reset pending interrupts as they are processed. Figure 46 shows the pin relationship.

Figure 47. External Memory Timing Register, R254 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

This register controls all the extended bus timing features.

D0 - DMA Select - If 0, DMA uses register file space. If 1, it uses Data Memory.

D1 - Stack Select - If 0, stack is located in register file space. If 1, it is located in Data Memory.

Figure 48. Interrupt Priority Register (IPR), R255 Bank 0

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Value | X | X | X | X | X | X | X | X |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

The Interrupt Priority register defines the priority order of the interrupt levels. Interrupts should be globally disabled before writing to this register.

D0 - Group A - 0=IRQ0 > IRQ1; 1=IRQ1 > IRQ0.

D2 - Group B - 0=IRQ2>(IRQ3,IRQ4); 1=(IRQ3,IRQ4) > IRQ2.

D3 - Subgroup B - 0=IRQ3>IRQ4; 1=IRQ4>IRQ3.

D5 - Group C - 0=IRQ5>(IRQ6,IRQ7); 1=(IRQ6,IRQ7)>IRQ5.

D6 - Subgroup C - 0=IRQ6>IRQ7; 1=IRQ7>IRQ6.

Instruction Summary

This section provides a summary of the IA88C00 instructions.

NOTE

Assignment of a value is indicated by the symbol “←”.

For example:

$Dst \leftarrow dst + src$

indicates that the source data is added to the destination data and the result is stored in the destination location.

The notation “addr (n) ” is used to refer to bit (n) of a given operand location.

For example:

dst (7)

refers to bit 7 of the destination operand.

Figure 49. Instruction Summary

| Instruction and Operation | Address Mode dst src | | Opcode Byte (Hex) | Flags Affected | | | | | |
|--|-------------------------|----|-------------------|----------------|---|---|---|---|---|
| | | | | C | Z | S | V | D | H |
| ADC dst, src $dst \leftarrow dst + src + C$ | † | | 1[] | * | * | * | - | 0 | * |
| ADD dst, src $dst \leftarrow dst + src$ | † | | 0[] | * | * | * | * | 0 | * |
| ADD dst, src $dst \leftarrow dst \text{ AND } src$ | † | | 5[] | - | * | * | 0 | - | - |
| BAND dst, src $dst \leftarrow dst \text{ AND } src$ | r0 | Rb | 67 | - | * | 0 | U | - | - |
| | Rb | r0 | 67 | | | | | | |
| BCP dst, src $dst - src$ | r0 | Rb | 17 | - | * | 0 | U | - | - |
| BITC dst $dst \leftarrow \text{NOT } dst$ | rb | | 57 | - | * | 0 | U | - | - |
| BITR dst $dst \leftarrow 0$ | rb | 77 | - | - | - | - | - | - | - |

| Instruction and Operation | Address Mode | dst scr | Opcode Byte (Hex) | Flags Affected | | | | | |
|----------------------------|--------------|---------|-------------------|----------------|---|---|---|---|---|
| | | | | C | Z | S | V | D | H |
| BITS dst dst←0 dst←1 | rb | 77 | - | - | - | - | - | - | - |

| Instruction and Operation | Address Mode | dst scr | Opcode Byte (Hex) | Flags Affected | | | | | |
|---|--------------|---------|-------------------|----------------|---|---|---|---|---|
| | | | | C | Z | S | V | D | H |
| BOR dst, src dst←0 OR src | r0 | rB | 07 | - | * | 0 | U | - | - |
| BTJRF dst←0 | RA | Rb | 37 | - | - | - | - | - | - |
| if src=0, PC=PC+dst BTJRT | RA | rb | 37 | - | - | - | - | - | - |
| IF SRC=0, PC=PC+dst BXOR dst, src dst←dst XOR src | r0 | Rb | 27 | - | * | 0 | U | - | - |
| CALL dst SP←SP - 2 @SP←PC, PC←dst | DA | | F6 | - | - | - | - | - | - |
| CCF | IRR | | F4 | | | | | | |
| C←NOT C | IA | | D4 | | | | | | |
| CLR dst dst←0 | | | EF | * | - | - | - | - | - |
| COM dst dst←NOT dst | R | | B0 | - | - | - | - | - | - |
| CP dst, src | IR | | B1 | - | * | * | 0 | - | - |
| Dst - src | R | | 60 | - | * | * | 0 | - | - |
| CPIJE | IR | | 61 | * | * | * | * | - | - |
| if dst - src=0, then PC←PC+RA Ir←Ir + 1 | † | | A[] | * | * | * | * | - | - |
| CPIJNE | R | Ir | C2 | - | - | - | - | - | - |
| if dst - src=0, then PC←PC+RA Ir←Ir + 1 | r | Ir | D2 | - | - | - | - | - | - |
| DA dst dst←DA dst | R | | 40 | * | * | * | U | - | - |
| DEC dst dst←dst - 1 | IR | | 41 | - | * | * | * | - | - |
| | R | | 00 | - | * | * | * | - | - |
| | IR | | 01 | | | | | | |

| | | | | | | | | | |
|--------------|----|----|----|---|---|---|---|---|---|
| DECW dst | RR | | 80 | - | * | * | * | - | - |
| dst←dst - 1 | IR | | 81 | | | | | | |
| DI | | | 8F | - | - | - | - | - | - |
| SMR(0)←0 | | | | | | | | | |
| DIV dst, src | | | | | | | | | |
| dst÷src | RR | R | 94 | * | * | * | * | - | - |
| dst (Upper)← | RR | IR | 95 | | | | | | |
| Quotient | | | | | | | | | |
| dst (Lower)← | RR | IM | 96 | | | | | | |
| Remainder | | | | | | | | | |

| Instruction and Operation | Address Mode dst src | | Opcode Byte (Hex) | Flags Affected | | | | | |
|------------------------------|----------------------------|---|----------------------|-------------------|---|---|----|---|------------------------------------|
| | | | | C | Z | S | V | D | H |
| DJNZ r, dst | RA | r | rA | - | - | - | - | - | - |
| r←r - 1 | | | (r=0 IoF) | | | | | | |
| If r = 0 | | | | | | | | | |
| PC←PC + dst | | | | | | | | | |
| EI | | | 9F | - | - | - | - | - | - |
| SMR(0) | | | | | | | | | |
| ENTER | | | 1F | - | - | - | - | - | - |
| SP←SP - 2 | | | | | | | | | |
| @ SP←IP | | | | | | | | | |
| IP←PC | | | | | | | | | |
| PC←@ IP | | | | | | | | | |
| IP←IP + 2 | | | | | | | | | |
| EXIT | | | 2F | - | - | - | - | - | - |
| IP←@SP | | | | | | | | | |
| SP←SP + 2 | | | | | | | | | |
| PC←@ IP | | | | | | | | | |
| IP←IP + 2 | | | | | | | | | |
| INC dst | r | | rE | - | * | * | * | - | - |
| dst←dst + 1 | | | r=0-F | | | | | | |
| | R | | 20 | | | | | | |
| | IR | | 21 | | | | | | |
| INCW dst | RR | | A0 | - | * | * | * | - | - |
| dst←dst + 1 | IR | | A1 | | | | | | |
| IRET (Fast) | | | | | | | | | |
| PC↔IP | | | | | | | BF | | |
| FLAG←FLAG | | | | | | | | | |
| FIS←0 | | | | | | | | | |
| | | | | | | | | | Restored to before interrupt |

IRET (Normal) BF Restored to
before
interrupt
 FLAGS←@SP;

SP←SP + 1;
 PC←@ SP
 SP←SP + 2;
 SMR(0) ←1

| | | | | | | | | | |
|---------------------------------------|---------------|-------------------------|---|---|---|---|---|---|---|
| JP cc, dst if cc is true PC←dst | DA IRR | ccD C = 0 to F 30 | - | - | - | - | - | - | - |
|---------------------------------------|---------------|-------------------------|---|---|---|---|---|---|---|

| | | | | | | | | | |
|---|----|--------------------|---|---|---|---|---|---|---|
| JR cc, dst if cc is true, PC←PC + d | RA | ccB cc = 0 to F | - | - | - | - | - | - | - |
|---|----|--------------------|---|---|---|---|---|---|---|

| | | | | | | | | | |
|------------------------|-------------|---------|------------------------------|---|---|---|---|---|---|
| LD dst, src dst←src | r r R | IM R | rC r8 r9 r = 0 to F | - | - | - | - | - | - |
|------------------------|-------------|---------|------------------------------|---|---|---|---|---|---|

| Instruction and Operation | Address Mode | Opcode Byte (Hex) | Flags Affected | C | Z | S | V | D | H |
|------------------------------|-----------------|----------------------|-------------------|---|---|---|---|---|---|
|------------------------------|-----------------|----------------------|-------------------|---|---|---|---|---|---|

| | | | | | | | | | |
|--|----|----|----|--|--|--|--|--|---|
| | r | IR | C7 | | | | | | |
| | IR | r | D7 | | | | | | |
| | R | R | E4 | | | | | | |
| | R | IR | E5 | | | | | | |
| | R | IM | E6 | | | | | | - |
| | IR | IM | D6 | | | | | | |
| | IR | R | F6 | | | | | | |
| | r | x | 87 | | | | | | - |
| | x | r | 97 | | | | | | |

| | | | | | | | | | |
|-------------------------|----------|----------|----------|---|---|---|---|---|---|
| LDB dst, src dst←src | r0 Rb | Rb r0 | 47 47 | - | - | - | - | - | - |
|-------------------------|----------|----------|----------|---|---|---|---|---|---|

| | | | | | | | | | |
|--------------------|---|--------------------------------------|--|---|---|---|---|---|---|
| LDC/LDE dst←src | r lrr r xs r x1 r DA | lrr r xs r x1 DA R | C3 D3 E7 F7 A7 B7 A7 B7 | - | - | - | - | - | - |
|--------------------|---|--------------------------------------|--|---|---|---|---|---|---|

| | | | | | | | | | |
|--|---|-----|----|---|---|---|---|---|---|
| LDCD/LDED dst, src dst←src rr←rr-1 | r | lrr | E2 | - | - | - | - | - | - |
|--|---|-----|----|---|---|---|---|---|---|

| | | | | | | | | | |
|--|---|-----|----|---|---|---|---|---|---|
| LDEI/LDCI dst, src dst←src rr←rr+1 | r | lrr | E3 | - | - | - | - | - | - |
|--|---|-----|----|---|---|---|---|---|---|

| | | | | | | | | | |
|---------------------|---|-----|----|---|---|---|---|---|---|
| LDCPD/LDCI dst, src | r | lrr | E3 | - | - | - | - | - | - |
|---------------------|---|-----|----|---|---|---|---|---|---|

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dst←src
rr←rr+1

| | | | | | | | | | |
|--|----|-----|------|---|---|---|---|---|---|
| LDCPI/LDEPI dst, src dst←src rr←rr+1 | r | lrr | E3 | - | - | - | - | - | - |
| LDW dst, src | RR | RR | C4 | - | - | - | - | - | - |
| | RR | IR | C5 | | | | | | |
| | RR | IMM | C6 | | | | | | |
| MULT dst, src | RR | R | 84 | * | 0 | * | * | - | - |
| | RR | IR | 85 | | | | | | |
| | RR | IM | 86 | | | | | | |
| NEXT PC←@ IP IP←IP + 2 | | | 0F | - | - | - | - | - | - |
| NOP | | | FF | - | - | - | - | - | - |
| OR dst, src dst←dst OR src | † | | 4[] | - | * | * | 0 | - | - |
| POP dst dst←@SP; SP←SP + 1 | | R | 50 | - | - | - | - | - | - |
| | | IR | 51 | | | | | | |
| POPUD dst, src dst←src IR←IR - 1 | R | IR | 92 | - | - | - | - | - | - |
| POPUI dst, src dst←src IR←IR + 1 | R | IR | 93 | - | - | - | - | - | - |

| Instruction and Operation | Address Mode dst scr | | Opcode Byte (Hex) | Flags Affected | | | | | |
|---|----------------------------|----|----------------------|-------------------|---|---|---|---|---|
| | | | | C | Z | S | V | D | H |
| PUSH scr SP←SP - 1; @SP←src | R | IR | 70 71 | - | - | - | - | - | - |
| PUSHUD dst, src IR←IR - 1 dst←src | IR | R | 82 | - | - | - | - | - | - |
| PUSHUI dst, src IR←IR + 1 dst←src | IR | R | 83 | - | - | - | - | - | - |
| RCF C←0 | | | CF | 0 | - | - | - | - | - |
| RET PC←@SP;SP←SP+2 | | | AF | - | - | - | - | - | - |
| RL dst C←dst(7) dst(0)←dst(7) | R | IR | 90 91 | * | * | * | * | - | - |

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| | | | | | | | | | |
|--|----|----|------|---|---|---|---|---|---|
| dst(N+1)←dst(N) N=0 to 6 | | | | | | | | | |
| RLC dst | R | | 10 | * | * | * | * | - | - |
| dst(0)←C | IR | | 11 | | | | | | |
| C←dst(7) | | | | | | | | | |
| dst(N)←dst(N+1) N=0 to 6 | | | | | | | | | |
| RR dst | R | | C0 | * | * | * | * | - | - |
| C←dst(0) | IR | | C1 | | | | | | |
| dst(7)←C | | | | | | | | | |
| dst(N)←dst(N+1) N=0 to 6 | | | | | | | | | |
| SB0 | | | 4F | - | - | - | - | - | - |
| BANK←0 | | | | | | | | | |
| SB1 | | | 5F | | | | | | |
| BANK←1 | | | | | | | | | |
| SBC dst, src | † | | 3[] | * | * | * | * | 1 | * |
| dst←dst - src - C | | | | | | | | | |
| SCF | | | DF | 1 | - | - | - | - | - |
| C←1 | | | | | | | | | |
| SRA dst | R | | D0 | * | * | * | 0 | - | - |
| dst(7)←dst(7) C←dst(0) dst(N)←dst(N+1) N=0 to 6 | | | | | | | | | |
| SRP src | | IM | 31 | - | - | - | - | - | - |
| RP0←IM RP1←IM+8 | | | | | | | | | |
| SRP0 | | IM | 31 | - | - | - | - | - | - |
| RP0←IM | | | | | | | | | |
| SRP1 | | IM | 31 | - | - | - | - | - | - |
| RP1←IM | | | | | | | | | |
| STOP | | | 6F | - | - | - | - | - | - |
| SUB dst, src | † | | 2[] | * | * | * | * | 1 | * |
| dst←dst - src | | | | | | | | | |
| SWAP dst | R | | F0 | - | * | * | U | - | - |
| Dst(0-3)↔dst(4-7) | IR | | F1 | | | | | | |
| TCM dst, src | † | | 6[] | - | * | * | 0 | - | - |
| (NOT dst) AND src | | | | | | | | | |
| TM dst, src | † | | 7[] | - | * | * | 0 | - | - |
| dst AMD src | | | | | | | | | |
| TSW dst, src | R | R | 7F | U | * | * | 0 | U | U |
| WFI | | | 3F | - | - | - | - | - | - |
| XOR dst, src | † | | B[] | - | * | * | 0 | - | - |

dst←dst
XOR src

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[]' in this table. Its value is found in the following table to the left of the applicable addressing mode pair.

For example, the opcode of an ADC instruction using the addressing modes r (destination) and ir (source) is 13.

| Address dst | Mode src | Lower Opcode Nibble |
|-------------|----------|---------------------|
| r | r | [2] |
| r | Ir | [3] |
| R | R | [4] |
| R | IR | [5] |
| R | IM | [6] |

Notes:

0 = Cleared to Zero

1 = Set to One

– = Unaffected

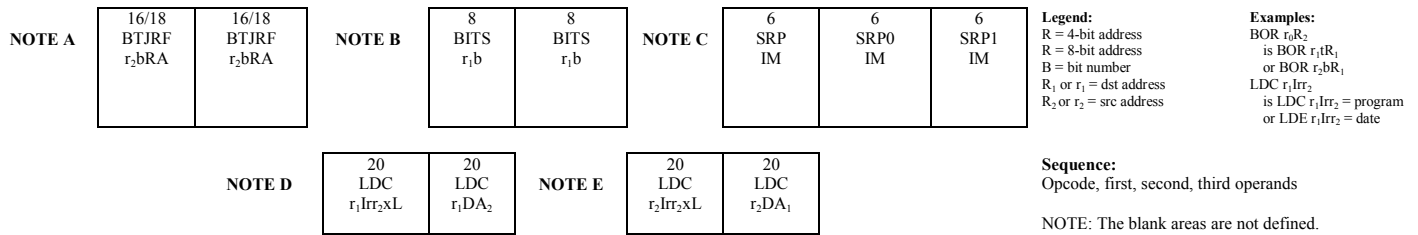
* = Set or reset, depending on result of operation.

U = Undefined

Opcode Map

Figure 50. Opcode Map

| Lower Nibble (Hex) | | | | | | | | | | | | | | | | |
|--------------------|---------------------------------|----------------------------------|---|--|--|---|---|---|--|--|------------------------------------|---------------------|------------------------------|---------------------|----------------------------|-----------------|
| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
| 0 | 6 DEC R ₁ | 6 DEC R ₂ | 6 ADD r ₁ r ₂ | 6 ADD r ₁ Ir ₂ | 10 ADD R ₂ R ₁ | 10 ADD IR ₂ R ₁ | 10 ADD R ₁ IM | 10 BOR r ₀ R _b | 6 LD r ₁ R ₂ | 6 LD R ₂ R ₁ | 12/10 DJNZ r ₁ RA | 12/10 JR CcRA | 6 LD r ₁ IM | 12/10 JP CcDA | 6 INC r ₁ | 14 NEXT |
| 1 | 6 RLC R ₁ | 6 RLC IR ₁ | 6 ADC r ₁ r ₂ | 6 ADC r ₁ Ir ₂ | 10 ADC R ₂ R ₁ | 10 ADC IR ₂ R ₁ | 10 ADC R ₁ IM | 10 BCP R ₁ b R ₂ | | | | | | | | 20 NEXT |
| 2 | 6 INC R ₁ | 6 INC IR ₁ | 6 SUB r ₁ r ₂ | 6 SUB r ₁ Ir ₂ | 10 SUB R ₂ R ₁ | 10 SUB IR ₂ R ₁ | 10 SUB R ₁ IM | 10 BXOR* r ₀ R _b | | | | | | | | 22 EXIT |
| 3 | 10 JP IRR ₁ | NOTE C | 6 SBC r ₁ r ₂ | 6 SBC r ₁ Ir ₂ | 10 SBC R ₂ R ₁ | 10 SBC IR ₂ R ₁ | 10 SBC R ₁ IM | NOTE A | | | | | | | | 6 WFI |
| 4 | 6 DA R ₁ | 6 DA IR ₁ | 6 OR r ₁ r ₂ | 6 OR r ₁ Ir ₂ | 10 OR R ₂ R ₁ | 10 OR R ₂ R ₁ | 10 OR R ₁ IM | 10 LDB* r ₀ R _b | | | | | | | | 6 SBO |
| 5 | 10 POP R ₁ | 6 POP IR ₁ | 6 AND r ₁ r ₂ | 6 AND r ₁ Ir ₂ | 10 AND R ₂ R ₁ | 10 AND IR ₂ R ₁ | 10 AND R ₁ IM | 8 BITC r ₁ b | | | | | | | | 6 SBI |
| 6 | 6 COM R ₁ | 6 COM IR ₁ | 6 TCM r ₁ r ₂ | 6 TCM r ₁ Ir ₂ | 10 TCM R ₂ R ₁ | 10 TCM IR ₂ R ₁ | 10 TCM R ₁ IM | 10 BAND* r ₀ R _b | | | | | | | | 6 STOP |
| 7 | 10/12 PUSH R ₂ | 10/14 PUSH IR ₂ | 6 TM r ₁ r ₂ | 6 TM r ₁ Ir ₂ | 10 TM R ₂ R ₁ | 10 TM IR ₂ R ₁ | 10 TM R ₁ IM | NOTE B | | | | | | | | 10 TSW RR |
| 8 | 10 DECW RR ₁ | 10 DECW IR ₁ | 10 PUSHUD IR ₁ R ₂ | 10 PUSHUI IR ₁ R ₂ | 24 MULT R ₂ RR ₁ | 24 MULT R ₂ RR ₁ | 24 MULT IM ₂ RR ₁ | 10 LD r ₁ xr ₂ | | | | | | | | 6 DI |
| 9 | 6 RL R ₁ | 6 RL IR ₁ | 10 POPUD IR ₂ R ₁ | 10 POPUI IR ₁ R ₂ | 28/12 DIV R ₂ RR ₁ | 28/12 DIV iR ₂ RR ₁ | 28/12 DIV IMRR ₁ | 10 LD r ₁ xr ₁ | | | | | | | | 6 EI |
| A | 10 INCW RR ₁ | 10 INCW IR ₁ | 6 CP r ₁ r ₂ | 6 CP r ₁ Ir ₂ | 10 CP R ₂ R ₁ | 10 CP IR ₂ R ₁ | 10 CP R ₁ IM | NOTE D | | | | | | | | 14 RET |
| B | 6 CLR R ₁ | 6 CLR IR ₁ | 6 XOR r ₁ r ₂ | 6 XOR r ₁ Ir ₂ | 10 XOR R ₂ R ₁ | 10 XOR IR ₂ R ₁ | 10 XOR R ₁ IM | NOTE E | | | | | | | | 16/6 IRET |
| C | 6 RRC R ₁ | 6 RRC IR ₁ | 16/18 CPIJE Ir ₁ r ₂ RA | 12 LDC* r ₂ Ir ₁ | 10 LDW RR ₂ RR ₁ | 10 LDW IR ₂ RR ₁ | 12 LDW RR ₁ IML | 6 LD r ₁ Ir ₂ | | | | | | | | 6 RCF |
| D | 6 SRA R ₁ | 6 SRA IR ₁ | 16 CPIJNE Ir ₁ r ₂ RA | 12 LDC* r ₂ Ir ₁ | 20 CALL IA ₁ | | 10 LD IR ₁ IM | 6 LD Ir ₁ r ₂ | | | | | | | | 6 SCF |
| E | 6 RR R ₁ | 6 RR IR ₁ | 16 LDCD* r ₁ Ir ₂ | 16 LDCD* r ₁ Ir ₂ | 10 LD R ₂ R ₁ | 10 LD IR ₂ R ₁ | 10 LD R ₁ IM | 18 LDC* r ₁ Ir ₂ XS | | | | | | | | 6 CCF |
| F | 8 SWAP R ₁ | 8 SWAP IR ₁ | 16 LDCPD* r ₂ Ir ₁ | 16 LDCPI* r ₂ Ir ₁ | 18 CALL IRR ₁ | 10 LD R ₂ IR ₁ | 18 CALL DA ₁ | 18 LDC* r ₂ Ir ₁ XS | | | | | | | | 6 NOP |
| | | | | | | | | | ⬇ | ⬇ | ⬇ | ⬇ | ⬇ | ⬇ | ⬇ | |



Instructions

Figure 51. Load Instructions

| Mnemonic | Operands | Instructions |
|----------|----------|--|
| CLR | dst | Clear |
| LD | dst, src | Load |
| LDB | dst, src | Load bit |
| LDC | dst, src | Load program memory |
| LDE | dst, src | Load data memory |
| LDCD | dst, src | Load program memory and decrement |
| LDED | dst, src | Load data memory and decrement |
| LDCI | dst, src | Load program memory and increment |
| LDEI | dst, src | Load data memory and increment |
| LDCPD | dst, src | Load program memory with pre-decrement |
| LDEPD | dst, src | Load data memory with pre-decrement |
| LDCPI | dst, src | Load program memory with pre-increment |
| LDEPI | dst, src | Load data memory with pre-increment |
| LDW | dst, src | Load word |
| POP | dst | Pop stack |
| POPUD | dst, src | Pop user stack (decrement) |
| POPUI | dst, src | Pop user stack (increment) |
| PUSH | src | Push stack |
| PUSHUD | dst, src | Push user stack (decrement) |
| PUSHUI | dst, src | Push user stack (increment) |

Figure 52. Arithmetic Instructions

| Mnemonic | Operands | Instructions |
|----------|----------|----------------|
| ADC | dst, src | Add with carry |
| ADD | dst, src | Add |
| CP | dst, src | Compare |
| DA | dst | Decimal adjust |
| DEC | dst | Decrement |
| DECW | dst | Decrement word |
| DIV | dst, src | Divide |
| INC | dst | Increment |

| | | |
|------|----------|---------------------|
| INCW | dst | Increment word |
| MULT | dst, src | Multiply |
| SBC | dst, src | Subtract with carry |
| SUB | dst, src | Subtract |

Figure 53. Logical Instructions

| Mnemonic | Operands | Instructions |
|----------|----------|-------------------|
| AND | dst, src | Logical AND |
| COM | dst | Complement |
| OR | dst, src | Logical OR |
| XOR | dst, src | Logical exclusive |

Figure 54. Program Control Instructions

| Mnemonic | Operands | Instructions |
|----------|----------|--|
| BTJRT | dst, src | Bit test jump relative on True |
| BTJRF | dst, src | Bit test jump relative on False |
| CALL | dst | Call procedure |
| CPIJE | dst, src | Compare, increment and jump on equal |
| CPIJNE | dst, src | Compare, increment and jump on non-equal |
| DJNE | r, dst | Decrement and jump on non-zero |
| ENTER | | Enter |
| EXIT | | Exit |
| IRET | | Return from interrupt |
| JP | cc, dst | Jump on condition code |
| JP | dst | Jump unconditional |
| JR | cc, dst | Jump relative on condition code |
| JR | dst | Jump relative unconditional |
| NEXT | | Next |
| RET | | Return |
| WFI | | Wait for interrupt |

Figure 55. Bit Manipulation Instructions

| Mnemonic | Operands | Instructions |
|----------|------------|----------------------------|
| BAND | dst, src | Bit AND |
| BCP | dst, src | Bit compare |
| BITC | dst | Bit complement |
| BITR | dst | Bit reset |
| BITS | dst | Bit set |
| BOR | dst, src | Bit OR |
| BXOR | dst, src | Bit exclusive OR |
| TCM | dst, src | Test complement under mask |
| TM | dst, src | Test under mask |
| TSW | src1, src2 | Test Word |

Figure 56. Rotate and Shift Instructions

| Mnemonic | Operands | Instructions |
|----------|----------|----------------------------|
| RL | dst | Rotate left |
| RLC | dst | Rotate left through carry |
| RR | dst | Rotate right |
| RRC | dst | Rotate right through carry |
| SWAP | dst | Swap nibbles |

Figure 57. CPU Control Instructions

| Mnemonic | Operands | Instructions |
|----------|----------|---------------------------|
| CCF | | Complement carry flag |
| DI | | Disable interrupts |
| EI | | Enable interrupts |
| NOP | | Do nothing |
| RCF | | Reset carry flag |
| SBO | | Set bank flag |
| SB1 | | Set bank 1 |
| SCF | | Set carry flag |
| SRP | src | Set register pointers |
| SRP0 | src | Set register pointer zero |
| SRP1 | src | Set register pointer one |
| STOP | | Enable STOP Mode |

Interrupts

The IA88C00 supports as many as 27 interrupt sources. Interrupt sources are sorted into 8 different priority levels. These levels are controlled by the interrupt Priority Register (IPR). Enabling and masking of individual interrupts is controlled by the System Mode Register (R222).

The various sources, vectors and levels of the interrupt structure are depicted in Figure 58 in this section.

| <u>INTERRUPT SOURCES</u> | <u>POLLING</u> | <u>VECTORS</u> | <u>LEVELS</u> |
|---------------------------------------|----------------|----------------|---------------|
| COUNTER 0 ZERO COUNT | | 12 | IRQ2 |
| EXTERNAL INTERRUPT (P2 ₆) | | | |
| EXTERNAL INTERRUPT (P2 ₇) | | | |
| COUNTER 1 ZERO COUNT | | 14 | IRQ5 |
| EXTERNAL INTERRUPT (P3 ₆) | | | |
| EXTERNAL INTERRUPT (P3 ₇) | | | |
| HANDSHAKE CHANNEL 0 | | 28 | IRQ4 |
| EXTERNAL INTERRUPT (P2 ₄) | | | |
| EXTERNAL INTERRUPT (P2 ₅) | | | |
| HANDSHAKE CHANNEL 1 | | 30 | IRQ7 |
| EXTERNAL INTERRUPT (P3 ₄) | | | |
| EXTERNAL INTERRUPT (P3 ₅) | | | |
| RESERVED | | 0 | |
| | | 2 | |
| RESERVED | | 4 | IRQ3 |
| | | 6 | |
| EXTERNAL INTERRUPT (P3 ₂) | | | |
| EXTERNAL INTERRUPT (P2 ₂) | | | |
| | | 8 | |
| EXTERNAL INTERRUPT (P3 ₂) | | 10 | IRQ0 |
| EXTERNAL INTERRUPT (P2 ₂) | | | |
| UART RECEIVE OVERRUN | | 16 | |
| UART FRAMING ERROR | | | |
| UART PARITY ERROR | | | |
| UART WAKEUP DETECT | | 18 | |
| UART BREAK DETECT | | | |
| UART CONTROL CHAR DETECT | | | IRQ6 |
| UART RECEIVE DATA | | 20 | |
| EXTERNAL INTERRUPT (P3 ₀) | | | |
| | | 22 | |
| EXTERNAL INTERRUPT (P2 ₀) | | | |
| UART ZERO COUNT | | 24 | |
| EXTERNAL INTERRUPT (P2 ₁) | | | IRQ1 |
| UART TRANSMIT DATA | | 26 | |
| EXTERNAL INTERRUPT (P3 ₁) | | | |

Figure 58. Interrupt Levels and Vectors

Interrupt Programming Model

The IA88C00 maintains program compatibility with the Super8. Enabling or disabling of interrupts are controlled via the following registers:

Interrupt enable/disable. See the System Mode register (R222).

Level enable. See the interrupt Mask register (R221).

Level priority. See the Interrupt Priority register (R255, Bank 0).

Source enable/disable. Interrupt sources are enabled or disabled in the individual source's Mode and Control register.

Functional Overview

For an interrupt to be serviced, it's source must be enabled. The corresponding interrupt and level must likewise be enabled. Each interrupt input is conditioned with edge-triggered devices to convert all interrupt inputs to "levels". This eliminates the requirement for external hardware to maintain the interrupt input prior to servicing.

When an interrupt source is received the processor is "vectored" to the vector address associated with the interrupt. In the fact of multiple interrupts, the enabled interrupt whose level has the highest priority is serviced first. For interrupts within the same level, the priority of the individual interrupt takes precedence.

Upon servicing the interrupt, the processor clears the Interrupt Enable bit in the System Mode register to prevent a high priority interrupt from disrupting the service routine. The program counter and status flags are pushed onto the stack and the program counter is loaded with the appropriate interrupt vector and the interrupt service routine (ISR) begins to execute. Upon completion, the ISR executes an RET instruction. The flags and program counter are popped off the stack and the Interrupt Enable bit in the System Mode register is set.

The IA88C00 supports a special mode of "fast" interrupt processing. Utilization of this mode requires program intervention. The vector address of the ISR must be loaded into the instruction pointer and the Fast Interrupt enable bit in the System Mode Register must be set. Upon receipt of the interrupt source, the ISR vector is loaded into the program counter while the old value of the program counter is saved in the Instruction Pointer. Status flags are saved in the FLAGS register and the Fast interrupt Status Bit in FLAGS is set. Upon completion of the ISR, the process is reversed.

Stack Operation

The IA88C00 maintains program model compatibility on all Stack operations. The stack may be maintained in either the register file or in data memory space. For programming model details see registers R216/R217 (the stack pointer) and register R254 (Memory Timing register)

The IA88C00 also supports user-defined stacks. These stacks are accessed via the PUSHUI, POPUD, LDEI and LDEPD instructions.

Counter/Timers

The IA88C00 provides two identical 16 bit timer/counters with an 8-bit prescaler. The counters are driven from a divide-by-4 clock derived from the oscillator. Each count provides robust functionality including:

- Up or down count
- Single or continuous count
- Output pulse train with variable duty cycle
- Input capture
- External gating/triggering

For longer events, the counters may be cascaded to form a 32-bit counter. For program model details see registers R224 through R230.

DMA

The IA88C00 supports high speed data transfer support for the UART and handshake channel 0 via Direct Memory Access (DMA). Data can be transferred between these peripherals and contiguous locations in either the register file or external data memory. For details on the programming model see registers R235 (UART transmit control) R236 (UART receive control), R244 (Handshake Channel 0 Control) and R240/241, Bank 1 (DMA Count).

WDT

The IA88C00 provides a “Watchdog” (WDT) timer to provide sanity checks on the processor. Should program execution hang, the WDT timeout will expire and the RESET pin will be held active for 5 ms. The WDT is prevented from timing out by periodically writing a “1” to bit D5 in the WDT/SMR register.

The WDT clock is derived from either an internal ring oscillator or from the crystal oscillator input. It should be noted that the frequency of the internal oscillator and associated WDT time-out can vary widely (as much as 3 times) with voltage and temperature. For details on the WDT programming model see register R230 (WDT/SMR register).

Stop Mode

When a STOP instruction is executed, the process enter Stop Mode. During Stop mode, the system clock and external oscillator are disabled. Stop Mode is exited via a hard reset, or by applying an edge to a pre-defined bit of either Port 2, 3, or 4. For details on the Stop Mode programming model see register R230 (WDT/SMR register).

Halt Mode

When the IA88C00 execute the Wait for Interrupt (WFI) instruction and bit 3 of R223 (Halt Mode register) is cleared, the processor enters HALT mode. The internal CPU clock is disabled, however, the oscillator remains active. Use of the UART, timers and DMA remains under user control. The Halt mode is exited via an interrupt or DMA request. The programming model for Halt Mode is detailed in R223 (Halt Mode register)

I/O Ports

The IA88C00 contains 40 I/O lines arranged into five 8-bit ports. Each line is TTL-compatible and can be configured as a address/data line. Each port includes an input register, an output register and a register address. The input register stores data coming into the port. The output register stores data to be written to a port. Reading a port's register address returns the value in the input register. Writing a port's register address loads the value in the output register. If the port is configured for an output, this value will appear on the external pins.

When the CPU reads the bits configured as outputs, the data on the external pins is returned. Under normal output loading, this has the same effect as reading the output register, unless the bits are configured as open-drain outputs.

The ports can be configured as shown in Figure 59.

Figure 59. Port Configuration

| Port | Configuration Choices |
|-------|---|
| 0 | High address and/or 0 |
| 1 | Multiplexed Low address/data or data only |
| 2 & 3 | Control I/O for UART, handshake channels, counter/timers, general I/O and external interrupts |
| 4 | Low address or general I/O |

Port 0

Port 0 can be assigned on a bit-by-bit basis as either general I/O or as address bits for external memory. The bits configured as I/O can be either all inputs or all outputs, they cannot be mixed. If configured for outputs, they can be either push-pull or open-drain types. I/O direction is controlled by mode control register R241. Push-pull or open-drain selection is controlled by mode control register R241.

Port 0 can be placed under handshake control handshake channel 1.
Any bits configured as I/O can be accessed via R208.

Port 0 bits configured as address outputs cannot be accessed via the register, and initially the four lower bits are configured as addresses eight through twelve.

Port 1

Port 1 is bi-directional. Port 1 is configured as either a byte wide Mux'ed Address(low byte)/Data bus or as Data bus only. This control is via the demux pin. The port address for Port 1 is R209. Port 1 drive characteristics can be selected to be either Push/Pull or Open Drain. This control is via the mode/control register R241 Bank0, ControlRegR241B0

Port 2 and 3

Ports 2 and 3 provide external control inputs and outputs for the UART, handshake channels and counter/timers. The pin assignments appear in Figure 60. Bits not used for control I/O can be configured as general purpose I/O lines and/or external interrupt inputs.

Those bits configured for general I/O can be configured individually for input or output. Those configured for output can be individually configured for (1) input or output and (2) open drain or push pull output.

Figure 60. Pin Assignments for Port 2 and 3

| Port 2 Bit Function | Port 3 Bit Function |
|--------------------------------------|--------------------------------------|
| 0 UART receive clock | 0 UART receive clock |
| 1 UART transmit | 1 UART transmit |
| 2 Reserved | 2 Reserved |
| 3 Reserved | 3 Reserved |
| 4 Handshake 0 input | 4 Handshake 1 input/WAIT |
| 5 Handshake 0 output | 5 Handshake 1 output/DM |
| 6 Counter 0 input | 6 Counter 1 input |
| 7 Counter 0 I/O | 7 Counter 1 I/O |

Port 4

Port 4 can be assigned as general I/O or as the lower address byte in de-mux mode. As general I/O, each bit can be configured individually as input or output, with either push-pull or open-drain outputs. I/O directions is controlled by mode control reg R246. Push-pull or open_drain selection is controlled by mode control reg R247. All Port 4 inputs are Schmitt-triggered. Port 4 can be placed under handshake control handshake channel 0. Port 4 register address is R212.

UART

The UART is a full-duplex asynchronous channel. It transmits and receives independently at 5 to 8 bits per character and contains options for even- or odd-bit parity and a wake-up feature.

Data can be read into or out of the UART via R239, Bank 0. This single address is able to serve a full-duplex channel because it contains two complete 8-bit registers, one for the transmitter and the other for the receiver. The programming model for the UART is outlined in R235 (UART Transmit Control), R236 (UART Receive Control), R237 (UART Interrupt Enable), R238 (Transmit Interrupt Register) R248/249 bank 1 (UART Baud Rate Generator), R250/251 bank 1 (UART Mode A/B Registers).

Pins

The UART uses the following Port 2 and 3 pins:

Figure 61. Port 2 and 3 Pins

| Port/Pin | UART Function |
|----------|----------------|
| 2/0 | Receive Clock |
| 3/0 | Receive Data |
| 2/1 | Transmit Clock |
| 3/1 | Transmit Data |

Transmitter

Data is output on the UART when the UART's register is specified as the destination (dst) of an operation. This automatically adds the start bit, the programmed parity bit and the programmed number of stop bits. It can also add a wake-up bit if that option is selected.

The extra bits in R239 are ignored if the UART is programmed to a 5-, 6-, or 7-bit character.

Depending on the programmed data rate, serial data is transmitted at a rate equal to 1, 1/16, 1/32 or 1/64 of the transmitter clock rate. All data is sent out on the falling edge of the clock input.

When the UART has no data to send, it holds the output marking (High). It can be programmed with the Send Break command to hold the output marking Low (Spacing). This output marking continues until the command is cleared.

Receiver

The UART begins receive operation when Receive Enable (URC, bit 0) is set to High. After this, a Low on the receive input pin for longer than half a bit time is interpreted as a start bit. The UART samples the data on the input pin in the middle of each clock cycle until a complete byte is assembled. This completed byte is placed in the Receive Data register.

If the 1X clock mode is selected, external bit synchronization must be provided, and the input data is sampled on the rising edge of the clock.

For character lengths of less than eight bits, the UART inserts 1s into the unused bits. And if parity is enabled, the parity bit is not stripped. The data bits, extra 1s and the parity bits are placed in the UART Data register (UIO).

While the UART is assembling a byte in its input shift register, the CPU has time to service an interrupt and manipulate the data character in UIO.

Once the complete character is assembled, the UART checks it and performs the following actions:

1. Sets the Control Character status bit, if it is an ASCII control character.
2. Checks the wake-up settings and completes any indicated action.
3. Checks to see if the calculated parity matches the programmed parity bit, if parity is enabled. If they do not match, it sets the parity Error bit in URC (R236, Bank 0), which remains set until reset by software.
4. Resets the Framing Error bit (URC, bit 4), if the character is assembled without any stop bits. This bit remains set until cleared by software.

Overrun errors occur when characters are received faster than they are read. That is, when the UART has assembled a complete character before the CPU has read current character, the UART sets the Overrun Error bit (URC, bit 3), and the character currently in the receive buffer is lost.

The overrun bit remains set until cleared by software.

Address Space

The IA88C00 can access 64 Kbytes of program memory and 64 Kbytes of data memory. These spaces can be either combined or separate. If separate, they are controlled by the DM line (Port P35), which selects data memory when Low and program memory when High.

CPU Program Memory

Program memory occupies address 0 to 64K. External program memory is accessed by configuring Ports 0 and/or 1 and/or 4 as the memory interface.

The address/data lines are controlled by AS, DS and R/W.

The first 32 program memory bytes are reserved for interrupt vectors. The lowest address available for user programs is 32 (decimal). This value is automatically loaded into the program counter after a hardware reset. Port 0 can be configured to provide from 0 to 8 additional address lines. Port 1 is used as an 8-bit multiplexed address/data port or as a data port when in de-mux mode.

CPU Data Memory

If separated from program memory by the DM optional output, the external CPU data memory space can be mapped anywhere from 0 to 64K (full 16-bit address space). Data memory uses the same address/data bit (Port 1) and additional address (chosen from Port 0) as program memory. The DM pin (P35) is mainly what distinguishes data memory from program memory. It is also distinguished by the fact that data memory can begin at address 0000H.

Figure 62 shows the system memory space.

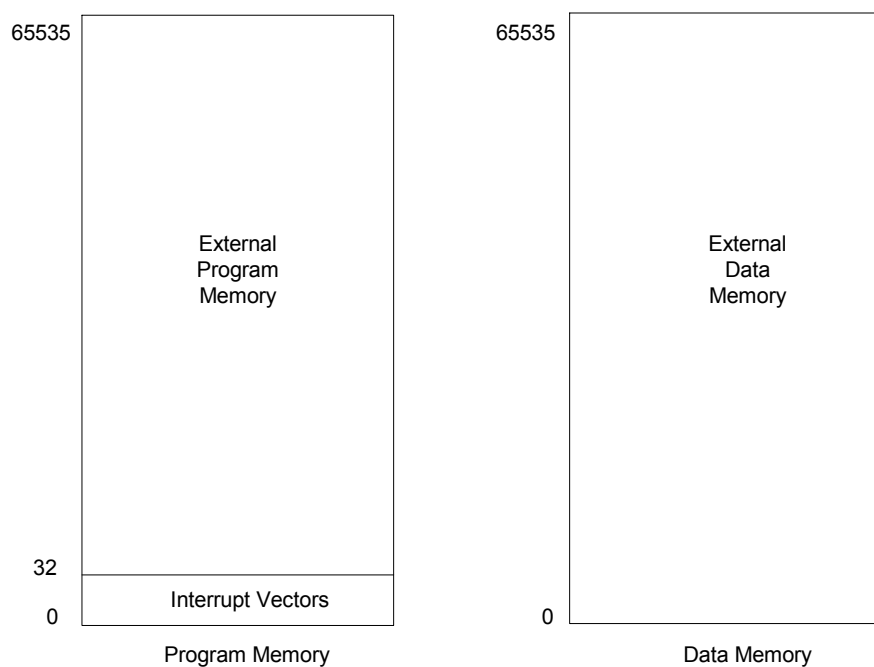


Figure 62. Program and Data Memory Address Space

Absolute Maximum Ratings

| Symbol | Description | Min | Max | Unit |
|------------------|-------------------|------|------|------|
| V _{DO} | Supply Voltage* | -0.3 | +7.0 | V |
| T _{STG} | Storage Temp | -65 | +150 | C |
| T _A | Oper Ambient Temp | † | † | C |

* Voltages on all pins with respect to GND

† See Ordering Information

CAUTION

Stress that exceeds that presented above may cause permanent damage to the device. This is a stress rating only. Acceptable operation of the device at any condition above that which is indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Standard Test Conditions

The following characteristics apply to standard test conditions as noted. All voltages are referenced to V_{SS}. Positive current flows into the referenced pin (Standard Test Load).

Standard conditions are:

4.5V < V_{CC} < 5.5V

GND – OV

-40°C < T_A < + 85°C

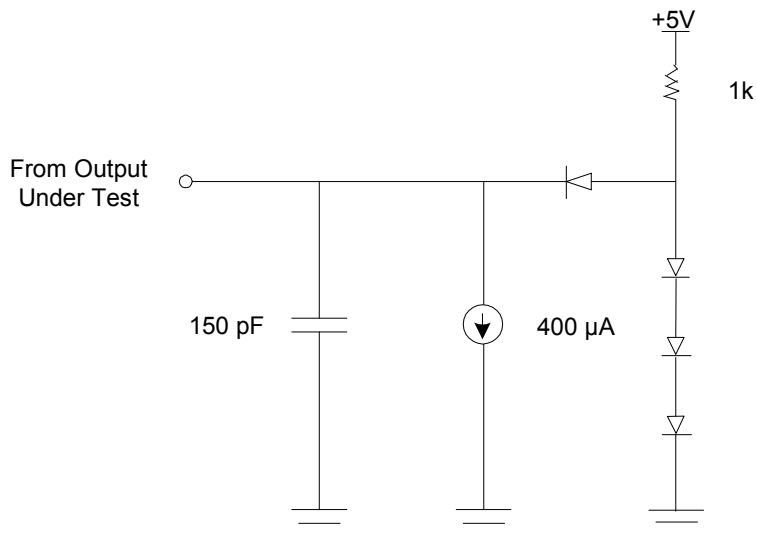


Figure 63. Standard Test Load

DC Characteristics

| Symbol | Parameter | Min | Max | Unit | Condition |
|------------------|--------------------------------|------|-----------------|---------|------------------------------------|
| V _{CH} | Clock Input High Voltage | 3.5 | V _{CC} | V | Driven by External Clock Generator |
| V _{CL} | Clock Input Low Voltage | -0.3 | 1.5 | V | Driven by External Clock Generator |
| V _{IH} | Input High Voltage | 2.2 | V _{CC} | V | |
| V _{IL} | Input Low Voltage | -0.3 | 0.8 | V | |
| V _{RH} | Reset Input High Voltage | 3.8 | V _{CC} | V | |
| V _{RL} | Reset Input Low Voltage | -0.3 | 0.8 | V | |
| V _{OH} | Output High Voltage | 3.5 | | V | I _{OH} = -400 μ A |
| V _{OL} | Output Low Voltage | | 0.4 | V | I _{OL} = +400 mA |
| V _{IL} | Input Leakage | -10 | 10 | μ A | |
| I _{OL} | Output Leakage | -10 | 10 | μ A | |
| I _{IR} | Reset Input Current | | -50 | μ A | |
| I _{CC} | V _{CC} Supply Current | | 90 | mA | [1] |
| I _{CC1} | Standby Current | | 5 | mA | @ 20 MHz [2] |
| | | | 10 | mA | @ 30 MHz [2] |
| I _{CC2} | Standby Current | | 20 | μ A | [3] |

NOTES

Following are estimated values:

1. In this case all outputs and I/O pins are floating.
2. Estimated Values, not tested. HALT mode is invoked with UART CT0 and CT1 deactivated with all input pins tied to V_{CC} or V_{SS}.
3. Estimated Values, not tested. STOP mode is invoked with all input pins tied to V_{CC} or V_{SS}.

AC Electrical Characteristics

Figure 64. External I/O or Memory Read and Write Timing

| Number | Symbol | Parameter |
|--------|------------|--|
| 1 | TdA(AS) | Address valid to /AS Rise Delay |
| 2 | ThAS(A) | /AS Rise to Address Valid |
| 3 | TdAS(DI) | /AS Rise to Data in Required Valid Delay |
| 4 | TwAS | /AS Low Width |
| 5 | TdAZ (DSR) | Address Float to /DS (Read) |
| 6 | TwDSR | /DS (Read) Low Width |
| 7 | TwDSW | /DS (Write) Low Width |
| 8 | TdDSR (DI) | /DS (Read) to Data |
| 9 | ThDSR (DI) | /DS Rise (Read) to Data in Hold Time |
| 10 | TdDS (A) | /DS Rise to Address Active Delay |
| 11 | TdDA (AS) | /DS Rise to /AS Delay |
| 12 | TdR/W (AS) | R/W to AS Rise Delay |
| 13 | TdDS (R/W) | DS Rise to R/W Valid Delay |
| 14 | TdDO (DSW) | Data Out to /DS (Write) Delay |
| 15 | ThDSW (DO) | /DS Rise (Write) to Data Out Hold Time |
| 16 | TdA (DI) | Address to Data In Required Valid Delay |
| 17 | TdAS (DSR) | /AS Rise to D/S (Read) Delay |
| 18 | TsDI (DSR) | Data in Setup Time to DS Rise (Read) |
| 19 | TdDM (AS) | /DM to /AS Rise Delay |
| 20 | TdDS (DM) | /DS Rise to /DM Valid Delay |
| 21 | ThDS (A) | /DS Rise to Address Valid Hold Time |
| 22 | TwW | Wait Width (One Wait) Window |
| 23 | TdAS (W) | /AS Rise to Wait Delay |

Figure 65. 20 MHz Timing

| No. | Symbol | Normal Min | Max | Extended Min | Max |
|-----|------------|---------------|-----|-----------------|-----|
| 1 | TdA (AS) | 25 | | 70 | |
| 2 | ThAS (A) | 25 | | 70 | |
| 3 | TdAS (DI) | | 180 | | 375 |
| 4 | TwAS | 35 | | 85 | |
| 5 | TdAZ (DSR) | 0 | | 0 | |
| 6 | TwDSR | 140 | | 285 | |
| 7 | TwDSW | 85 | | 185 | |
| 8 | TdDSR (DI) | | 115 | | 260 |
| 9 | ThDSR (DI) | 0 | | 0 | |
| 10 | TdDS (A) | 25 | | 25 | |
| 11 | TdDS (AS) | 20 | | 65 | |
| 12 | TdR/W (AS) | 25 | | 70 | |
| 13 | TdDS (R/W) | 20 | | 65 | |
| 14 | TdDO (DSW) | 30 | | 70 | |
| 15 | ThDSW (DO) | 20 | | 65 | |
| 16 | TdA (DI) | | 205 | | 445 |
| 17 | TdAS (DSR) | 25 | | 70 | |
| 18 | TsDI (DSR) | 25 | | 65 | |
| 19 | TdDM (AS) | 20 | | 65 | |
| 20 | TdDS (DM) | 20 | | 65 | |
| 21 | ThDS (A) | 20 | | 65 | |

Figure 66. 12 MHz Timing

| No. | Symbol | Normal Min | Max | Extended Min | Max |
|------------|---------------|-----------------------|------------|-------------------------|------------|
| 1 | TdA (AS) | 55 | | 135 | |
| 2 | ThAS (A) | 55 | | 135 | |
| 3 | TdAS (DI) | | 305 | | 630 |
| 4 | TwAS | 70 | | 150 | |
| 5 | TdAZ (DSR) | 0 | | 0 | |
| 6 | TwDSR | 240 | | 480 | |
| 7 | TwDSW | 150 | | 320 | |
| 8 | TdDSR (DI) | | 215 | | 440 |
| 9 | ThDSR (DI) | 0 | | 0 | |
| 10 | TdDS (A) | 55 | | 130 | |
| 11 | TdDS (AS) | 45 | | 125 | |
| 12 | TdR/W (AS) | 55 | | 135 | |
| 13 | TdDS (R/W) | 45 | | 125 | |
| 14 | TdDO (DSW) | 65 | | 150 | |
| 15 | ThDSW (DO) | 45 | | 125 | |
| 16 | TdA (DI) | | 365 | | 770 |
| 17 | TdAS (DSR) | 55 | | 135 | |
| 18 | TsDI (DSR) | 25 | | 25 | |
| 19 | TdDM (AS) | 50 | | 130 | |
| 20 | TdDS (DM) | 45 | | 125 | |
| 21 | ThDS (A) | 45 | | 125 | |

Figure 67. 25 MHz Timing

| No. | Symbol | Normal Min | Max | Extended Min | Max |
|-----|------------|---------------|-----|-----------------|-----|
| 1 | TdA (AS) | 15 | | 50 | |
| 2 | ThAS (A) | 15 | | 50 | |
| 3 | TdAS (DI) | | 140 | | 280 |
| 4 | TwAS | 26 | | 65 | |
| 5 | TdAZ (DSR) | 0 | | | 0 |
| 6 | TwDSR | 110 | | 220 | |
| 7 | TwDSW | 65 | | 142 | |
| 8 | TdDSR (DI) | | 85 | | 195 |
| 9 | ThDSR (DI) | 0 | | 0 | |
| 10 | TdDS (A) | 20 | | 55 | |
| 11 | TdDS (AS) | 15 | | 50 | |
| 12 | TdR/W (AS) | 15 | | 50 | |
| 13 | TdDS (R/W) | 15 | | 50 | |
| 14 | TdDO (DSW) | 20 | | 50 | |
| 15 | ThDSW (DO) | 15 | | 50 | |
| 16 | TdA (DI) | | 155 | | 330 |
| 17 | TdAS (DSR) | 15 | | 50 | |
| 18 | TsDI (DSR) | 25 | | 25 | |
| 19 | TdDM (AS) | 10 | | 45 | |
| 20 | TdDS (DM) | 15 | | 50 | |
| 21 | ThDS (A) | 15 | | 50 | |

Input Handshake Timing

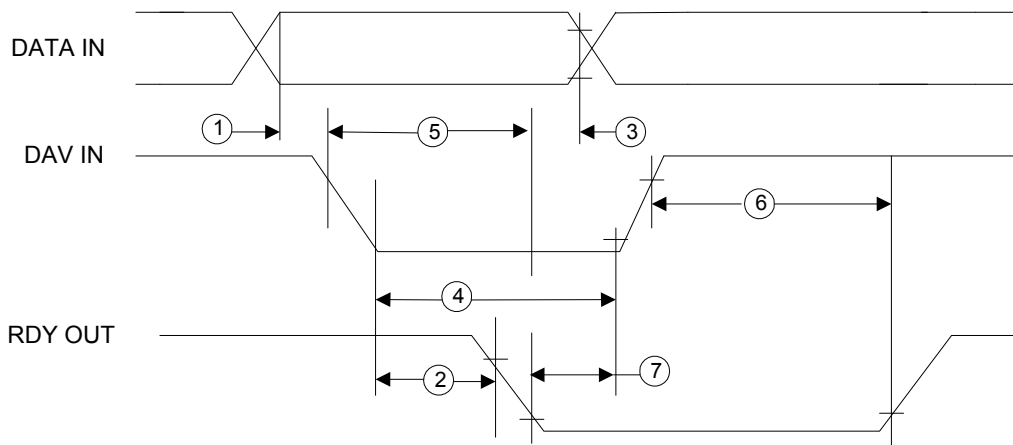


Figure 68. Fully Interlocked Mode (Input Handshake)

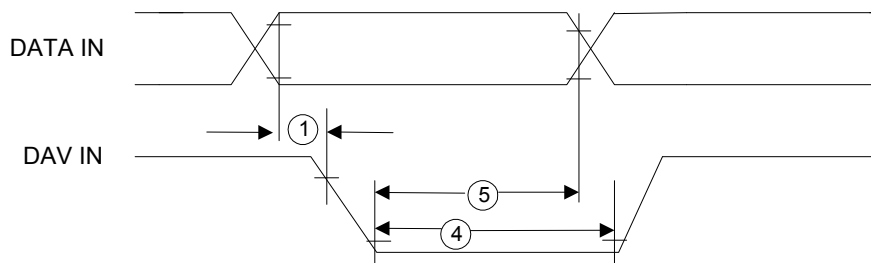


Figure 69. Strobed Mode (Input Handshake)

AC Electrical Characteristics

Input Handshake

| No. | Symbol | Parameter | Min | Max | Notes*† |
|-----|--------------|------------------------------------|-----|-----|---------|
| 1 | TsDI(DAV) | Data In to Setup Time | 0 | | |
| 2 | TdDAVlf(RDY) | /DAV Fall Input to RDY Fall Delay | | 200 | 1 |
| 3 | ThDI(RDY) | Data In Hold Time from RDY Fall | 0 | | |
| 4 | TwDAV | /DAV In Width | 45 | | |
| 5 | ThD(DAV) | Data In Hold Time from /DAV Fall | 130 | | |
| 6 | TdDAV(RDY) | /DAV Rise Input to RDY Rise Delay | | 100 | 2 |
| 7 | TdRDYf(DAV) | RDY Rise Output to /DAV Rise Delay | 0 | | |

NOTES

1. Standard Test Load
2. This time assumes user program reads data before /DAV Input goes High. RDY will not go high before data is read.
- * Times are given in nanoseconds.
- † Times are preliminary and subject to change.

Output Handshake Timing

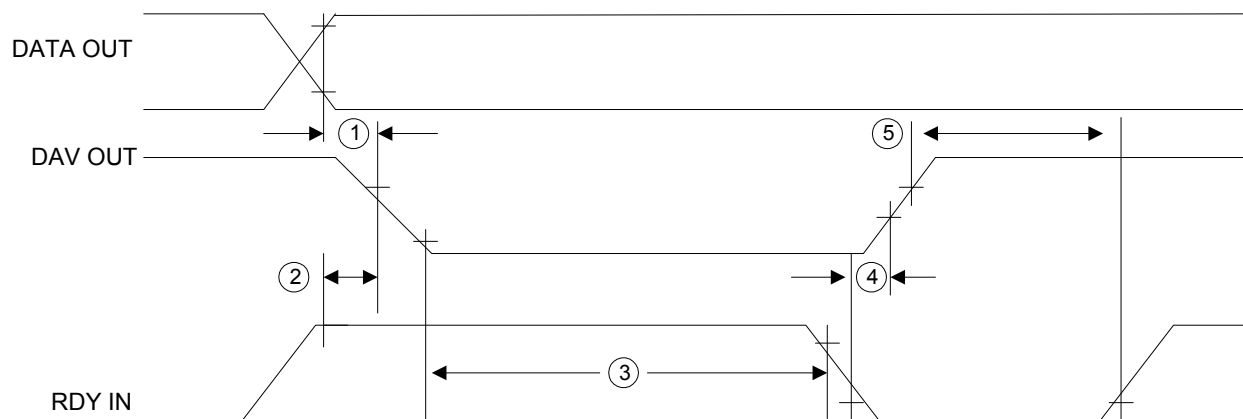


Figure 70. Fully Interlocked Mode (Output Handshake)

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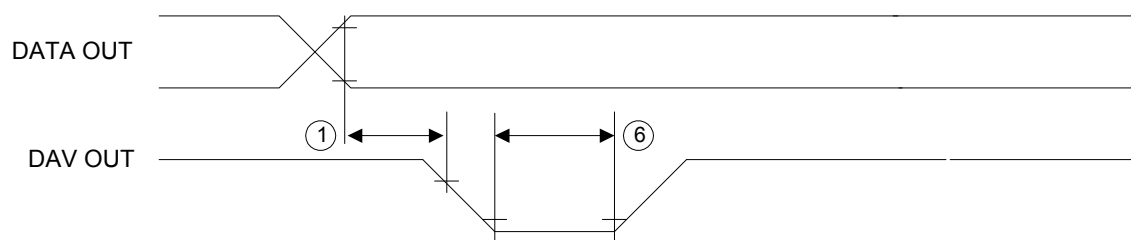


Figure 71. Strobed Mode (Output Handshake)

AC Electrical Characteristics (12 MHz, 20 MHz)

Output Handshake

| No. | Symbol | Parameter | Min | Max | Notes*† |
|-----|--------------|------------------------------------|-----|-----|---------|
| 1 | TdDO(DAV) | Data Out to /DAV Fall Delay | 90 | | 1, 2 |
| 2 | TdRDYr(DAV) | RDY Rise Input to /DAV Fall Delay | | 110 | 1 |
| 3 | ThDAV(RDY) | /DAV Fall Output to RDY Fall Delay | 0 | | |
| 4 | TdRDY(DAV) | /RDY Fall Input to /DAV Rise Delay | 0 | 110 | 1 |
| 5 | TdDAVOr(RDY) | /DAV Rise Output to RDY Rise Delay | 0 | | |
| 6 | TwDAVO | /DAV Output Width | 150 | | 2 |

Notes:

1. Standard Test Load
2. Time given is for zero value in Deskew Counter. For non-zero value of n where n = 1,2, ...15 add 2 x n x TpC to the given time.
- † Times given are in nanoseconds.
- * Times are preliminary and subject to change.

ERPOM Read Timing

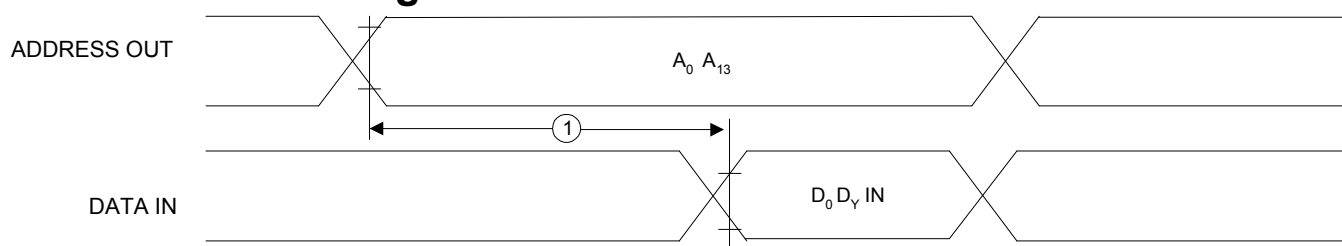


Figure 72. EPROM READ Timing

AC Electrical Characteristics (20 MHz)

EPROM Read Cycle

| No. | Symbol | Parameter | Min | Max | Notes†* |
|-----|---------|---|-----|-----|---------|
| 1 | TdA(DR) | Address Valid to Read Data Required Valid | | 170 | 1 |

NOTES

1. WAIT states add 167 ns to these times.
- † All times are in nanoseconds and are for 12 MHz input frequency.
- * Timings are preliminary and subject to change.

Wait Timing

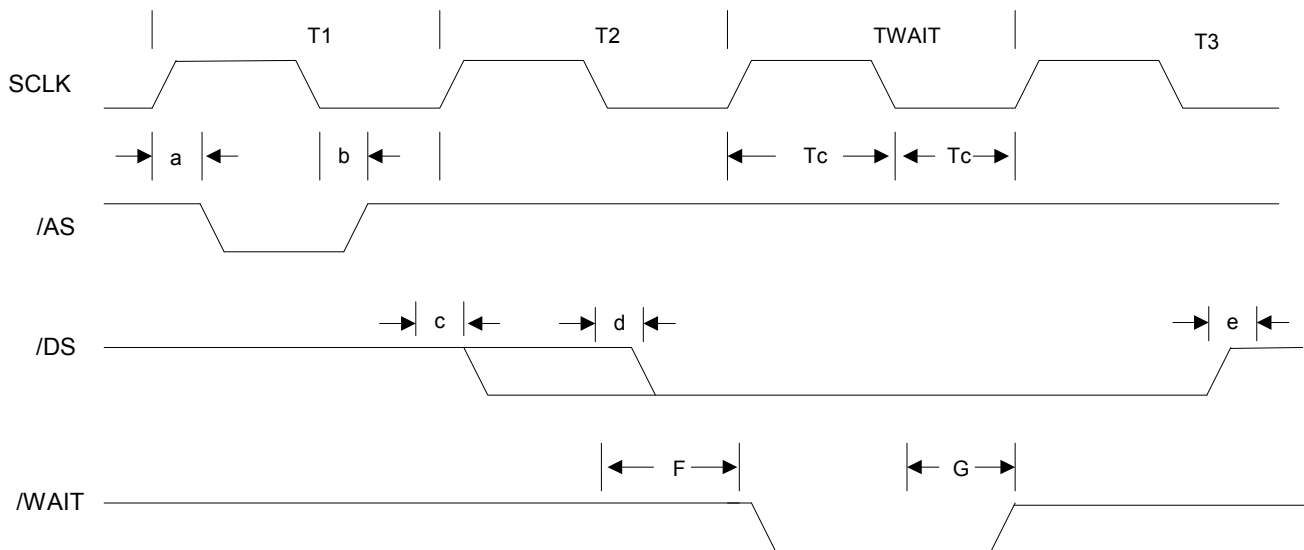


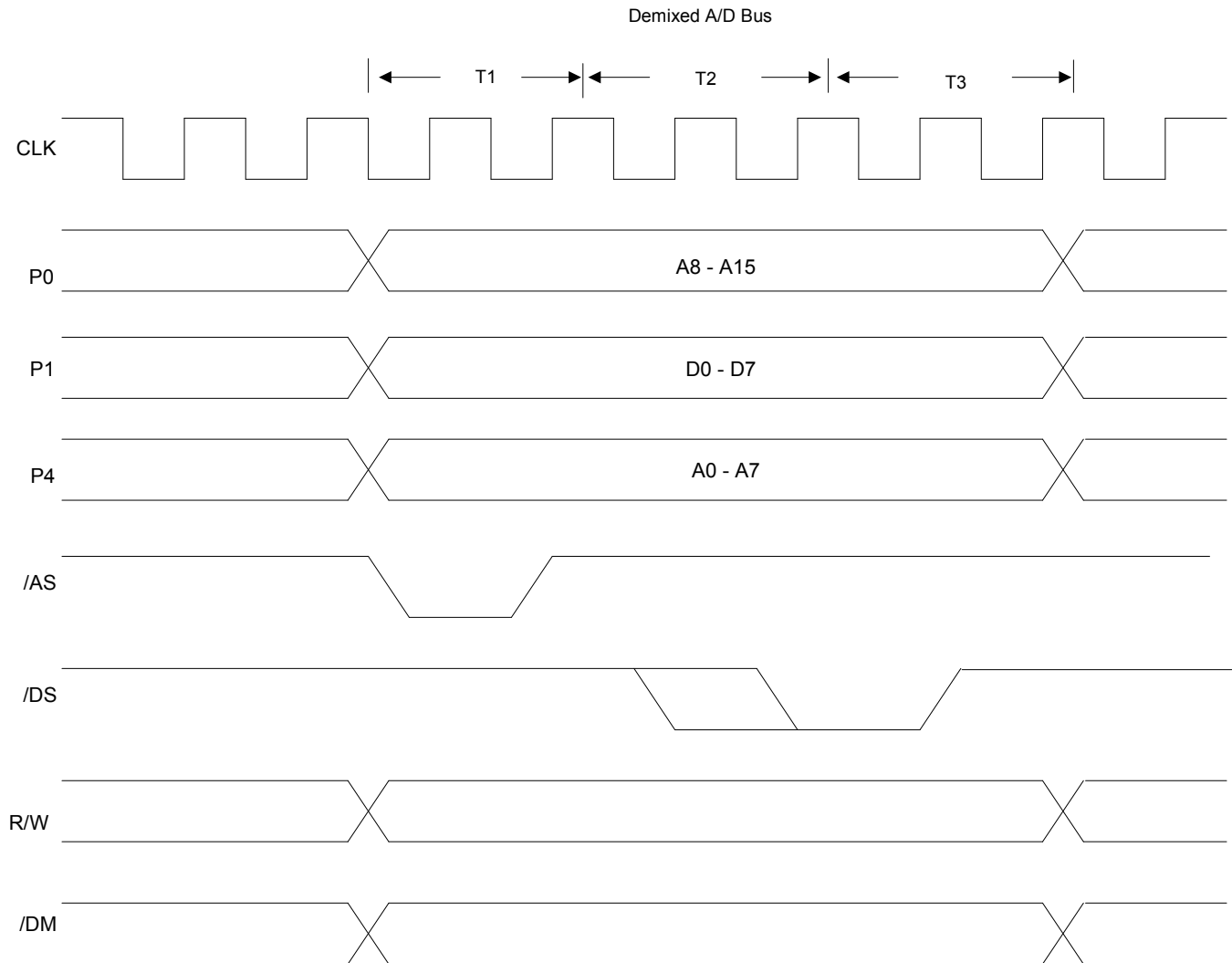
Figure 73. Wait Timing

| | Description | | |
|---|---|------|-----|
| a | Skew of T1 SCLK Rise to /AS Fall | 10.0 | Max |
| b | Skew of T1 SCLK Rise to /AS Rise | 10.0 | Max |
| c | Skew of T2 SCLK Rise to Read /DS Fall | 20.0 | Max |
| d | Skew T2 SCLK Fall to Write /DS Fall | 20.0 | Max |
| e | Skew T3 SCLK Fall to /DS Rise | 20.0 | Max |
| F | /WAIT Fall Delay After T2 SCLK Fall to Generate at Least 1 WAIT State | 20.0 | Max |
| G | /WAIT Fall Delay after T2 SCLK Fall to Prevent an Additional WAIT State | 15.0 | Max |

NOTES

All figures are in nanoseconds.

De-Multiplexed Bus Timing



NOTES

/AS, /DS, R/W, /DM Timing remains unchanged in demuxed A/D bus mode.

Package Information

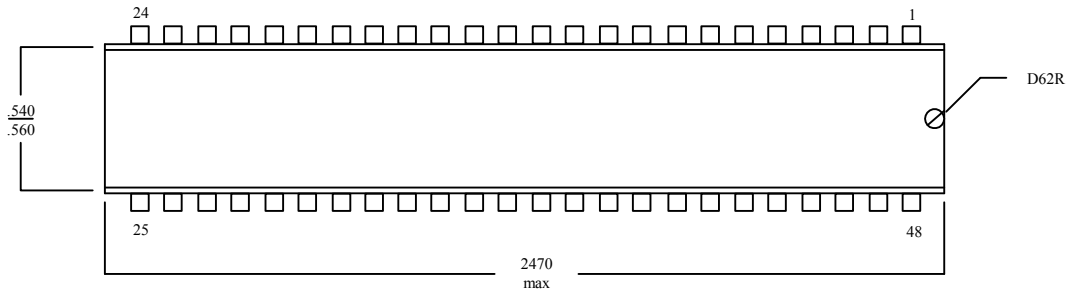


Figure 74. 48-Lead Aerial View

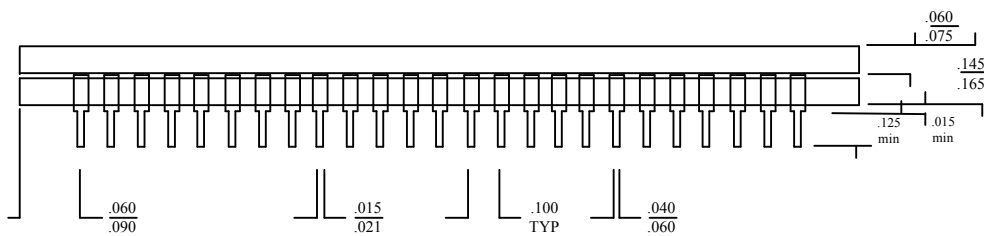


Figure 75. 48-Lead Side View

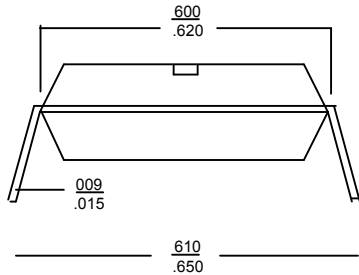


Figure 76. 48-Lead End View

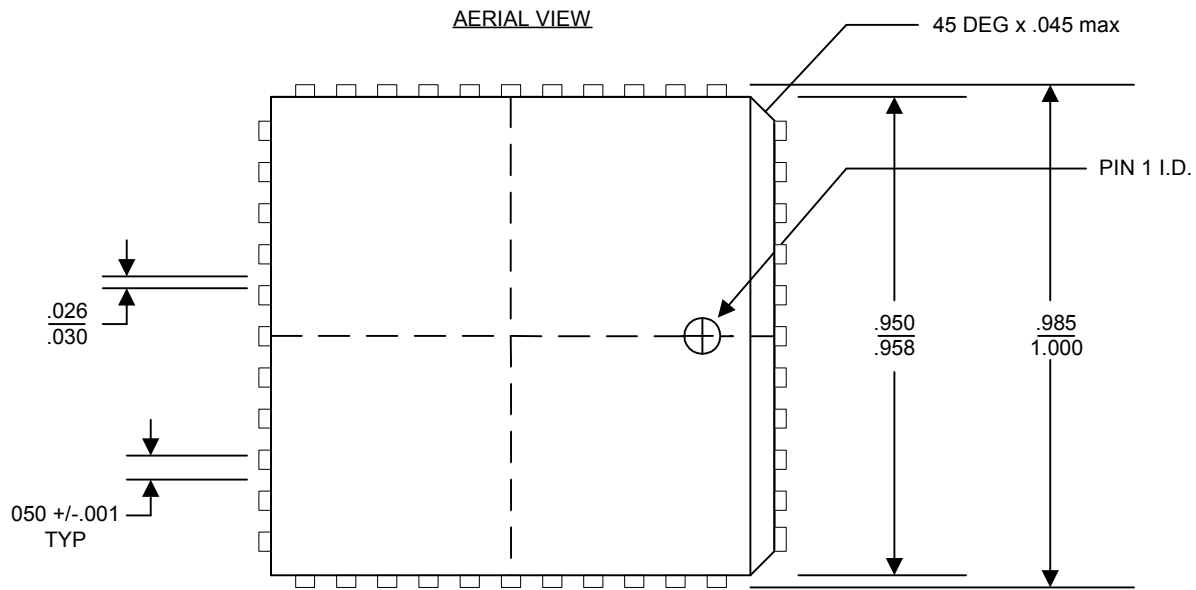


Figure 77. 68-Lead Package Aerial View

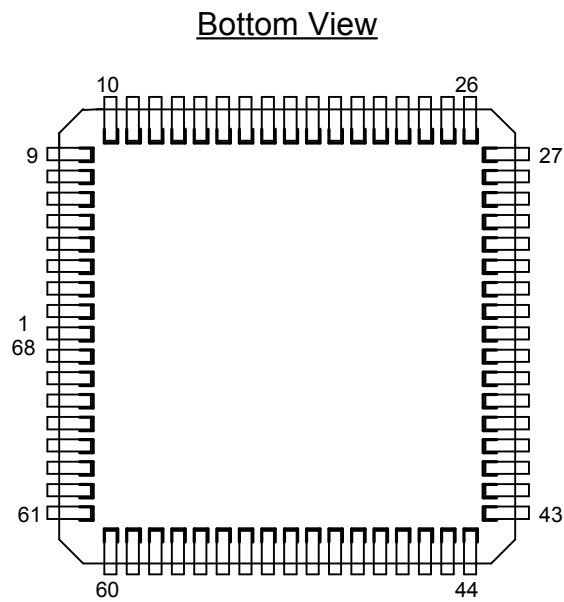


Figure 78. 68-Lead Package Bottom View

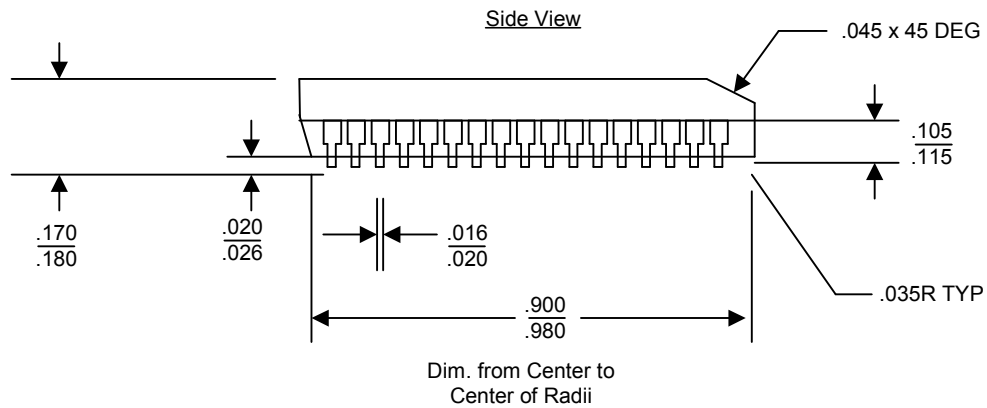


Figure 79. 68-Lead Package Side View

Ordering Information

| <u>Innovasic</u> <u>Semiconductor</u>[®] Part Number | Package Type | Temperature Grades |
|--|---|--|
| IA88C00-PDW48C (standard packaging) IA88C00-PDW48I (standard packaging) IA88C00-PDW48C-R (RoHS packaging) IA88C00-PDW48I-R (RoHS packaging) | 48-Pin Plastic Dual In-line Package (DIP) | Commercial Industrial Commercial Industrial |
| IA88C00-PLC68C (standard packaging) IA88C00-PLC68I (standard packaging) IA88C00-PLC68C-R (RoHS packaging) IA88C00-PLC68I-R (RoHS packaging) | 68-Pin Plastic Leaded Chip Carrier (PLCC) | Commercial Industrial Commercial Industrial |