

### Features

- 32 standard frequencies from 25 MHz to 322.265625 MHz
- LVPECL, LVDS and HCSL output signaling
- 0.1 ps RMS phase jitter (random) for Ethernet applications
- Contact [SiTime](#) for  $\pm 10$  ppm frequency stability
- Wide temperature range from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$   
Contact [SiTime](#) for higher temperature range options
- Industry-standard packages: 3.2 x 2.5, 7.0 x 5.0 mm  
Contact [SiTime](#) for 5.0 x 3.2 mm package

### Applications

- 10/40/100 GB Ethernet, SONET, SATA, SAS, Fibre Channel
- Telecom, networking, instrumentation, storage, servers



### Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over temperature and rated operating voltage with standard output termination show in the termination diagrams. Typical values are at  $25^{\circ}\text{C}$  and nominal supply voltage.

**Table 1. Electrical Characteristics – Common to LVPECL, LVDS and HCSL**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Frequency Range</b>						
Output Frequency Range	f	32 standard frequencies between 25 MHz and 322.265625 MHz			MHz	Refer to <a href="#">Table 10</a> for the list of supported frequencies
<b>Frequency Stability</b>						
Frequency Stability	F_stab	-10	–	+10	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage and load variations. Contact <a href="#">SiTime</a> for $\pm 10$ ppm
		-20	–	+20	ppm	
		-25	–	+25	ppm	
		-50	–	+50	ppm	
First Year Aging	F_1y	–	$\pm 1$	–	ppm	At $25^{\circ}\text{C}$
<b>Temperature Range</b>						
Operating Temperature Range	T_use	-20	–	+70	$^{\circ}\text{C}$	Extended Commercial
		-40	–	+85	$^{\circ}\text{C}$	Industrial. Contact <a href="#">SiTime</a> for higher temperature range options
<b>Supply Voltage</b>						
Supply Voltage	Vdd	2.97	3.30	3.63	V	
		2.70	3.00	3.30	V	
		2.52	2.80	3.08	V	
		2.25	2.50	2.75	V	
<b>Input Characteristics</b>						
Input Voltage High	V <sub>IH</sub>	70%	–	–	Vdd	Pin 1, OE
Input Voltage Low	V <sub>IL</sub>	–	–	30%	Vdd	Pin 1, OE
Input Pull-up Impedance	Z <sub>in</sub>	–	100	–	k $\Omega$	Pin 1, OE logic high or logic low
<b>Output Characteristics</b>						
Duty Cycle	DC	45	–	55	%	
<b>Startup and OE Timing</b>						
Startup Time	T <sub>start</sub>	–	–	3.0	ms	Measured from the time Vdd reaches its rated minimum value.
OE Enable/Disable Time	T <sub>oe</sub>	–	–	3.8	$\mu\text{s}$	f = 156.25 MHz.

Table 2. Electrical Characteristics – LVPECL

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
Current Consumption	I <sub>dd</sub>	–	–	89	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3V or 2.5V
OE Disable Supply Current	I <sub>OE</sub>	–	–	58	mA	OE = Low
Output Disable Leakage Current	I <sub>leak</sub>	–	0.15	–	μA	OE = Low
Maximum Output Current	I <sub>driver</sub>	–	–	32	mA	Maximum average current drawn from OUT+ or OUT-
<b>Output Characteristics</b>						
Output High Voltage	VOH	V <sub>dd</sub> -1.1	–	V <sub>dd</sub> -0.7	V	See Figure 2
Output Low Voltage	VOL	V <sub>dd</sub> -1.9	–	V <sub>dd</sub> -1.5	V	See Figure 2
Output Differential Voltage Swing	V <sub>Swing</sub>	1.2	1.6	2.0	V	See Figure 3
Rise/Fall Time	T <sub>r</sub> , T <sub>f</sub>	–	225	290	ps	20% to 80%, see Figure 2
<b>Jitter</b>						
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.220	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dds</sub> . Includes spurs. 7.0 x 5.0 mm package.
		–	0.225	0.280	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dds</sub> . Includes spurs, 3.2 x 2.5 mm package.
		–	0.1	–	ps	f = 156.25, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, Includes spurs, all V <sub>dds</sub>
RMS Period Jitter <sup>[1]</sup>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>DD</sub> = 3.3V or 2.5V

## Notes:

1. Measured according to JESD65B

Table 3. Electrical Characteristics – LVDS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
Current Consumption	I <sub>dd</sub>	–	–	79	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3V or 2.5V
OE Disable Supply Current	I <sub>OE</sub>	–	–	58	mA	OE = Low
Output Disable Leakage Current	I <sub>leak</sub>	–	0.15	–	μA	OE = Low
<b>Output Characteristics</b>						
Differential Output Voltage	VOD	250	–	455	mV	See Figure 4
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 4
Offset Voltage	VOS	1.125	–	1.375	V	See Figure 4
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 4
Rise/Fall Time	T <sub>r</sub> , T <sub>f</sub>	–	400	470	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 4
<b>Jitter</b>						
RMS Phase Jitter (random)	T <sub>phj</sub>	–	0.215	0.265	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dds</sub> . Includes spurs. 7.0 x 5.0 mm package.
		–	0.235	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dds</sub> . Includes spurs. 5.0 x 3.2 mm package. 0.275 ps.
		–	0.1	–	ps	f = 156.25, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, Includes spurs, all V <sub>dds</sub>
RMS Period Jitter <sup>[2]</sup>	T <sub>jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>DD</sub> = 3.3V or 2.5V

## Notes:

2. Measured according to JESD65B

**Table 4. Electrical Characteristics – HCSL**

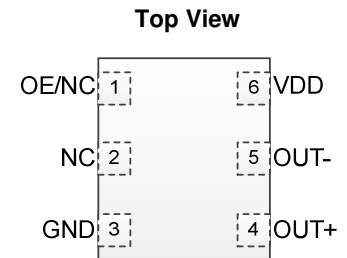
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>Current Consumption</b>						
Current Consumption	I <sub>dd</sub>	–	–	89	mA	Excluding Load Termination Current, V <sub>dd</sub> = 3.3V or 2.5V
OE Disable Supply Current	I <sub>_OE</sub>	–	–	58	mA	OE = Low
Output Disable Leakage Current	I <sub>_leak</sub>	–	0.15	–	μA	OE = Low
Maximum Output Current	I <sub>_driver</sub>	–	–	35	mA	Maximum average current drawn from OUT+ or OUT-
<b>Output Characteristics</b>						
Output High Voltage	VOH	0.60	–	0.90	V	See Figure 2
Output Low Voltage	VOL	-0.05	–	0.08	V	See Figure 2
Output Differential Voltage Swing	V <sub>_Swing</sub>	1.2	1.4	1.80	V	See Figure 3
Rise/Fall Time	T <sub>r</sub> , T <sub>f</sub>	–	360	465	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%, see Figure 2
<b>Jitter</b>						
RMS Phase Jitter (random)	T <sub>_phj</sub>	–	0.220	0.270	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dds</sub> , Includes spurs, 7.0 x 5.0 mm package.
		–	0.230	0.275	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all V <sub>dds</sub> , Includes spurs, 3.2 x 2.5 mm package.
		–	0.1	–	ps	f = 156.25, IEEE802.3-2005 10GbE jitter mask integration bandwidth = 1.875 MHz to 20 MHz, Includes spurs, all V <sub>dds</sub>
RMS Period Jitter <sup>[3]</sup>	T <sub>_jitt</sub>	–	1.0	1.6	ps	f = 100, 156.25 or 212.5 MHz, V <sub>DD</sub> = 3.3V or 2.5V

**Notes:**

3. Measured according to JESD65B

**Table 5. Pin Description**

Pin	Map	Functionality	
1	OE/NC	Output Enable (OE)	H <sup>[4]</sup> : specified frequency output L: output is high impedance
		Non Connect (NC)	H or L or Open: No effect on output frequency or other device functions
2	NC	NA	No Connect; Leave it floating or connect to GND for better heat dissipation
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage <sup>[5]</sup>



**Figure 1. Pin Assignments**

**Notes:**

- 4. In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven.
- 5. A capacitor of value 0.1 μF or higher between V<sub>dd</sub> and GND is required. An additional 10 μF capacitor between V<sub>dd</sub> and GND is required for the best phase jitter performance

### Table 6. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Min.	Max.	Unit
VDD	-0.5	4.0	V
VIH		VDD + 0.3V	V
VIL	-0.3		V
Storage Temperature	-65	150	°C
Maximum Junction Temperature		130	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C

### Table 7. Thermal Considerations<sup>[6]</sup>

Package	$\theta_{JA}$ , 4 Layer Board (°C/W)	$\theta_{JC}$ , Bottom (°C/W)
3225, 6-pin	80	30
7050, 6-pin	52	19

**Notes:**

6. Refer to JESD51 for  $\theta_{JA}$  and  $\theta_{JC}$  definitions, and reference layout used to determine the  $\theta_{JA}$  and  $\theta_{JC}$  values in the above table.

### Table 8. Maximum Operating Junction Temperature<sup>[7]</sup>

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	95°C
85°C	110°C

**Notes:**

7. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

### Table 9. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	G
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	G
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

## Waveform Diagrams

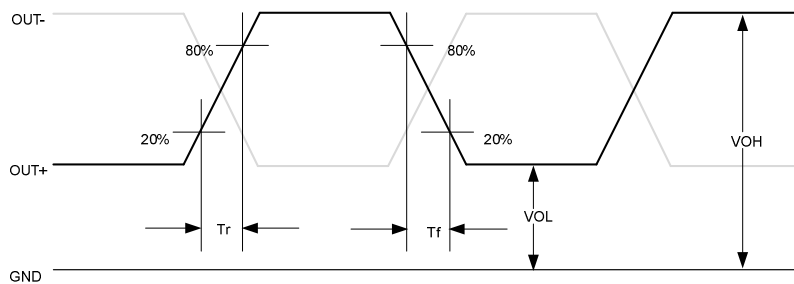


Figure 2. LVPECL/HCSL Voltage Levels per Differential Pin (OUT+/OUT-)

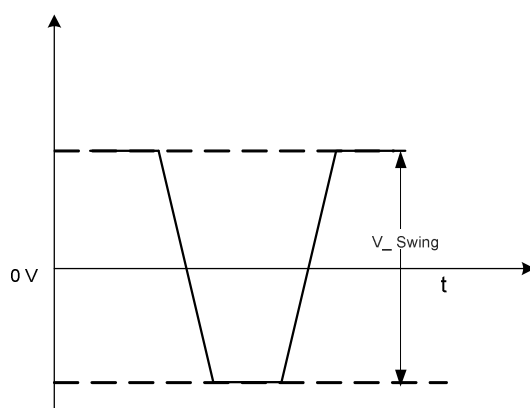


Figure 3. LVPECL/HCSL Voltage Levels across Differential Pair

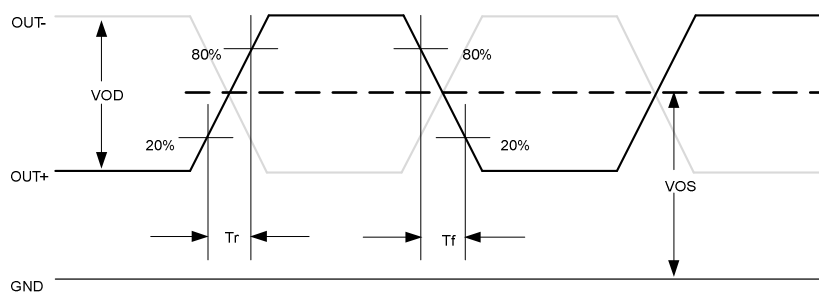


Figure 4. LVDS Voltage Levels per Differential Pin (OUT+/OUT-)

## Termination Diagrams

### LVPECL:

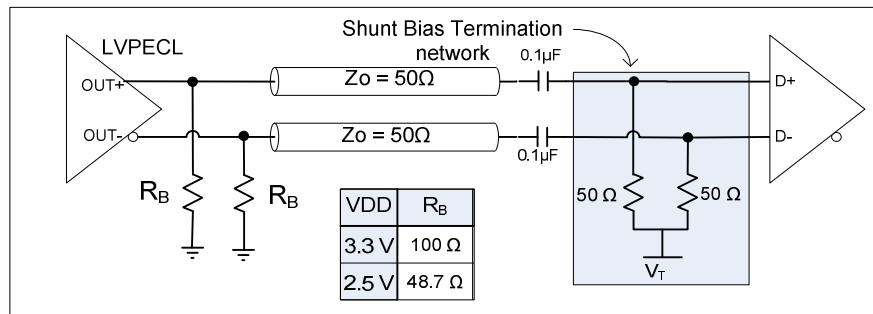


Figure 5: LVPECL with AC-coupled termination

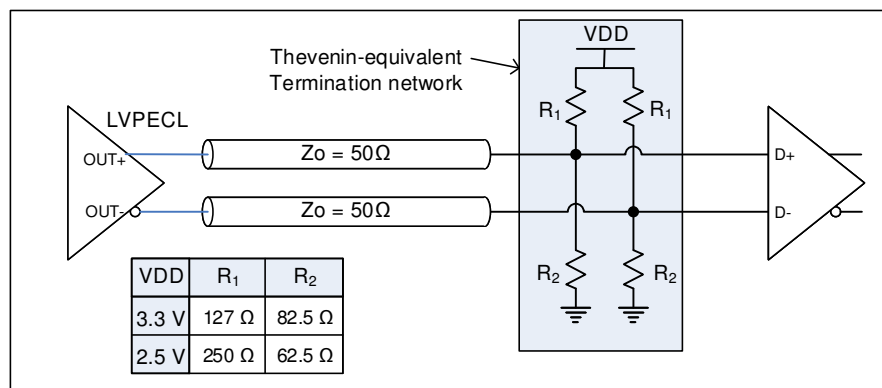


Figure 6: LVPECL DC-coupled load termination with Thevenin equivalent network

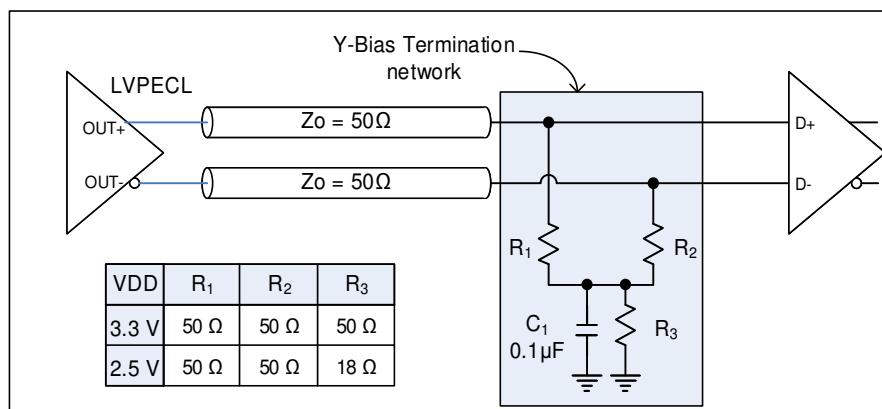


Figure 7: LVPECL with Y-Bias termination

### Termination Diagrams (Continued)

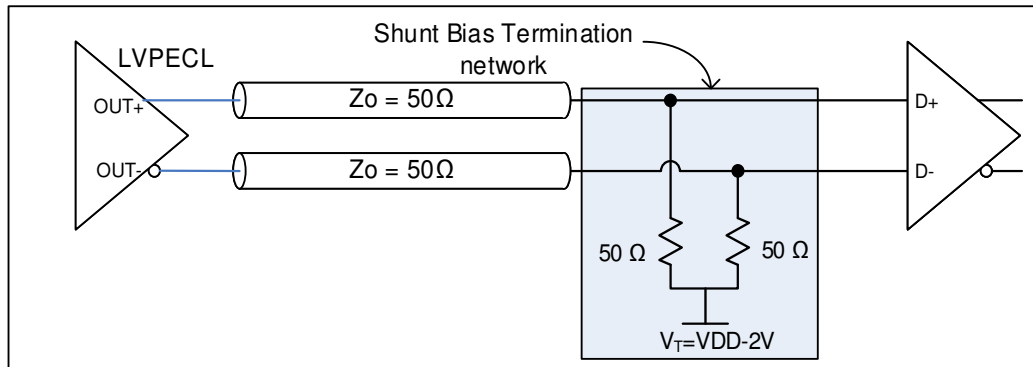


Figure 8: LVPECL with DC-coupled parallel shunt load termination

## Termination Diagrams (Continued)

LVDS:

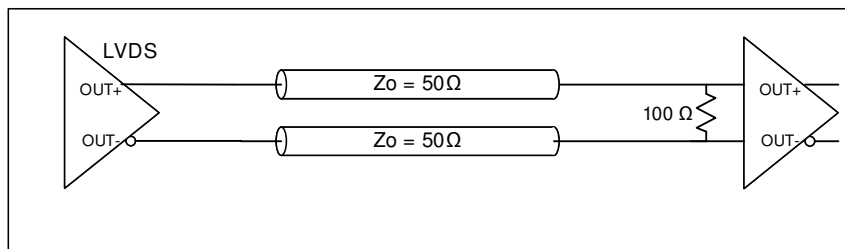


Figure 9: LVDS single DC termination at the load

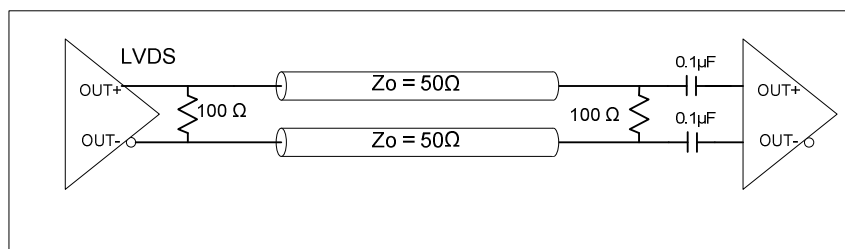


Figure 10: LVDS double AC termination with capacitor close to the load

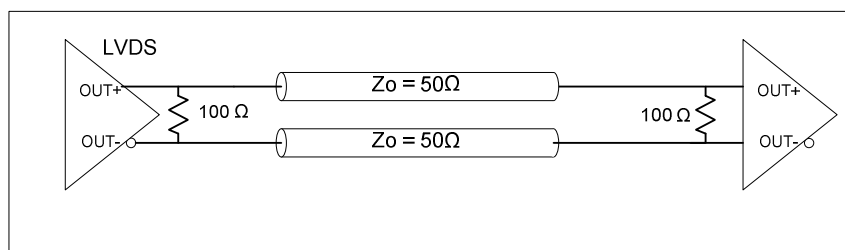


Figure 11: LVDS double DC termination



### Termination Diagrams (Continued)

HCSL:

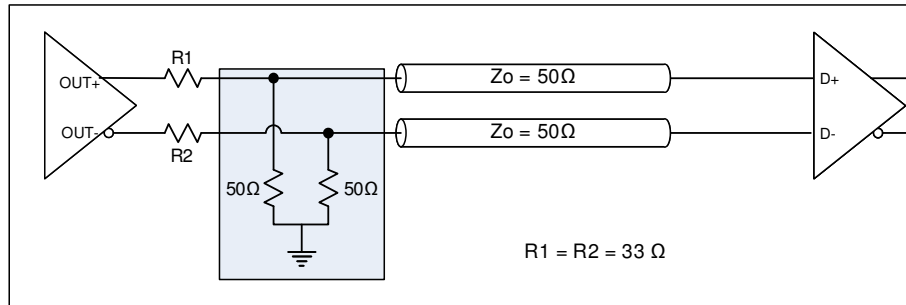


Figure 12: HCSL interface termination

## Dimensions and Patterns

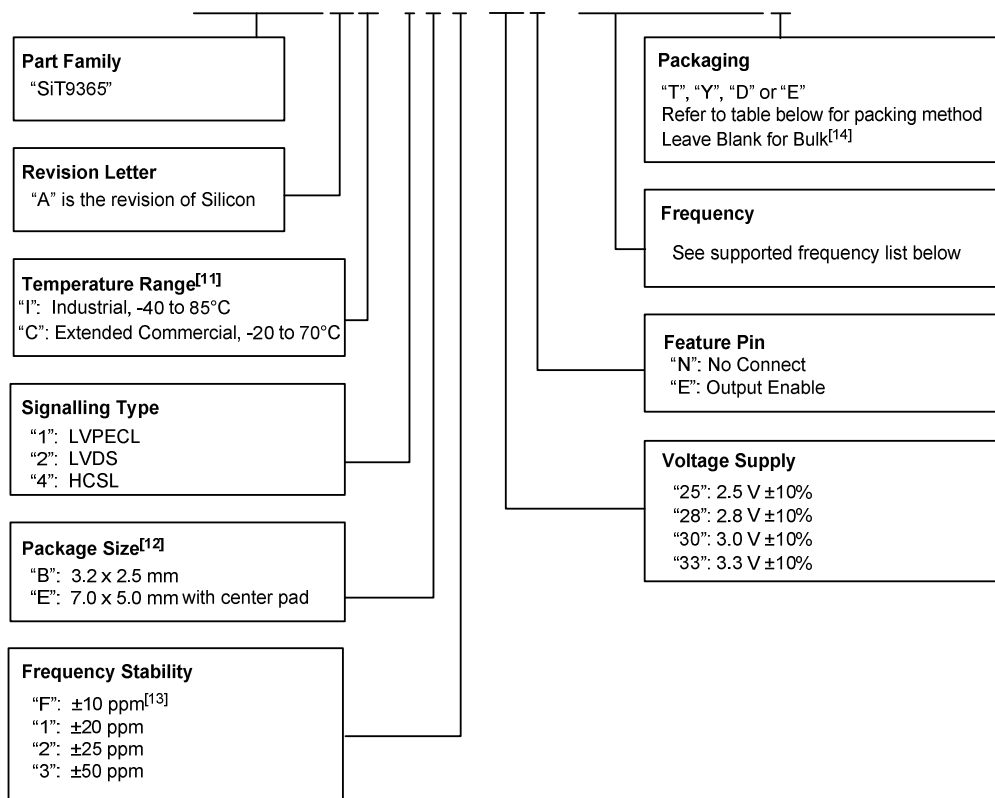
Package Size – Dimensions (Unit: mm) <sup>[8]</sup>	Recommended Land Pattern (Unit: mm) <sup>[9]</sup>																																																														
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**Notes:**

8. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
9. A capacitor of value 0.1 μF or higher between Vdd and GND is required. An additional 10 μF capacitor between Vdd and GND is required for the best phase jitter performance
10. The center pad has no electrical function. Soldering down the center pad to the GND is recommended for best thermal dissipation, but is optional.

## Ordering Information

### SiT9365AC-1B2-33E125.000000T



**Notes:**

11. Contact [SiTime](#) for higher temperature range options
12. Contact [SiTime](#) for 5.0 x 3.2 mm package
13. Contact [SiTime](#) for ± 10 ppm option
14. Bulk is available for sampling only

**Table 10. Supported Frequencies**

25.000000 MHz	30.720000 MHz	50.000000 MHz	53.125000 MHz	61.440000 MHz	62.500000 MHz	74.175824 MHz	74.250000 MHz
75.000000 MHz	77.760000 MHz	98.304000 MHz	100.000000 MHz	106.250000 MHz	122.880000 MHz	125.000000 MHz	133.333333 MHz
148.351648 MHz	150.000000 MHz	153.600000 MHz	155.520000 MHz	156.250000 MHz	159.375000 MHz	160.000000 MHz	161.132813 MHz
166.666666 MHz	168.040678 MHz	200.000000 MHz	212.500000 MHz	250.000000 MHz	300.000000 MHz	322.265625 MHz	325.000000 MHz

**Table 11. Ordering Codes for Supported Tape & Reel Packing Method**

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)	12 mm T&R (3ku)	12 mm T&R (1ku)	16 mm T&R (3ku)	16 mm T&R (1ku)
7.0 x 5.0	—	—	—	—	T	Y
3.2 x 2.5	D	E	T	Y	—	—

**Table 12. Revision History**

Revision	Release Date	Change Summary
1.0	09/06/2017	Final release

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