L9634

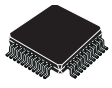
OCTAL INTELLIGENT SQUIB DRIVER ASIC

PRELIMINARY DATA

1 FEATURES

- EIGHT SQUIB DEPLOYMENT DRIVERS
- DEPLOYMENT CURRENT AND TIME PROGRAMMABLE VIA SPI, (1.2A/2ms AND 1.75A/4ms)
- CAPABILITY TO DEPLOY WITH 1.47A (2.14A) UNDER 40V (21V) LOAD-DUMP CONDITION AND THE LOW SIDE MOS SHORTED TO -1V.
- 5.5MHZ SPI INTERFACE WITH MESSAGE VALIDATION
- 4 CHANNELS OF DISCRETE/SERIAL LOGIC ARMING INTERFACE PROGRAMMABLE VIA SPI
- DEPLOYMENT DRIVER SELF-DIAGNOSTICS:
  - SHORT TO BATTERY/GROUND AND OPEN CIRCUIT
  - SQUIB RESISTANCE MEASUREMENT
  - SHORT BETWEEN CHANNELS DETECTIONS
  - HIGH AND LOW SIDE MOS TESTS
  - GROUND LOSS DETECTION
- -40 °C TO +85 °C OPERATING AMBIENT TEMPERATURE
- 4KV ESD CAPABILITY ON ALL OUTPUT-DRIVER PINS AND 2KV ON ALL OTHERS

Figure 1. Package



TQFP44

Table 1. Order Codes

Part Number	Package
L9634	TQFP44

2 DESCRIPTION

The L9634 is an Octal Intelligent Squib Driver ASIC. It is packaged in a 44pin Thin Quad Flat Pack (TQFP) package and designed using ST's proprietary BCD4 technology. The UH30 is intended to deploy up to eight airbag squib circuits and provide diagnostics for each of the deployment drivers. Each of the eight drivers is sized to deliver up to 1.75A minimum for up to 4ms. The deployment current and time are both programmable via the SPI port

Figure 2. Block Diagram

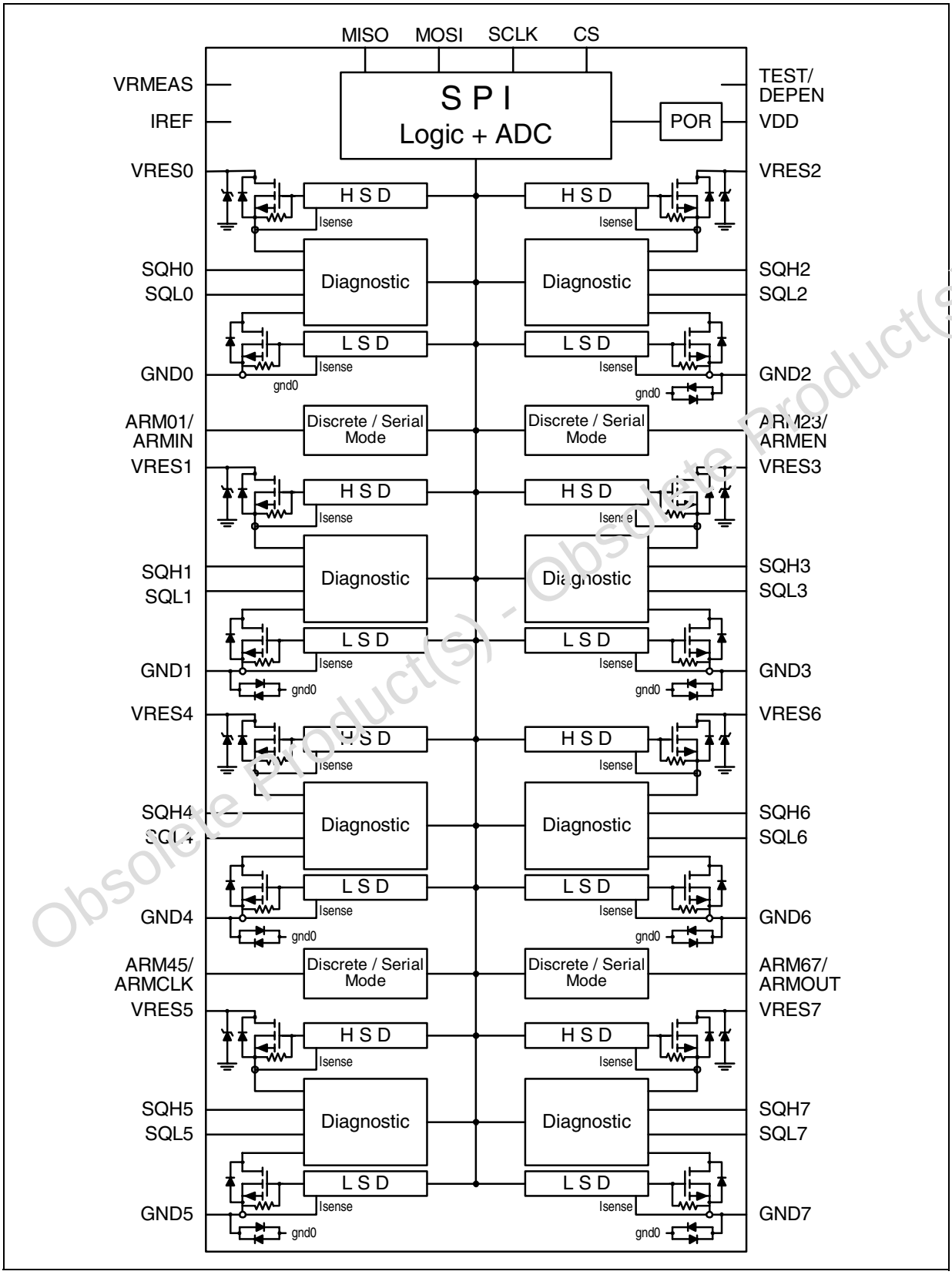


Figure 3. Pin Connection (Top view)

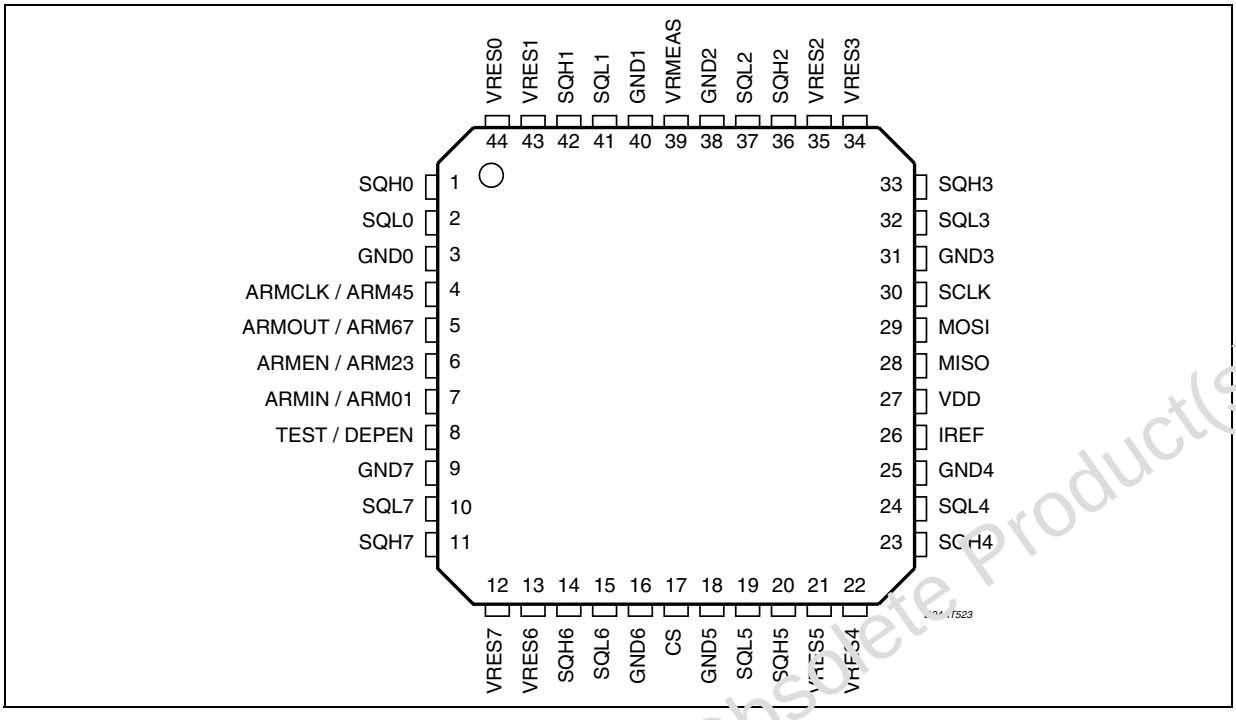


Table 2. Pin Function

N°	Pin	Description	I/O Type
1	SQH0	High Side Driver Output for Channel 0	Out
2	SQL0	Low Side Driver Output for Channel 0	Out
3	GND0	Power Ground 0	-
4	ARMCLK	ARM Serial Mode Clock Input	In
	ARM45	Discrete Arm Signal for Channel 4 & 5	In
5	ARMOUT	ARM Serial Mode Data Output	Out
	ARM67	Discrete Arm Signal for Channel 6 & 7	In
6	ARMEN	ARM Serial Mode Data Enable	In
	ARM23	Discrete Arm Signal for Channel 2 & 3	In
7	ARMIN	ARM Serial Mode Data Input	In
	ARM01	Discrete Arm Signal for Channel 0 & 1	In
8	TEST	Test Input Pin	In
	DEPEN	Deployment Enable	In
9	GND7	Power Ground 7	-
10	SQL7	Low Side Driver Output for Channel 7	Out
11	SQH7	High Side Driver Output for Channel 7	Out
12	VRES7	Reserve Voltage for Loop Channel 7	In
13	VRES6	Reserve Voltage for Loop Channel 6	In
14	SQH6	High Side Driver Output for Channel 6	Out
15	SQL6	Low Side Driver Output for Channel 6	Out
16	GND6	Power Ground 6	-
17	CS	SPI Chip Select	In

Table 2. Pin Function (continued)

N°	Pin	Description	I/O Type
18	GND5	Power Ground 5	-
19	SQL5	Low Side Driver Output for Channel 5	Out
20	SQH5	High Side Driver Output for Channel 5	Out
21	VRES5	Reserve Voltage for Loop Channel 5	In
22	VRES4	Reserve Voltage for Loop Channel 4	In
23	SQH4	High Side Driver Output for Channel 4	Out
24	SQL4	Low Side Driver Output for Channel 4	Out
25	GND4	Power Ground 4	-
26	IREF	External Current Reference Resistor	Out
27	VDD	VDD Supply Voltage	In
28	MISO	SPI Data Out	Out
29	MOSI	SPI Data In	In
30	SCLK	SPI Clock	In
31	GND3	Power Ground 3	-
32	SQL3	Low Side Driver Output for Channel 3	Out
33	SQH3	High Side Driver Output for Channel 3	Out
34	VRES3	Reserve Voltage for Loop Channel 3	In
35	VRES2	Reserve Voltage for Loop Channel 2	In
36	SQH2	High Side Driver Output for Channel 2	Out
37	SQL2	Low Side Driver Output for Channel 2	Out
38	GND2	Power Ground 2	-
39	VRMEAS	Supply Voltage for Resistance Measurement	In
40	GND1	Power Ground 1	-
41	SQL1	Low Side Driver Output for Channel 1	Out
42	SQH1	High Side Driver Output for Channel 1	Out
43	VRES1	Reserve Voltage for Loop Channel 1	In
44	VRES0	Reserve Voltage for Loop Channel 0	In

Table 3. Absolute Maximum Ratings *)

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.3 to 6.5	V
	VRMEAS voltage	-0.3 to 40	V
	VRES voltage	-0.3 to 40	V
	SQHX, SQLX squib high and low side drv	-1 to 40	V
V_{in}	Discrete input voltage	-0.3 to 6.5	V
T_j	Maximum junction temperature	+150	°C

*) Maximum ratings are absolute values: exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 4. Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}amb}$	Thermal Resistance Junction to Ambient	68	°C/W
$R_{thj\text{-}case}$	Thermal Resistance Junction to Case	14	°C/W
T_{stg}	Storage Temperature	-50 to +175	°C

3 ELECTRICAL CHARACTERISTICS

Table 5. Electrical Characteristics
(VRES = 6.5 to 40V, VDD = 4.9 to 5.1V, VRMEAS = 7.0V to 26.5V, T_{amb} = -40°C to +95°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{RST}	VDD Internal Voltage Reset	VDD drops until deployment drivers are disabled	4.2		4.7	V
I_{DD}	VDD Input Current	Normal operation			5	mA
		Short to –1V on SQH			5	
		Short to –1V on SQL			5	
		Deployment			20	
V_{IH}	Input Voltage MOSI, SCLK, CS, ARMx	Input Logic = 1			2.0	V
V_{IL}		Input Logic = 0	0.8			
V_{HYS}			50			mV
I_{LKG}	Input Leakage Current MOSI, SCLK	V_{IN} = VDD			1	µA
		V_{IN} = 0 to V_{IH}	-1			
V_{IH_DEPEN}	DEPEN Input Voltage				2.0	V
V_{IL_DEPEN}			0.8			
V_{HYS}			50			mV
V_{IH_TEST}	TEST Input Voltage				8.5	V
V_{IL_TEST}			5.5			
I_{PD}	Input Pulldown Current ARMx, CS	V_{IN} = V_{IL} to VDD	10		50	µA
	DEPEN	V_{IN} = V_{IL} to VDD	10		100	
V_{OH}	Output Voltage MISO	I_{OH} = -800µA	VDD–0.8			V
V_{OL}		I_{OL} = 1.6mA			0.4	
I_Z	MISO Tri-State Current	MISO = VDD			10	µA
		MISO = 0V	-10			
Deployment Drivers DC specification						
I_{LKG}	SQH Leakage	VRMEAS=VDD=0, VRESx=36V, V_{SQH}= 0V			50	µA
I_{STG}		VRMEAS=18V; VDD=5V; V_{SQH}= -1V	-5			mA
I_{LKG}	VRESx Bias Current[1]	VRMEAS=18V; VDD=5V; VRESx=36V;SQH shorted to SQL			10	µA
I_{LKG}	SQL Leakage	VRMEAS=Vdd=0, V_{SQL}=18V	-10		10	µA
I_{STG}		VRMEAS=18V; VDD=5V; V_{SQL}= -1V	-5			mA
I_{STB}		VRMEAS=18V; VDD=5V; V_{SQL}= 18V			5	mA
I_{PD}	SQL Pulldown Current	V_{SQLx} = 1.8V - VDD	500		700	µA
SG_{th}	Short to Ground Threshold	VDD = 5.0V	1.9		2.1	V
SB_{th}	Short to Battery Threshold	VDD = 5.0V	3.9		4.1	V

Table 5. Electrical Characteristics (continued)
(VRES = 6.5 to 40V, VDD = 4.9 to 5.1V, VRMEAS = 7.0V to 26.5V, T_{amb} = -40°C to +95°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OC_{th}	Open Circuit Threshold	VDD = 5.0V	1.9		2.1	V
V_{I_th}	MOS Test Load Voltage Detection		100		300	mV
I_{SRC}	Resistance Measurement Current Source	VDD = 5.0V; VRMEAS = 7.0V to 26.5V	38		42	mA
I_{SINK}	Resistance Measurement Current Sink		45		55	mA
R_{DSon}	Total High and Low Side On Resistance	High Side MOS + Low Side MOS VRES = 6.9V; I = 1.2A @95°C			1.5	Ω
R_{DSon}	Total High and Low Side On Resistance	High Side MOS + Low Side MOS VRES = 6.9V; I_{VRES} = 1.1A @95°C			1.5	Ω
R_{DSon}	High Side MOS On Resistance	VRES = 40V; I_{VRES} = 1.1A; Ta = 95°C			0.50	Ω
R_{DSon}	Low Side MOS On Resistance	VRES = 40V; I_{VRES} = 1.1A; Ta = 95°C			1.0	Ω
I_{DEPLOY}	Deployment Current (Channel 0, 3, 4, and 7)	MOSI: Command Mode D11=0; R_{LOAD}=3.75Ω; VRES=6.9 to 40V	1.2		1.47	A
		MOSI: Command Mode D11=1; R_{LOAD}=5.3Ω; VRES=12V to 21V	1.75		2.14	
I_{LIM}	Low side MOS current limit (Channel 0, 3, 4, and 7)	MOSI: Command Mode D11=1/0; R_{LOAD}=5.3Ω; V_{SQH}=18V	1.75		2.14	A
I_{DEPLOY}	Deployment Current (Channel 1, 2, 5, and 6)	MOSI: Command Mode D11=0; R_{LOAD}=3.75Ω; VRES=6.9 to 40V	1.34		1.64	A
		MOSI: Command Mode D11=1; R_{LOAD}=5.3Ω; VRES=12V to 21V	1.95		2.39	
I_{LIM}	Low side MOS current limit (Channel 1, 2, 5, and 6)	MOSI: Command Mode D11=1/0; R_{LOAD}=5.3Ω; V_{SQH}=18V	1.95		2.39	A
I_{BIAS}	Diagnostics Bias Current	V_{SQH}=0V; Part is configured to run in diagnostics mode via SPI	-7		-4	I_{PD}
V_{BIAS}	Diagnostics Bias Voltage	I_{SQH} = -1.5mA	2.7		3.3	V
R_{IREF}	IREF Resistance Threshold	Open Circuit			62.5	kΩ
		Short Circuit	2.5			kΩ
R_{L_RANGE}	Load Resistance Range	%0000 0000 = 0.0Ω; %1111 1111 = 10.0Ω	0.0		10.0	W
ADC_{ACC}	ADC Accuracy	R_L = 4.0Ω to 10.0Ω			5	%
		R_L = 0.0Ω to 4.0Ω			5	counts
ADC_{RES}	ADC Resolution		8			bits
I_{PEAK}	MOS Transient Response Peak Current	See Figure 19 and Figure 20			2.0	I_{FINAL}

Table 5. Electrical Characteristics (continued)
(VRES = 6.5 to 40V, VDD = 4.9 to 5.1V, VRMEAS = 7.0V to 26.5V, T_{amb} = -40°C to +95°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Deployment Drivers AC Specification						
t_{POR}	POR De-glitch Timer		5		20	µs
t_{ON}	MOSs turn on time	ARMx and DEPEN pins asserted Measured from falling edge CS to 90% of I_{FINAL}; See Figure 19 and Figure 20			150	µs
t_{settle}	MOSs settling time	ARMx and DEPEN pins asserted Measured from falling edge CS to 90% - 110% of I_{FINAL}; See Figure 19 and Figure 20			300	µs
t_{PULSE}	Pulse Stretch Timer	See “Pulse Stretch Timer table”	0		60	ms

1. Not applicable during the diagnostic.

Figure 4. MOS Settling time and turn-on time 1

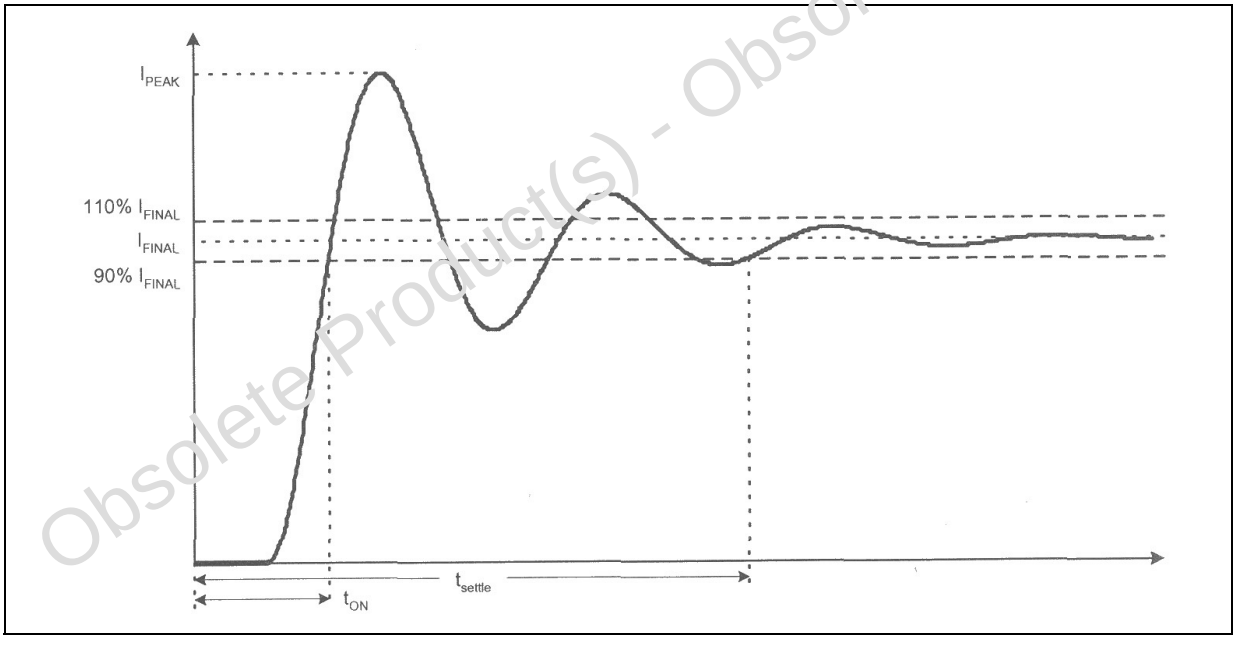


Figure 5. MOS Settling time and turn-on time 2

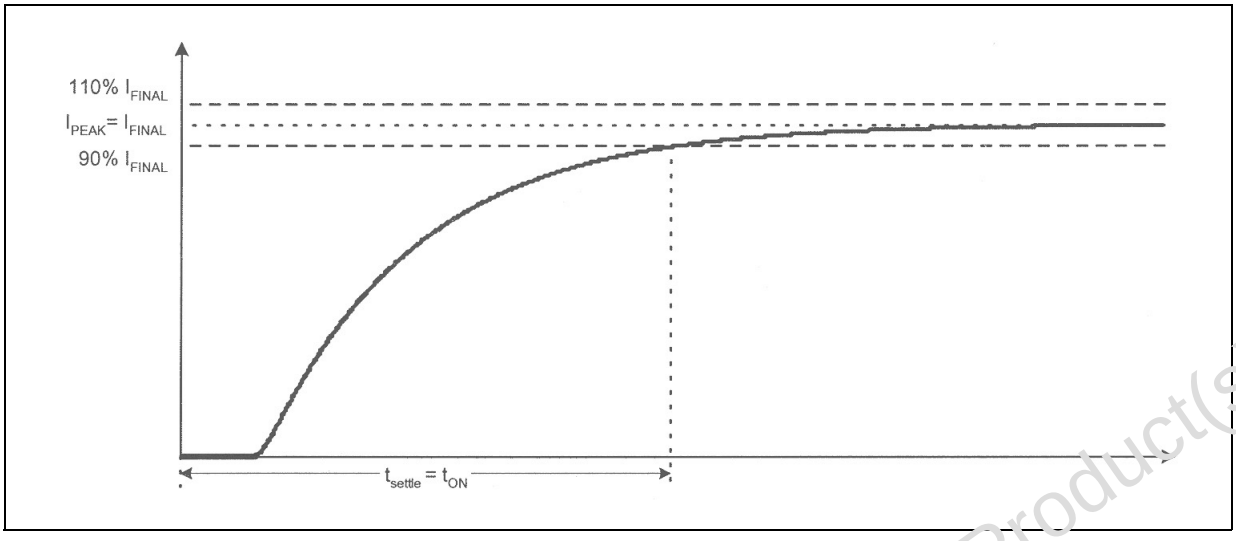


Table 5. Electrical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{P_ACC}	Pulse Stretch Timer Accuracy		-20		20	%
t_{GLITCH}	Pulse Stretcher De-glitch timer		5		25	µs
t_{DEPLOY}	Deployment Time	VRES = 6.9 - 40V[4]; (see table)	2		2.25	ms
		VRES = 12 – 21V[3]; (see table)	4		4.5	
$t_{TIMEOUT}$	Diagnostic Bias Current Time	Time from falling edge of CS until SPI diagnostic complete flag is set, in case of Short to GND for a single channel diagnostic.			2.5	ms
t_{FLT_DLY}	Fault Detection Filter[2]		10		50	µs
I_{SLEW}	Rmeas Current di/dt				40	mA/µs
t_{RES}	Resistance Measurement Time[2]	Duration when I_{DIAG_SRC} and I_{DIAG_SINK} are connected to SQH and SQL during a Resistance Measurement			2.5	ms
t_{MOS_ON}	MOS test turn-on time[2]	On-time of a LS/HS driver during a MOS test			2.5	ms
t_{DETECT}	MOS test detection window[2]	Time window to check for a LS/HS MOS fault on a single loop			7.5	ms
t_{PROP_DLY}	LS/HS MOS turn off propagation delay[2]	Time is measured from the valid LS/HS MOS condition to the LS/HS turn off			10	µs
t_{DIAG1}	Diagnostic Time[3]	For a single loop; MOS Test Disabled			5	ms
t_{DIAG_MULT}		For 8 loops MOS Tests Disabled			40	

2. Application information only; not tested.
3. Time from Falling edge of CS until SPI “diagnostic” flag is set.

Table 6. SPI Timing (All SPI timing is performed with a 200pF load on MISO unless otherwise noted)

Item	Symbol	Parameter	Limits Min	Limits Max	Unit
-	fop	Transfer Frequency	dc	5.50	MHz
1	t_{SCK}	SCLK Period	181	-	ns
2	t_{LEAD}	Enable Lead Time	65	-	ns
3	t_{LAG}	Enable Lag Time	50	-	ns
4	t_{SCLKHS}	SCLK High Time	65	-	ns
5	t_{SCLKLS}	SCLK Low Time	65	-	ns
6	t_{SUS}	MOSI Input Setup Time	20	-	ns
7	t_{HS}	MOSI Input Hold Time	20	-	ns
8	t_A	MISO Access Time	-	66	ns
9	t_{DIS}	MISO Disable Time (Note 1)	-	100	ns
10	t_{VS}	MISO Output Valid Time	-	45	ns
11	t_{HO}	MISO Output Hold Time (Note 1)	0		ns
12	t_{RO}	Rise Time (Design Information)	-	30	ns
13	t_{FO}	Fall Time (Design Information)	-	30	ns
14	t_{CSN}	CS Negated Time	100	-	ns

Notes: 1. Parameters t_{dis} and t_{ho} is measured with no additional capacitive load beyond the normal test fixture capacitance on the MISO pin. Additional capacitance during the disable time test erroneously extends the measured output disable time, and minimum capacitance on MISO is the worst case for output hold time.

Figure 6. SPI Timing Diagram

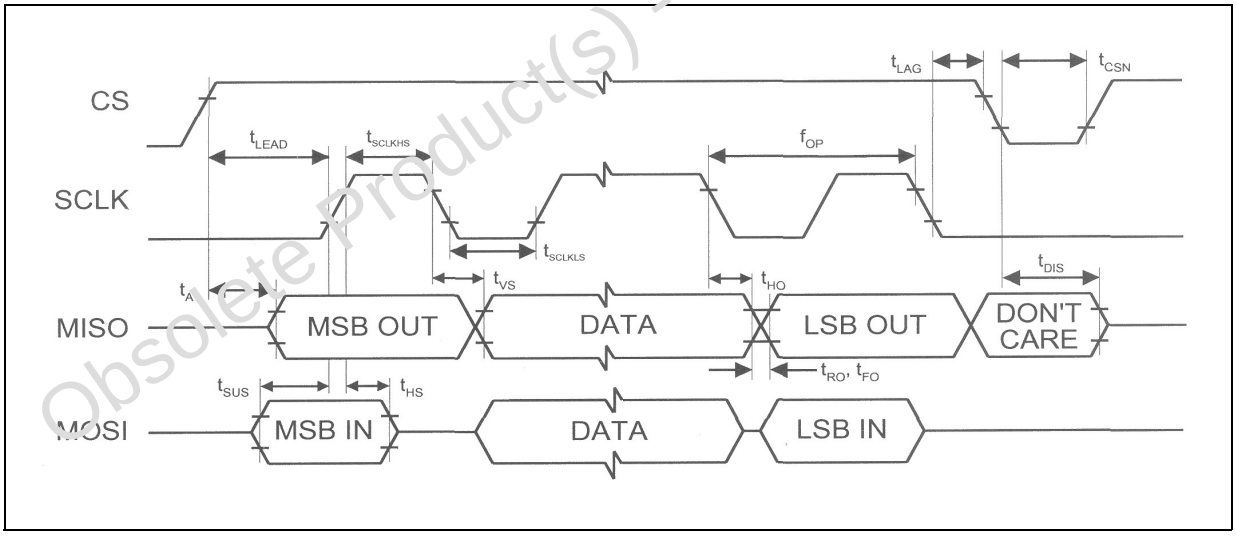
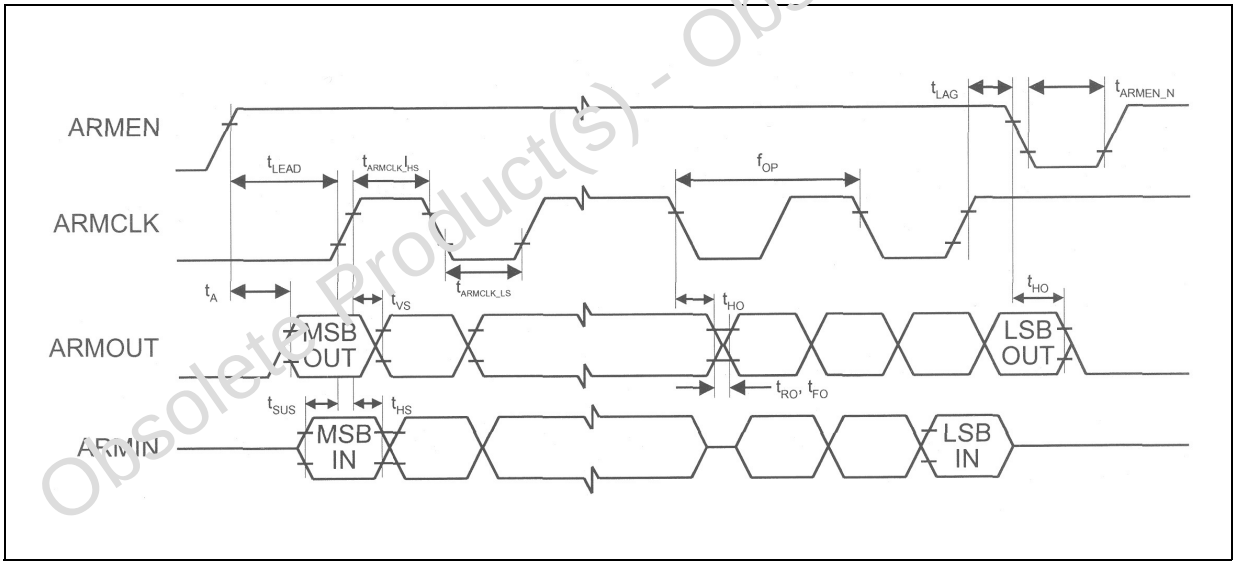


Table 7. Arming Serial Mode Timing

(All Arming serial mode timing is performed with a 50pF load on ARMOUT unless otherwise noted)

Item	Symbol	Parameter	Limits Min	Limits Max	Unit
-	fop	Transfer Frequency	dc	2	MHz
1	t_{ARMCLK}	ARMCLK Period	500		ns
2	t_{LEAD}	Enable Lead Time	250		ns
3	t_{LAG}	Enable Lag Time	100		ns
4	t_{ARMCLK_HS}	ARMCLK High Time	220		ns
5	t_{ARMCLK_LS}	ARMCLK Low Time	220		ns
6	t_{SUS}	ARMIN Input Setup Time	30		ns
7	t_{HS}	ARMIN Input Hold Time	10		ns
8	t_A	ARMOUT Access Time		125	ns
9	t_{VS}	ARMOUT Output Valid Time		190	ns
10	t_{HO}	ARMOUT Output Hold Time	10		ns
11	t_{RO}	Rise Time (Design Information)		20	ns
12	t_{FO}	Fall Time (Design Information)		30	ns
13	t_{ARMEN_N}	ARMEN Negated Time	200		ns

Figure 7. Arming Serial Mode Timing



4 CIRCUIT DESCRIPTION

OSD is an integrated circuit to be used in air bag systems. Its main functions are deployment of the air bag and diagnostics of the SDM (Sensing Deployment Module). The OSD supports 8 de-ployment loops.

The main features of OSD IC are:

- 8 deployment drivers sized to deliver 1.2A min for 2ms min at 40V max or 1.75A min for 4ms min at 21V max (current and time are internally limited while power supply is externally lim-ited).
- 10% accuracy for deployment current.
- 5% accuracy for deployment time.
- High side and Low side current limits programmable via SPI.
- Low-voltage internal reset
- 5.5MHz SPI Interface
- SPI Message Validation
- 4 discrete logic arming inputs
- High and low-side MOS tests
- Squib resistance measurement with 5% accuracy
- Short to -1V protection on all deployment loops (high and low side).
- Capability to deploy with 1.2A min under 40V load-dump condition and the low side MOS is shorted to -1V.
- Capability to deploy with 1.75A min under 21V condition and the low side MOS is shorted to -1V
- Capability to deploy with 1.75A min, when the high side MOS is shorted to 18V-battery and -1V ground difference.
- Capability to deploy the air bag with 1.2A min @ 6.9V VRES
- Deployment loops short to ground and short to battery detection
- Short between loops detection
- -40°C to +95°C ambient temperature
- Package: 44LD TQFP
- Technology: ST's proprietary BCD4 Process

4.1 Power On Reset

VDD loss of regulation detection is filtered for tPOR prior to issue an internal reset. This filter is intended to provide protection from short transients on VDD input. When VDD input voltage decreases below VRST for tPOR, OSD undergoes an internal reset. OSD keeps all current sinks and current sources, except the IPD, inactive and all outputs are driven to an inactive state and remains inactive as VDD decays down to 0V. When VDD rises above VRST, the outputs and the internal current sinks and current sources are enabled. When OSD is in reset, none of the outputs are momentarily turned on.

4.2 Deployment Drivers

The on chip deployment drivers are sized to deliver IDEPLOY. Deployment current and period are programmable via SPI. The high side driver survives deployment condition 1 and 2 as defined here below. SQLx is shorted to ground (-1V) in these two conditions.

Table 8. Deployment Survivability Conditions

No.	Drivers	Conditions			
		I_{DEPLOY}	Voltage	R_{LOAD}	Duration
1.	SQHx	1.47A	VRESx = 40V; SQLx = -1V	1.7Ω	2.5mS
2.		2.14A	VRESx = 21V; SQLx = -1V	1.7Ω	4.5mS
3.	SQLx	2.14A	SQHx = 18V	1.7Ω	4.5mS

The Low Side driver survives deployment condition 3 as defined above.

Upon receiving a valid deployment condition, the respective SQH and SQL drivers are turned on. Also, SQH and SQL drivers are turned on momentarily during a MOS diagnostic. Otherwise, SQH and SQL are inactive under any normal, fault, or transient conditions. Upon a successful deployment of the respective SQH and SQL drivers, a deploy command success flag is asserted via SPI. Refer to Figure 4, Figure 5, Figure 6, and Figure 7. for the valid deployment condition and the "Deploy Command Success" timing.

The following power-up conditions are considered as normal operations in OSD. VRES input can be connected to either a power supply output or an ignition voltage. VDD is connected to the 5V output of power supply. When VRES is connected to the power supply, VDD voltage will reach its regulation voltage before VRES voltage is stabilized. In this condition, OSD has a control of its internal logic and prevents an inadvertent turn-on of the drivers.

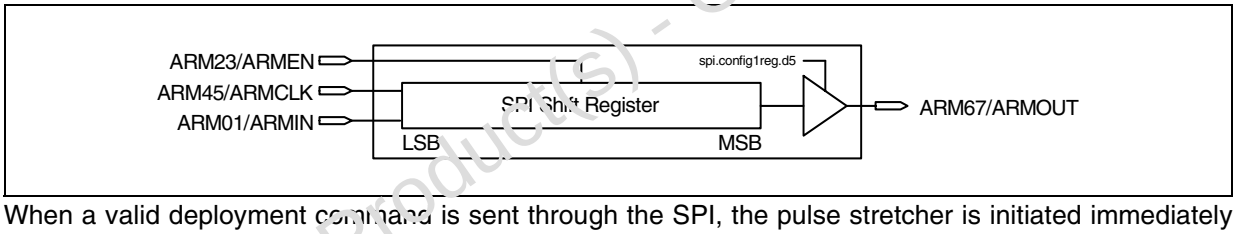
When VRES is connected to the ignition, VRES voltage will be stabilized before VDD reach its regulation voltage. In this condition, all drivers are inactive. A pulldown on the gates of high side drivers (SQH) is provided to prevent these drivers from momentarily turning-on.

Any fault conditions on OSD does not turn on the SQH and SQL drivers. Only a valid deployment condition turns on the respective SQH and SQL drivers.

4.3 Arming Inputs

The arming inputs serve as a fail-safe mechanism to prevent inadvertent deployment. Along with the SPI deployment bit, these inputs provide redundancy. These pins are used either as discrete outputs or as a serial data communication interface with 4-bit shift register. Pulse stretcher timer is provided for each channel/loop. Either ARMx signal or SPI deployment bit starts the pulse stretcher.

Figure 8. Arming Serial Mode Diagram



When a valid deployment command is sent through the SPI, the pulse stretcher is initiated immediately following the falling edge of CS. When another valid deployment command is sent before the timer for the first command expired, the timer is refreshed. Sending an idle command terminates the pulse stretch timer operation. ONLY a timer operation started by a valid SPI deployment command is terminated. An idle command does not affect the timer operation started by ARM signal. OSD deploys a channel, ONLY when the respective ARM signal is asserted during a valid pulse stretcher signal. During the deployment, OSD turns on the respective high (SQH) and low side (SQL) drivers for tDEPLOY. Once deployment is initiated it can not be terminated. If one or more channels are deploying, OSD ignores all commands to the respective channels. The rest of the channels resume operation and respond to the SPI commands. Refer to Figure 5 for a deployment diagram initiated by a SPI deployment command.

In a discrete mode, when the ARM signal is asserted (active high), the pulse stretcher signal is asserted after the de-glitch filter time, tGLITCH, expires. The de-glitch filter is used to prevent noise from starting the pulse stretcher. The pulse stretcher timer, tPULSE, is initiated after a de-glitch time of the ARM falling edge. OSD deploys a channel, ONLY when the respective SPI deployment command is sent during a valid pulse stretcher signal. During the deployment, OSD turns on the respective high (SQH) and low side (SQL) drivers for tDEPLOY. When deployment is initiated it can not be stopped. Refer to Figure 4 and Figure 5 for a deployment diagram initiated by an ARM discrete signal.

In serial mode, OSD latch the arm state for each channel from the shift register when ARMEN is negated. After the de-glitch filter time, tGLITCH, of the ARMEN falling edge expires, OSD starts the pulse stretch timer for the respective channel. Serial mode is selected by setting bit D5 in the Deployment Configuration Register 1 (see "Deployment Configuration Register 1 table 15"). OSD deploys a channel, ONLY when the respective SPI deployment command is sent during a valid pulse stretcher signal. During the deploy-

ment, OSD turns on the respective high (SQHx) and low side (SQLx) drivers for tDEPLOY. When deployment is initiated it can not be stopped. Refer to Figure 11 and Figure 12 for a deployment diagram initiated by an arming signal in serial mode.

Figure 9. Discrete Mode: Deployment Sequence with Pulse Stretch Timer Enabled

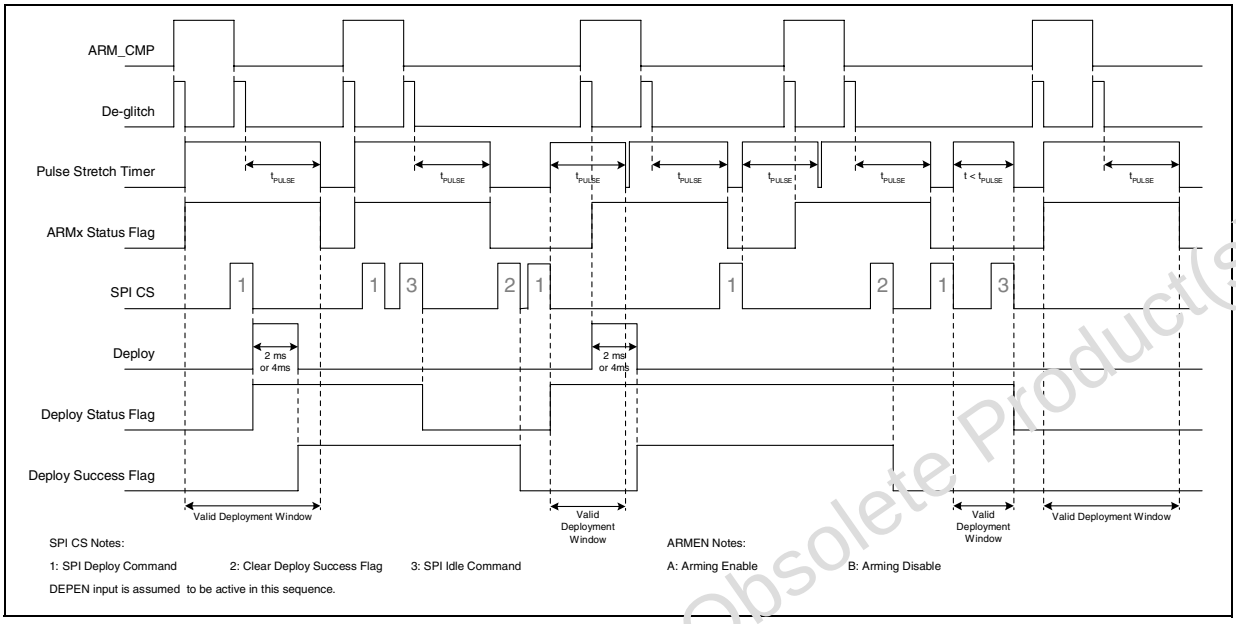


Figure 10. Discrete Mode: Deployment Sequence with Pulse Stretch Timer Disabled

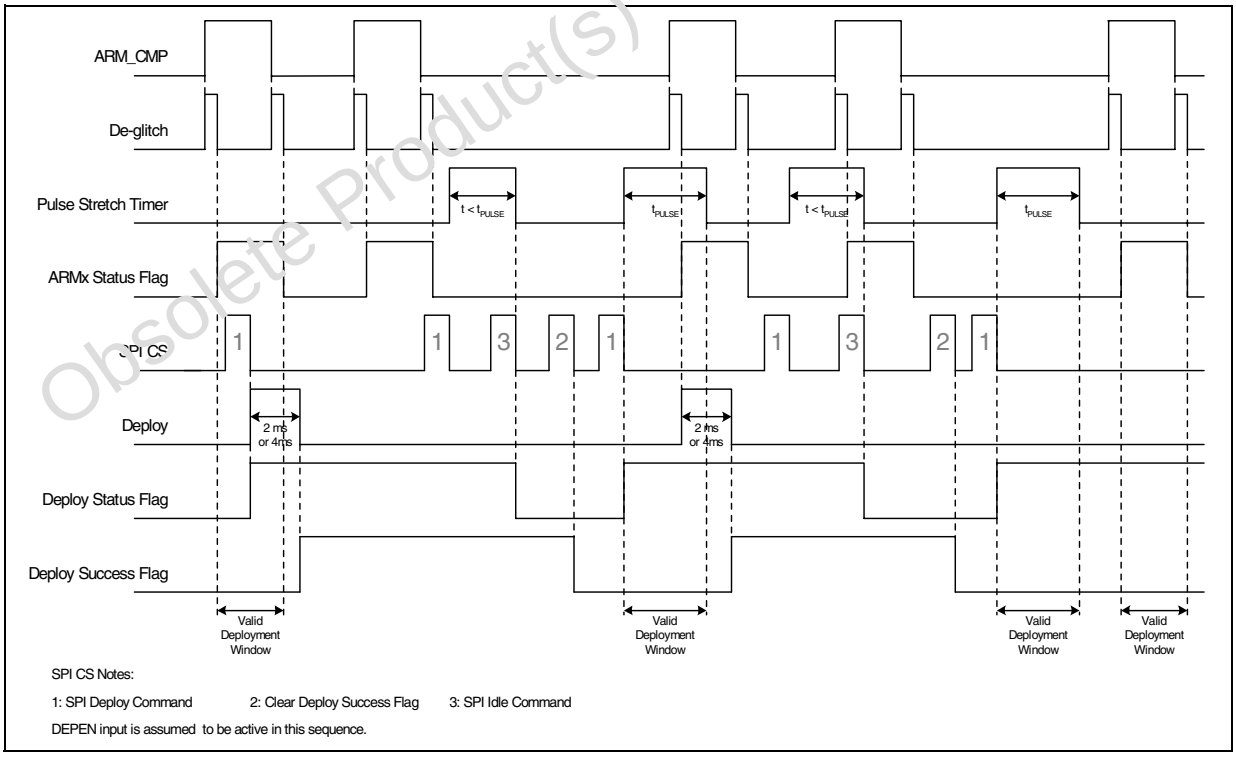


Figure 11. Serial Mode: Deployment Sequence with Pulse Stretch Timer Enabled

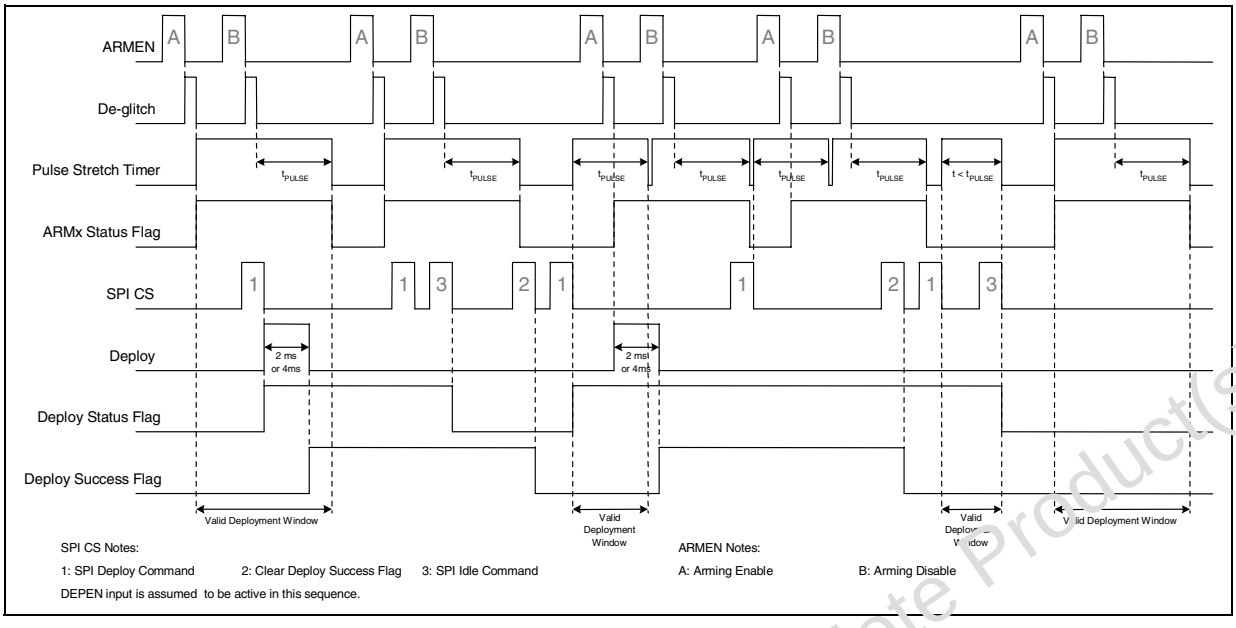
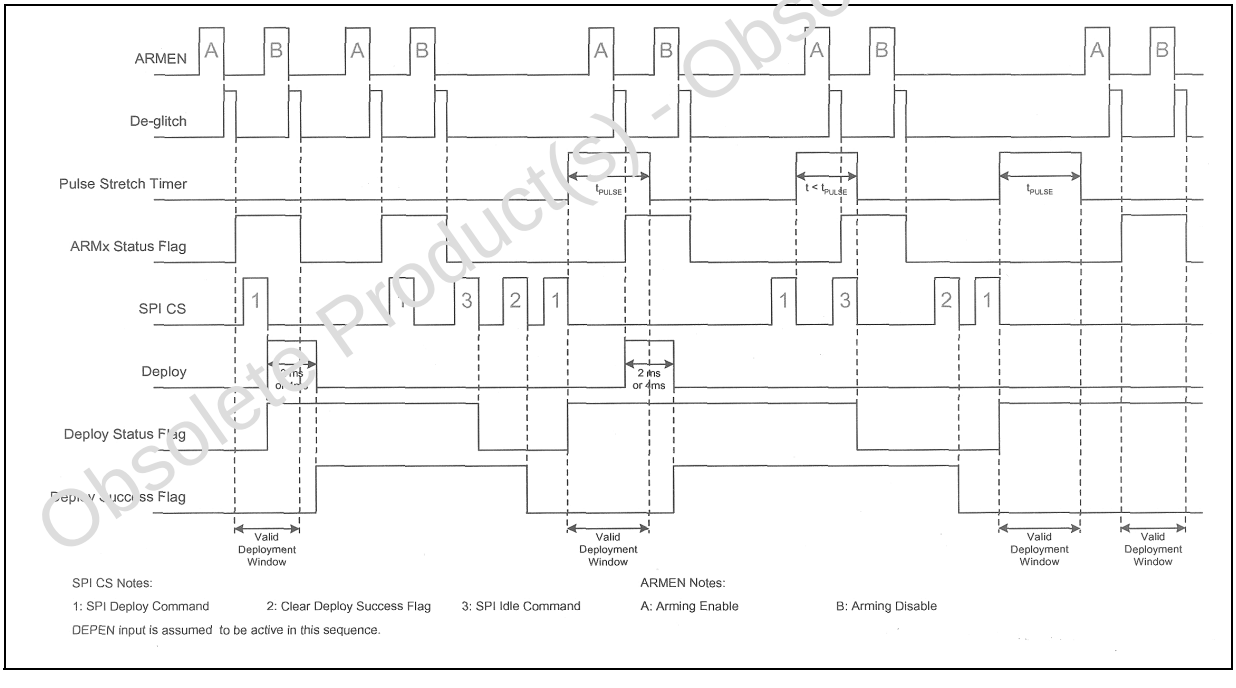


Figure 12. Serial Mode: Deployment Sequence with Pulse Stretch Timer Disabled

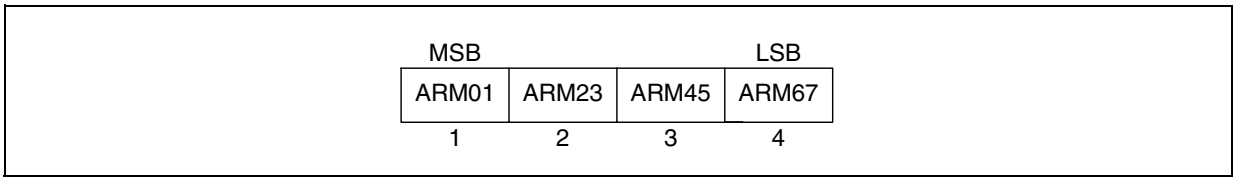


4.4 ARM01 / ARMIN

In discrete mode, this pin acts as the ARM input channel 0 and channel 1. In serial mode, this pin acts as the input of Arming shift register.

The ARMIN input takes data from the processor or another OSD while ARMEN is asserted. The MSB is the first bit of each word received on ARMIN. The LSB is the last bit of each word received on ARMIN. See Figure 8 below for Aming shift register. This pin has a TTL level compatible input voltages allowing proper operation with another devices using a 3.3V to 5.0V supply.

Figure 13. Arming Shift Register



4.5 ARM23 / ARMEN

In discrete mode, this pin acts as the ARM input channel 2 and channel 3. In serial mode, this pin acts as an active high input to select this device for serial transfers. This pin has a TTL level compatible input voltages allowing proper operation with another devices using a 3.3V to 5.0V supply.

While ARMEN is asserted, arming register data is shifted into the ARMIN pin and shifted-out of the ARMOUT pin on both rising and falling edges of ARMCLK. On the falling edge of ARMEN, OSD latch-in the bits from the shift register, and clear the shift register contents.

4.6 ARM45 / ARMCLK

In discrete mode, this pin acts as the ARM input channel 4 and channel 5. In serial mode, this pin acts as a clock input for serial communication. This pin has a TTL level compatible input voltages allowing proper operation with another devices using a 3.3V to 5.0V supply.

When ARMEN is asserted, on the rising or falling edge of ARMCLK the logic level input at the ARMIN pin is shifted into the internal Arming shift register. While MSB in the shift register is shifted-out on the ARMOUT pin. Serial data is shifted in and out of the shift register on each ARMCLK edge. When ARMEN is negated, OSD ignores ARMCLK signal.

A clock edge counter is provided to verify a valid serial arming communication. A valid serial arming communication contains (4n - 1) ARMCLK edges. Otherwise, OSD ignores the serial arming messages.

4.7 ARM67 / ARMOUT

In discrete mode, this pin acts as the ARM input channel 6 and channel 7. In serial mode, this pin acts as the output of Arming shift register. This pin has a TTL level compatible input voltages allowing proper operation with another devices using a 3.3V to 5.0V supply.

When ARMEN is negated, ARMOUT pin is pulled down. When ARMEN is asserted, the MSB is the first bit of the nibble shifted onto ARMOUT. The LSB is the last bit shifted onto ARMOUT.

4.8 TEST / DEPEN (Deployment Enable)

DEPEN is a deployment enable input, which is an active high input. When DEPEN is negated, it inhibits the high-side and the low-side MOSs from turning on. If DEPEN is negated when a valid deployment is received, OSD inhibits the deployment. If DEPEN is negated when a diagnostic command is received, OSD executes the diagnostic sequence. If a MOS diagnostic is executed while DEPEN is negated, OSD returns a low-side MOS fault. SPI remains functional while this pin is pulled low. When this pin is asserted, OSD is able to drive its high and low side drivers upon receiving a valid deployment command or a MOS diagnostic. DEPEN does not initiate a deployment nor terminate a deployment if it is already started.

To enter a test mode, this pin has to be pulled higher than VIH_TEST.

4.9 Deployment Driver Diagnostics

OSD runs an on-chip self-diagnostics when commanded via SPI. By default, OSD is in the monitor mode (D15 & D14 = %11). The on-chip diagnostic operates according to the flow chart shown in Figure 15. If a fault condition is detected, the state machine asserts a fault bit, which serves as a flag to the processor. Once a fault bit asserted, OSD terminates the diagnostic tests for that particular channel and start diagnostic tests on the next channel. The fault information in OSD is sent out through MISO. For diagnostic

mode SPI bit definition.

OSD is able to differentiate short to battery, open circuit, and short to ground. A resistance measurement provides the resistance value of a load connected between SQH and SQL. MOS diagnostic verifies the functionality of the high and low side MOS. Refer to Figure 14 for the diagnostic diagram. A detailed operation for each test is described in sections below.

Figure 14. Diagnostic Diagram

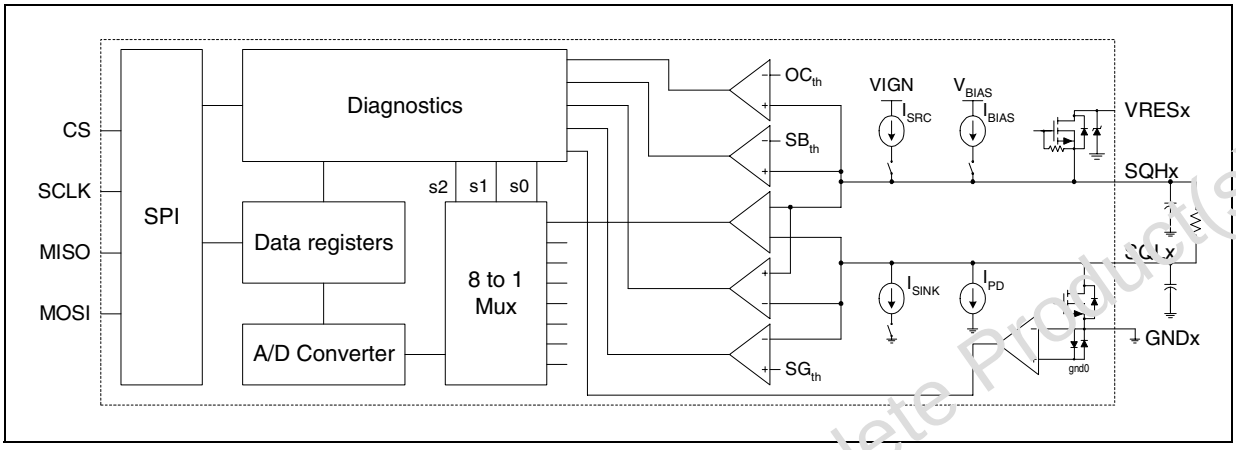
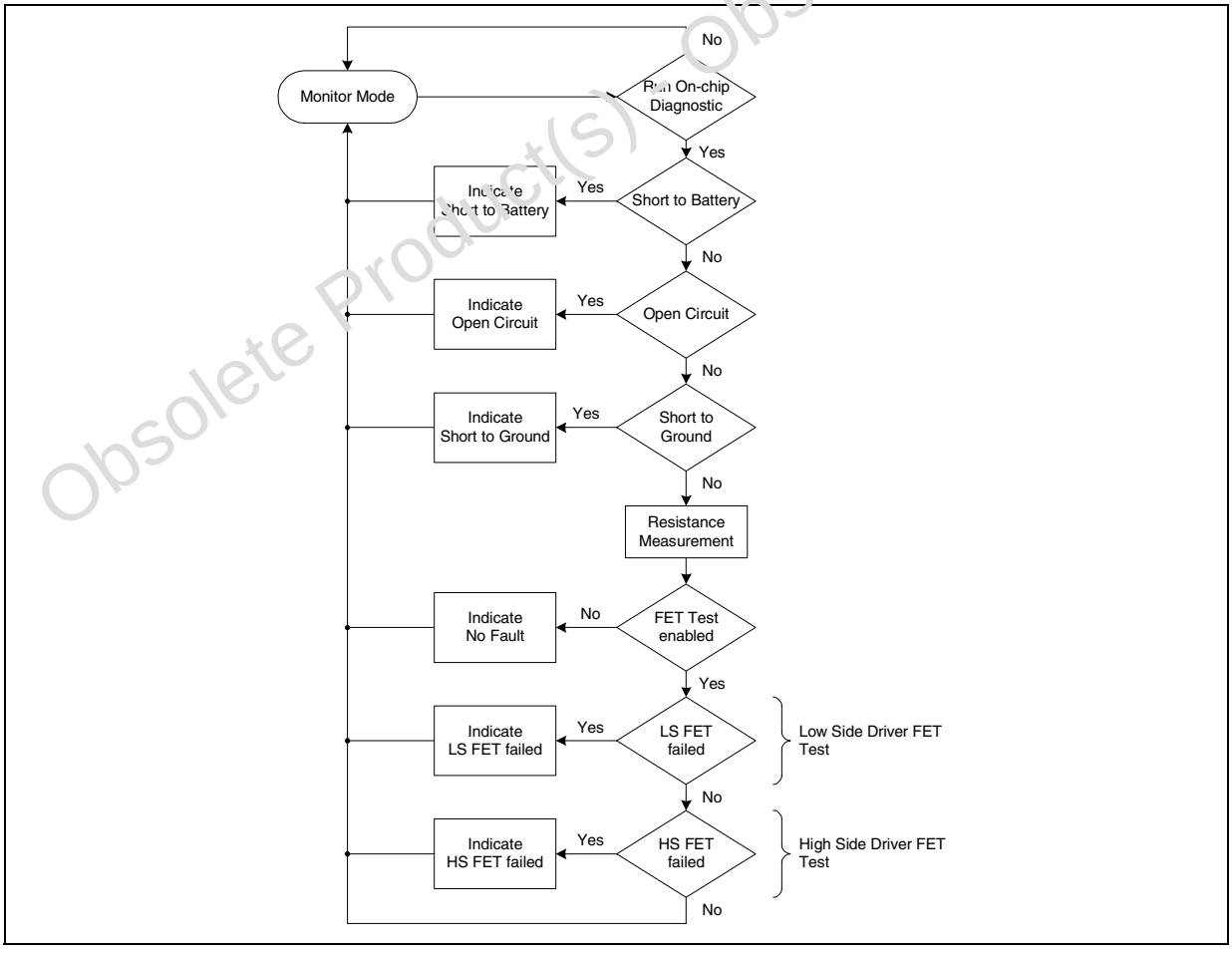


Figure 15. Diagnostic Flow Chart



4.10 Short Between Loops Diagnostic

OSD has a loop bias voltage that is multiplexed between the eight deployment loops. The bias voltage is pulled-up to VDIAG_BIAS. Each deployment loop is pulled to ground through a current sink, IPD. If one of these loops is shorted to the one that is biased, a "Short Between Loops" fault bit is asserted and reported via SPI. Refer to Figure 16 for Short Between Loops diagram.

Short between loops test is initiated when OSD receives one of the following message:

- MOSI monitor mode message with bit D12 = '1,' bit D9 = '1,' and bit D8 = '1.'
- MOSI diagnostic mode message with bit D12 = '1' and bit D9 = '1.'

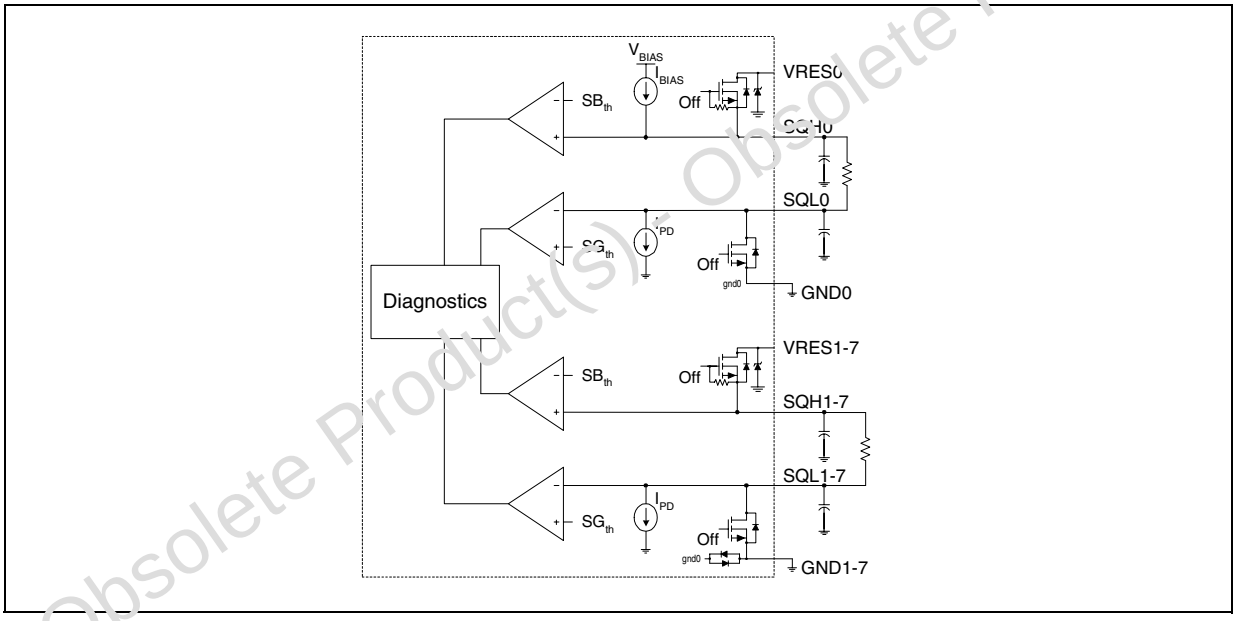
The test terminates when OSD receives one of the following message:

- MOSI monitor mode message with bit D12 = '1,' bit D9 = '1,' and bit D8 = '0'
- MOSI diagnostic mode message with bit D12 = '1' and bit D9 = '0.'
- MOSI command mode with bit D7 through bit D0 = '0.'

If the test is in progress, OSD will continue the test when any of the following messages is received.

- MOSI monitor mode, except the one with bit D12 = '1,' bit D9 = '1,' and bit D8 = '0'
- MOSI register mode

Figure 16. Short Between Loops Diagram

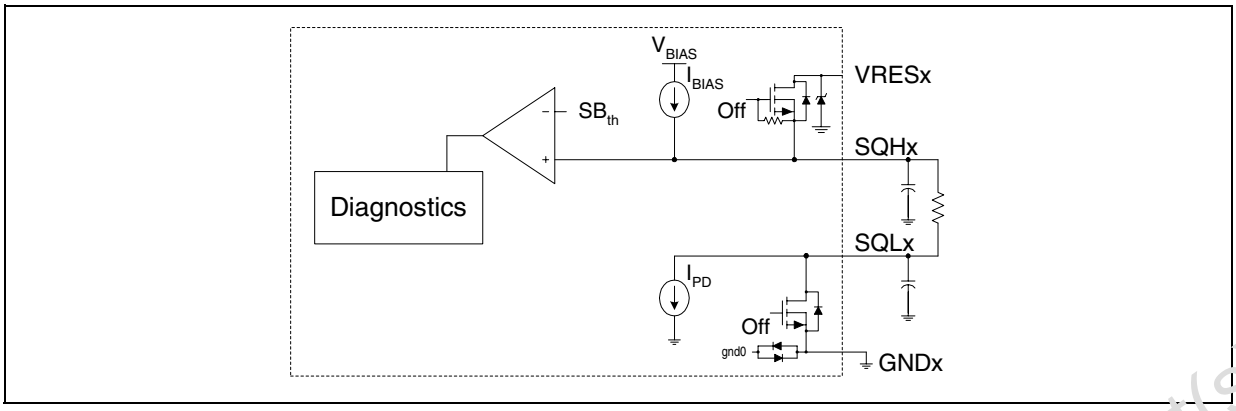


After a POR event, short between loop is disabled. Need to receive a SPI command to execute a short between loop diagnostic.

4.11 Short to Battery Diagnostic

During a short to battery test, a current source referenced to VDD is connected to the SQHx. When no short to battery condition exists, SQHx and SQLx are equal to VDIAG_BIAS. If the voltage on SQHx is above SBth for tFLT_DLY, OSD will assert the short to battery fault. Refer to Figure 17 for a short to battery test diagram.

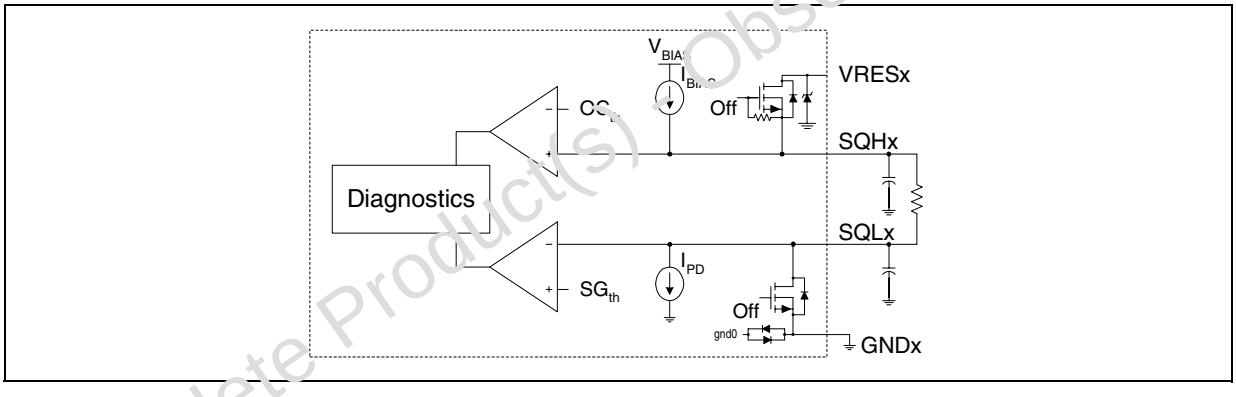
Figure 17. Short-to-Battery Diagnostic Diagram



4.12 Open Circuit and Short to Ground Diagnostic

During an open circuit or a short to ground test, a current source referenced to V_{DIAG_BIAS} is connected to the SQHx. When no open circuit or short to ground condition exists, SQHx and SQLx are equal to V_{DIAG_BIAS}. An open circuit fault is detected when SQHx voltage is at V_{DIAG_BIAS} and the SQLx voltage is at ground potential. A short to ground is detected when SQLx voltage is at ground potential and the SQHx voltage is below the open circuit threshold, OC_{th}.

Figure 18. Open Circuit and Short to Ground Diagnostic Diagram



The open circuit and short to ground conditions are summarized in the table below. A fault condition exists for at least t_{FH_DLY} before OSD sets the respective fault bit.

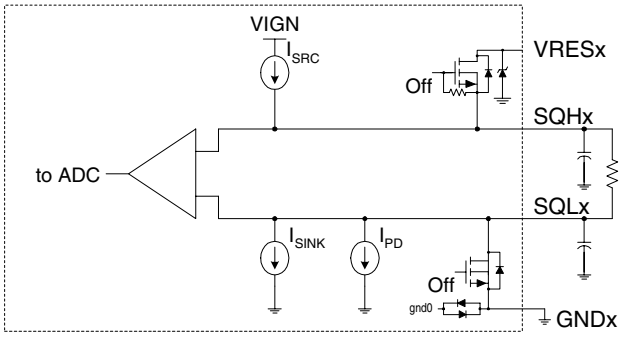
Table 9. Open Circuit / Short to Ground Fault Condition

Comparator Output		Condition
OC	SG	
0	0	Invalid State
0	1	Short to Ground
1	0	Normal operation
1	1	Open Circuit

4.13 Resistance Measurement

In a resistance measurement test, OSD provides a current source, ISRC, on SQHx and a current sink, ISINK, on SQLx. The 8-bit ADC is multiplexed between the deployment loops. This ADC converts the voltage across the SQHx and SQLx. The conversion results is stored for SPI retrieval. Figure 19 shows the resistance measurement diagram.

Figure 19. Resistance Measurement Diagram



The ADC has a resolution of 8 bits and an accuracy of 5%. The ADC is robust to disruption that may occur due to adjacent loops short to 40V or -1V.

4.14 MOS Diagnostic

During a MOS test, the I_{BIAS} current source referenced to V_{BIAS} is connected to the SQHx. In case of normal condition, SQHx and SQLx are equal to V_{BIAS}.

DEPEN pin is asserted in order to run a MOS diagnostic. If DEPEN pin is negated, OSD will inhibit the high/low side MOS from turning on. In this case, the MOS diagnostic is terminated after t_{DETECT} is expired and the respective MOS fault bit is set.

4.15 Low Side MOS Diagnostic

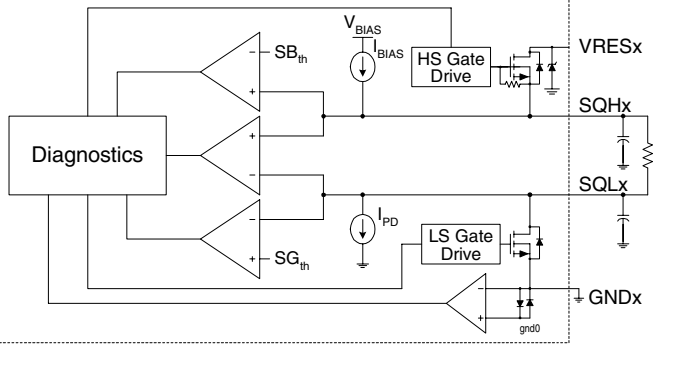
Upon detection of the following conditions, OSD turns the low side driver off and terminates the diagnostic within the specified time, tPROP_DLY.

- V_{SQL} is less than SGth threshold voltage
- (V_{SQHx} - V_{SQLx}) is greater than V_{th}
- V_{SQH} is greater than SB_{th} threshold voltage

Any of the above conditions are considered as a normal operation. Upon detection any of these conditions, OSD does not set the low side driver fault bits.

On a single channel, high-side and low-side MOS diagnostics is completed within t_{DETECT}. A low-side MOS fault bit is only set when t_{DETECT} is expired before any of the above conditions are detected. A fault detection filter, t_{FLT_DLY}, is provided to protect against short-transients on SQH and SQL pins. See Figure 20 for MOS test diagram.

Figure 20. MOS Diagnostic Diagram



4.16 High Side MOS Diagnostic

Upon detection of the following conditions, OSD turns the high side driver off and terminate the diagnostic within the specified time, t_{PROP_DLY}.

- V_{SQH} is greater than SBth threshold voltage
- (V_{SQHx} - V_{SQLx}) is greater than V_{I_TH}
- V_{SQL} is less than SG_{th} threshold voltage

Any of the above conditions are considered as a normal operation. Upon detection any of these conditions, OSD does not set the high side driver fault bits.

On a single channel, high-side and low-side MOS diagnostics are completed within t_{DETECT}. A high-side MOS fault bit is only set when t_{DETECT} is expired before any of the above conditions are detected. A fault detection filter, t_{FLT_DLY}, is provided to protect against short-transients on SQH and SQL pins. See Figure 20 for MOS test diagram.

4.17 Loss of Ground Diagnostic

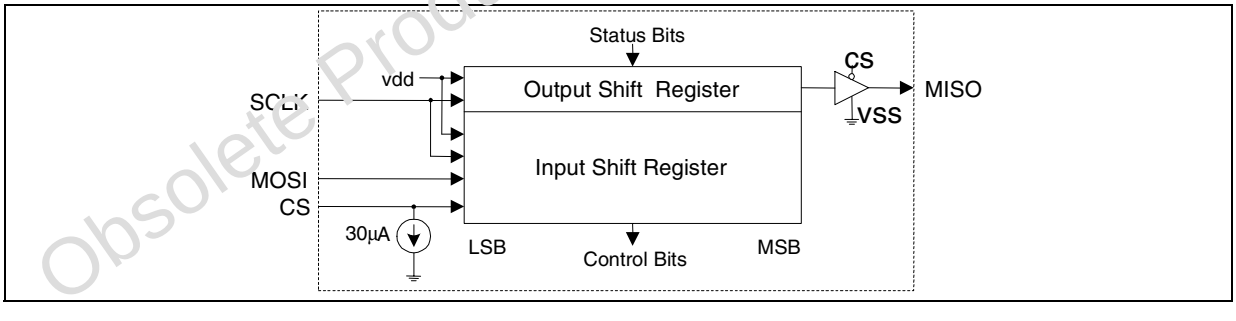
Loss of ground is detected when the power ground of a deployment loop has a high impedance/open connection to the ground. Each channel has a dedicated power ground and a dedicated loss of ground detection. Upon a detection of loss of ground condition, OSD inhibits a diagnostic and a deployment for the respective channel. The rest of the channels are not affected by a loss of ground condition on the other channels. A loss of ground condition does not affect a deployment or a pulse stretch timer that is already started.

A ground reference for OSD logic is connected to GND0 pin. When OSD detects a high impedance on this ground reference, OSD will go in reset mode.

4.18 Serial Peripheral Interface (SPI)

The OSD contains a serial peripheral interface consisting of Serial Clock (SCLK), Serial Data Out (MISO), Serial Data In (MOSI), and Chip Select (CS). This device is configured as an SPI slave.

Figure 21. SPI Block Diagram



4.19 Chip Select (CS)

The CS input selects OSD for serial data transfers. This TTL-compatible input has an internal pull-down to command the de-asserted state should an open circuit condition occur When CS is asserted, the MISO pin is released from tri-state mode, and all status information is latched in the SPI shift register. While CS is asserted, register data is shifted in the MOSI pin and shifted out the MISO pin on each subsequent SCLK. When CS is negated, the MISO pin is tri-stated and the fault register reloaded (latched) with the current filtered status data.

To allow sufficient time to reload the fault registers; the CS pin must remain negated for at least t_{CSN}. CS must also be immune to spurious pulses as defined in the SPI Timing table (MISO may come out of tri-state, but no status bits can be cleared and no control bits altered). Glitches on the CS line while SCLK is not running will be ignored, although the MISO pin may be enabled. In each valid CS, OSD allows 16-bit

SPI transfer. OSD ignores all SPI transfers, which are not a 16-bit transfer and issue a SPI fault response in the next valid CS.

4.20 Serial Clock (SCLK)

The SCLK input is the clock signal input for synchronization of serial data transfer. This pin has TTL level compatible input voltages allowing proper operation with microprocessors using a 3.3 to 5.0 volt supply.

When CS is asserted, both the SPI master and this device latch input data on the rising edge of SCLK. The SPI master typically shifts data out on the falling edge of SCLK, as does this device.

4.21 Serial Data Output (MISO)

The MISO output pin is in a tri-state condition when CS is negated. When CS is asserted, the MSB is the first bit of the word transmitted on MISO and the LSB is the last bit of the word transmitted on MISO. This pin supplies a "rail to rail" output, so if interfaced to a microprocessor that is using a lower VDD supply, the appropriate microprocessor input pin shall not sink more than IOH and shall not clamp the MISO voltage to less than $V_{OH(min)}$ while the MISO pin is in a logic "1" state.

4.22 Serial Data Input (MOSI)

The MOSI input takes data from the master microprocessor while CS is asserted. The MSB is the first bit of each word received on MOSI and the LSB is the last bit of each word received on MOSI. This pin has TTL level compatible input voltages allowing proper operation with micro-processors using a 3.3 to 5.0 volt supply.

4.23 SPI Transmission

The SPI provides access to read/write to the registers internal to OSD. OSD responses to various commands summarized in the below table. OSD response to the previous command is sent in the next valid CS.

Table 10. OSD SPI Response

Mode Bits		MOSI Command	Mode Bits		MISO Response
D15	D14		D15	D14	
0	0	Register Mode	0	0	Register Mode
0	1	Command Mode	0	1	Command Mode
1	0	Diagnostic Mode	1	1	Status Response
1	1	Monitor Mode	1	1	Status Response
X	X	SPI Transmission Fault	1	0	SPI Fault Response

4.24 SPI Bit Definition - MOSI Bit

Figure 22. MOSI Bit Layout

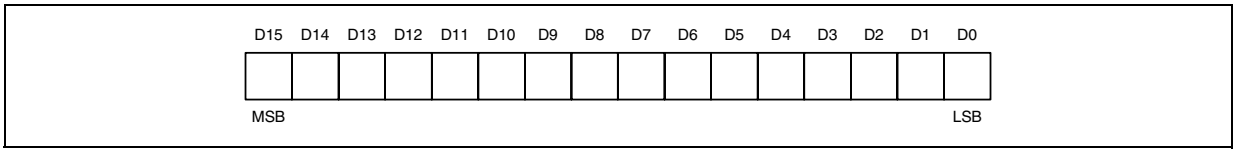


Table 11. MOSI Mode Bits Definition

Bit D15	Bit D14	Description
0	0	Register Mode
0	1	Command Mode
1	0	Diagnostic Mode
1	1	Monitor Mode

4.25 Register Mode

Register mode message is defined as shown in table below.

Table 12. MOSI Register Mode Message Definition

Bit	State	Description
D15	0	Mode Bits
D14	0	
D13	0	Read Configuration Register
	1	Write Configuration Register
D12		Address-bit
D11		
D10		
D9		
D8		
D7		Data-bit
D6		
D5		
D4		
D3		
D2		
D1		
D0		

When bit D13 is set to '1,' OSD writes the data-bit to its internal register. The address bit desig-nates a specific register in OSD. This address-bit is defined as shown below.

When the ADC resistance measurement is addressed, OSD ignores the data-bit. Upon the detection of this ADC resistance measurement on the address-bit, OSD sends the 8-bit resistance measurement value in the register mode response.

A write request contains valid mode bits, bit D13 set to '1,' valid address bits and valid data bits. In the next valid CS, a register mode response contains the valid register content and not the echo from previous command.

A read request contains valid mode bits, bit D13 set to '0,' and valid address bits. The data bits will be ignored by the OSD. In the next valid CS, a register mode response contains a valid register content. This register is determined by the address bits sent in the previous command.

Table 13. Address-bit Definition

Bit D12	Bit D11	Bit D10	Bit D9	Bit D8	Description
RES	**ADC**	**DIAG**	**AD1**	**AD0**	**Program Other Options**
0	0	0	0	0	STATUS.FLT Configuration Register
0	0	0	0	1	Deployment Configuration 1 Register
0	0	0	1	0	Deployment Configuration 2 Register
0	0	0	1	1	Soft Reset
RES	**ADC**	**DIAG**	**AD1**	**AD0**	**Diagnostic Fault Registers**
0	0	1	0	0	Channel 0 and 1 Register (see table 18)
0	0	1	0	1	Channel 2 and 3 Register, Table 19
0	0	1	1	0	Channel 4 and 5 Register (see table 20)

Table 13. Address-bit Definition (continued)

Bit D12	Bit D11	Bit D10	Bit D9	Bit D8	Description
0	0	1	1	1	Channel 6 and 7 Register, Table 21
RES	**ADC**	**AD2**	**AD1**	**AD0**	**ADC Resistance Measurement Result**
0	1	0	0	0	8-bit ADC Measurement Register: Ch 0
0	1	0	0	1	8-bit ADC Measurement Register: Ch 1
0	1	0	1	0	8-bit ADC Measurement Register: Ch 2
0	1	0	1	1	8-bit ADC Measurement Register: Ch 3
0	1	1	0	0	8-bit ADC Measurement Register: Ch 4
0	1	1	0	1	8-bit ADC Measurement Register: Ch 5
0	1	1	1	0	8-bit ADC Measurement Register: Ch 6
0	1	1	1	1	8-bit ADC Measurement Register: Ch 7

4.26 STATUS.FLT Configuration Register

STATUS.FLT register is defined as shown in the below table. The setting of these registers will influence the diagnostic fault indication flag in the status response. If any of these bits set to '1' OSD inhibits the faults of the respective channels from affecting bit D13 (diagnostic fault flag) in the MISO Status Response. This STATUS.FLT configuration register does not afftect the operation of diagnostic fault registers.

Table 14. STATUS.FLT Configuration Register

Bit	Status	Description
D7	0	Enable Fault Report on Channel 7 (default)
	1	Disable Fault Report on Channel 7
D6	0	Enable Fault Report on Channel 6 (default)
	1	Disable Fault Report on Channel 6
D5	0	Enable Fault Report on Channel 5 (default)
	1	Disable Fault Report on Channel 5
D4	0	Enable Fault Report on Channel 4 (default)
	1	Disable Fault Report on Channel 4
D3	0	Enable Fault Report on Channel 3 (default)
	1	Disable Fault Report on Channel 3
D2	0	Enable Fault Report on Channel 2 (default)
	1	Disable Fault Report on Channel 2
D1	0	Enable Fault Report on Channel 1 (default)
	1	Disable Fault Report on Channel 1
D0	0	Enable Fault Report on Channel 0 (default)
	1	Disable Fault Report on Channel 0

4.27 Deployment Configuration Register 1

The deployment configuration register 1 is defined as shown in the next table. During a deployment event, a write request to this register is inhibited.

Table 15. Deployment Configuration Register 1

Bit	Status	Description
D7		Pulse Stretch timer (see table)
D6		
D5	0	ARM Parallel Mode (default)
	1	ARM Serial Mode
D4	-	Don't Care
D3	0	ARM67 Pulse Stretch Disable (default)
	1	ARM67 Pulse Stretch Enable
D2	0	ARM45 Pulse Stretch Disable (default)
	1	ARM45 Pulse Stretch Enable
D1	0	ARM23 Pulse Stretch Disable (default)
	1	ARM23 Pulse Stretch Enable
D0	0	ARM01 Pulse Stretch Disable (default)
	1	ARM01 Pulse Stretch Enable

Bit D3 through bit D0 is used to inhibit the ARMx signal from initiating the pulse stretch timer. When these bits are "0," ARMx signal is prohibited from initiating the timer. Otherwise, a valid ARMx signal starts the timer. If the timer has already initiated by the SPI deployment command, the ARMx signal does not affect the timer.

Bit D7 and bit D6 is used to set the period of pulse stretch timer. OSD has 8 independent timers for each channel. Either a valid ARMx or a SPI deployment command is capable to start the pulse stretch timer. These bits set the timer duration according to table. These values are default to %00 after battery connect.

Table 16. Pulse Stretch Timer

Bit D7	Bit D6	Stretch Period (ms)
0	0	7.5
0	1	15
1	0	30
1	1	60

4.28 Deployment Configuration Register 2

The second deployment configuration register contains bits to configure the deployment period and the deployment current for each loop. During a deployment event, a write request to this register is inhibited. The register is defined as shown in herebelow table.

Table 17. Deployment Configuration Register 2

Bit	Status	Description
D7	0	Channel 6/7 2ms Deployment Period (default)
	1	Channel 6/7 4ms Deployment Period
D6	0	Channel 6/7 1.2A Deployment Current (default)
	1	Channel 6/7 1.75A Deployment Current
D5	0	Channel 4/5 2ms Deployment Period (default)
	1	Channel 4/5 4ms Deployment Period
D4	0	Channel 4/5 1.2A Deployment Current (default)
	1	Channel 4/5 1.75A Deployment Current
D3	0	Channel 2/3 2ms Deployment Period (default)
	1	Channel 2/3 4ms Deployment Period
D2	0	Channel 2/3 1.2A Deployment Current (default)
	1	Channel 2/3 1.75A Deployment Current
D1	0	Channel 0/1 2ms Deployment Period (default)
	1	Channel 0/1 4ms Deployment Period
D0	0	Channel 0/1 1.2A Deployment Current (default)
	1	Channel 0/1 1.75A Deployment Current

4.29 Soft Reset

The soft reset in OSD is achieved by writing $AA and $55 within two subsequent 16-bit SPI transmissions. If the sequence is broken, the processor will be required to re-transmit the sequence. OSD is not in reset if the sequence is not completed within two subsequent 16-bit SPI transmissions.

4.30 Diagnostic Fault Registers

These diagnostic fault registers contain the fault status for each of the channels.
Each register is cleared immediately after a SPI reading on that particular register.
The diagnostic fault registers is defined as shown here below:

Table 18. Diagnostic Fault Register: Channel 0 and 1

Bit	State	Description
D7	0	No Fault: Channel 1
	1	Fault Exists: Channel 1
D6		Channel 1 Diagnostic Fault-bit Refer to Diagnostic Fault-bit Definition table 22
D5		
D4		
D3	0	No Fault: Channel 0
	1	Fault Exists: Channel 0
D2		Channel 0 Diagnostic Fault-bit Refer to Diagnostic Fault-bit Definition table 22

Table 19. Diagnostic Fault Register: Channel 2 and 3

Bit	State	Description
D7	0	No Fault: Channel 3
	1	Fault Exists: Channel 3
D6		Channel 3 Diagnostic Fault-bit Refer to Diagnostic Fault-bit Definition table 22
D5		
D4		
D3	0	No Fault: Channel 2
	1	Fault Exists: Channel 2
D2		Channel 2 Diagnostic Fault-bit Refer to Diagnostic Fault-bit Definition table 22

Table 20. Diagnostic Fault Register: Channel 4 and 5

Bit	State	Description
D7	0	No Fault: Channel 5
	1	Fault Exists: Channel 5
D6		Channel 5 Diagnostic Fault-bit Refer to Diagnostic Fault-bit Definition table 22
D5		
D4		
D3	0	No Fault: Channel 4
	1	Fault Exists: Channel 4
D2		Channel 4 Diagnostic Fault-bit Refer to Diagnostic Fault-bit Definition table 22

Table 21. Diagnostic Fault Register: Channel 2 and 3

Bit	State	Description
D7	0	No Fault: Channel 7
	1	Fault Exists: Channel 7
D6		Channel 7 Diagnostic Fault-bit Refer to Diagnostic Fault-bit Definition table 22
D5		
D4		
D3	0	No Fault: Channel 6
	1	Fault Exists: Channel 6
D2		Channel 6 Diagnostic Fault-bit Refer to Diagnostic Fault-bit Definition table 22

Diagnostic fault bit indicates short between loops, short to battery, open circuit, short to ground, high or low side MOS fault. The channel number is determined by the address bit in register mode command. These faults are decoded as shown in Diagnostic Fault-bit Definition table. Bit D7 and bit D3 indicate if a fault condition exists in the respective channels. Loss of ground fault has the highest priority among all fault conditions.

Table 22. Diagnostic Fault-bit Definition

D6/D2	D5/D1	D4/D0	Description
0	0	0	No Fault
0	0	1	Short Between Loops
0	1	0	Short to Battery
0	1	1	Open Fault
1	0	0	Short to Ground
1	0	1	Low Side MOS Fault
1	1	0	High Side MOS Fault
1	1	1	Loss of Ground Fault

4.31 Resistance Measurement Registers

OSD has 8 independent resistance measurement registers. The resistance measurement registers is defined as shown in the table.

Table 23. ADC Resistance Measurement Register

Bit	Description
D7	8-bit ADC Resistance Measurement Result
D6	
D5	
D4	
D3	
D2	
D1	
D0	

ADC resistance measurement registers contain the measurement results of each of the OSD deployment channels. The channel number is determined by the address bit in diagnostic command (see Address bit definition table 13)

4.32 Command Mode

Command Mode message is defined as shown in next table.

Table 24. MOSI Command Mode Message Definition

Bit	State	Description
D15	0	Mode Bits
D14	1	
D13		Odd Parity
D12	-	Don’t Care
D11	-	Don’t Care
D10	-	Don’t Care
D9	-	Don’t Care
D8	-	Don’t Care
D7	0	Channel 7 Idle
	1	Deploy Channel 7
D6	0	Channel 6 Idle
	1	Deploy Channel 6
D5	0	Channel 5 Idle
	1	Deploy Channel 5
D4	0	Channel 4 Idle
	1	Deploy Channel 4
D3	0	Channel 3 Idle
	1	Deploy Channel 3
D2	0	Channel 2 Idle
	1	Deploy Channel 2
D1	0	Channel 1 Idle
	1	Deploy Channel 1
D0	0	Channel 0 Idle
	1	Deploy Channel 0

Odd parity check includes all 16 bits. "Don't care" bit is included in the parity check as well.

Bit D7 to bit D0 is used to start the deployment or the pulse stretch timer. OSD provides an independent timer for each channel. When any of these bits are set to '1,' OSD starts the deployment of the pulse stretch timer for the respective channels. If any of these bits are set to '0' when the pulse stretch timer is still active, OSD terminates the pulse stretch timer for the respective channels. Once deployment is initiated it will not be terminated. During the deployment, OSD will ignore all commands.

When DEPEN is negated, OSD ignores the deploy command. In other words, OSD will not initiate the pulse stretch timer or a deployment in this condition. However, when the pulse stretcher is already started by a deploy command, DEPEN will not terminate the pulse stretch timer. Upon receiving an idle command, OSD will terminates the pulse stretch timer regardless of DEPEN signal. In this case, only a pulse stretch timer that is started by a deploy command that can be terminated by sending an idle command.

4.33 Diagnostic Mode

Diagnostic Mode message is defined as shown in table.

Table 25. MOSI Diagnostic Mode Message Definition

Bit	State	Description
D15	1	Mode Bits
D14	0	
D13		Odd Parity
D12	0	Read Status Response Only
	1	Run On-chip Diagnostic
D11	-	Don’t Care
D10	-	Don’t Care
D9	0	Short Between Loops Test Disable
	1	Short Between Loops Test Enable
D8	0	MOS Test Disable
	1	MOS Test Enable
D7	0	Disable Channel 7 Diagnostic
	1	Enable Channel 7 Diagnostic
D6	0	Disable Channel 6 Diagnostic
	1	Enable Channel 6 Diagnostic
D5	0	Disable Channel 5 Diagnostic
	1	Enable Channel 5 Diagnostic
D4	0	Disable Channel 4 Diagnostic
	1	Enable Channel 4 Diagnostic
D3	0	Disable Channel 3 Diagnostic
	1	Enable Channel 3 Diagnostic
D2	0	Disable Channel 2 Diagnostic
	1	Enable Channel 2 Diagnostic
D1	0	Disable Channel 1 Diagnostic
	1	Enable Channel 1 Diagnostic
D0	0	Disable Channel 0 Diagnostic
	1	Enable Channel 0 Diagnostic

Odd parity check includes all 16 bits. "Don't care" bit is included in the parity check as well.

When bit D12 is set to '1,' OSD starts its internal diagnostics on any channels selected in bit D7 through bit D0. When any of bit D7 through bit D0 are set to '1,' OSD performs diagnostics on the respective channels. The diagnostic sequence is shown in Figure 10. When bit D12 is set to '0,' OSD ignores bit D9 through bit D0.

Bit D9 and bit D8 are utilized to control the short between loops and MOS tests. If any of these bits are set to '1,' OSD performs the respective tests to any channels as selected in bit D7 thorugh bit D0. OSD executes these tests based on the diagnostic flow chart, shown in Figure 15.

4.34 Monitor Mode

Monitor Mode message is defined as shown in below:

Table 26. MOSI Monitor Mode Message Definition

Bit	State	Description
D15	1	Mode Bits
D14	1	
D13		Odd Parity
D12	0	Read Status Response Only
	1	Write Commands
D11	-	Don't Care
D10	-	Don't Care
D9	0	Do not modify Short Between Loops Test
	1	Modify Short Between Loops Test
D8	0	Disable Short Between Loops Test
	1	Enable Short Between Loops Test
D7	0	Keep Deploy Success Flag Channel 7
	1	Clear Deploy Success Flag Channel 7
D6	0	Keep Deploy Success Flag Channel 6
	1	Clear Deploy Success Flag Channel 6
D5	0	Keep Deploy Success Flag Channel 5
	1	Clear Deploy Success Flag Channel 5
D4	0	Keep Deploy Success Flag Channel 4
	1	Clear Deploy Success Flag Channel 4
D3	0	Keep Deploy Success Flag Channel 3
	1	Clear Deploy Success Flag Channel 3
D2	0	Keep Deploy Success Flag Channel 2
	1	Clear Deploy Success Flag Channel 2
D1	0	Keep Deploy Success Flag Channel 1
	1	Clear Deploy Success Flag Channel 1
D0	0	Keep Deploy Success Flag Channel 0
	1	Clear Deploy Success Flag Channel 0

Odd parity check includes all 16 bits. "Don't care" bit is included in the parity check as well.

When bit D12 is set to a '0,' OSD ignores all command bits, specified in bit D9 to bit D0.

The monitor mode message is allowed to start or to stop the short between loops test. To start the test, both bit D9 and bit D8 has to be set to '1.' To stop the test, bit D9 is set to '1' and bit D8 is set to '0.' If bit D9 is set to '0,' OSD ignores the state of bit D8. In this condition, OSD does not affect the test. If bit D12 is set to '0,' OSD ignores bit D9 and bit D8.

Bit D7 through bit D0 is used to clear/keep the deploy success flag. When these bits are set to '1,' the flag is cleared. Otherwise, OSD does not affect the state of these flags.

4.35 MISO Bit Definition

Figure 23. MISO Bit Layout

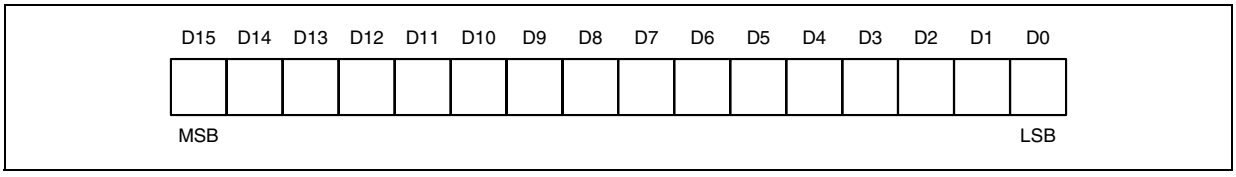


Table 27. MISO Mode Bits Definition

Bit D15	Bit D14	Description
0	0	Register Mode Response
0	1	Command Mode Response
1	0	SPI Fault Response
1	1	Status Response

4.36 Register Mode Response

Register Mode Response is defined as shown in table.

Table 28. MISO Register Mode Response Definition

Bit	State	Description
D15	0	Mode Bits
D14	0	
D13		Echo of MOSI Read/Write Bit
D12		Address Bits Refer to Address-bit Definition table
D11		
D10		
D9		
D8		
D7		Data Bits
D6		
D5		
D4		
D3		
D2		
D1		
D0		

Bit D13 is used to reflect the status of MOSI Read/Write bit (refer to bit D13 in "MOSI Register Mode Message Definition table").

Bit D7 through bit D0 contain data bits. These data bits contain either diagnostic fault register or ADC resistance measurement register depending upon the MOSI request. Both register are defined as shown in "Diagnostic Fault Register Channel 0 and 1 table" and "ADC Resistance Measurement Register table".

4.37 Command Mode Response

Command Mode Response defined as shown below.

Table 29. MISO Command Mode Response Definition

Bit	State	Description
D15	0	Mode Bits
D14	1	
D13	-	Don't Care
D12	0	DEPEN Negated
	1	DEPEN Asserted
D11	0	ARM67 Negated
	1	ARM67 Asserted
D10	0	ARM45 Negated
	1	ARM45 Asserted
D9	0	ARM23 Negated
	1	ARM23 Asserted
D8	0	ARM01 Negated
	1	ARM01 Asserted
D7		Deploy Channel 7 Status
D6		Deploy Channel 6 Status
D5		Deploy Channel 5 Status
D4		Deploy Channel 4 Status
D3		Deploy Channel 3 Status
D2		Deploy Channel 2 Status
D1		Deploy Channel 1 Status
D0		Deploy Channel 0 Status

DEPEN status flag indicates the state of DEPEN pin.

ARMx status flag indicates the state of the respective ARMx signal, including the pulse stretch timer. If the pulse stretch timer is initiated by a deployment command, it does not assert the ARMx status flag. This flag is de/asserted as soon as the de-glitch timer is expired.

Deploy status flag indicates the SPI deployment status for the respective channel. These flags reflect bit D7 through bit D0 of the most recent SPI command mode message. These bits do not include the status of pulse stretch timer. These bits will be overwritten by the most recent SPI command mode message. When DEPEN is negated, a valid deploy command is ignored and deploy status flag is not set.

4.38 SPI Fault Response

This SPI fault response indicates a fault in the last MOSI transmission. OSD uses the parity bit to determine the integrity of the MOSI command transmission.This response is defined as shown in table.

Table 30. MISO SPI Fault Response

Bit	State	Description
D15	1	Mode Bits
D14	0	
D13 – D0		Don't Care

4.39 Status Response

Status Response is the default response to the processor, and is defined as shown in table

Table 31. MISO Status Response Definition

Bit	State	Description
D15	1	Mode Bits
D14	1	
D13	0	No Diagnostic Fault
	1	Diagnostic Fault Exists
D12	0	Diagnostic not Complete
	1	Diagnostic Complete / Not Started
D11	0	ARM67 Negated
	1	ARM67 Asserted
D10	0	ARM45 Negated
	1	ARM45 Asserted
D9	0	ARM23 Negated
	1	ARM23 Asserted
D8	0	ARM01 Negated
	1	ARM01 Asserted
D7	0	No Deployment Event: Channel 7
	1	Deploy Command Successful: Channel 7
D6	0	No Deployment Event: Channel 6
	1	Deploy Command Successful: Channel 6
D5	0	No Deployment Event: Channel 5
	1	Deploy Command Successful: Channel 5
D4	0	No Deployment Event: Channel 4
	1	Deploy Command Successful: Channel 4
D3	0	No Deployment Event: Channel 3
	1	Deploy Command Successful: Channel 3
D2	0	No Deployment Event: Channel 2
	1	Deploy Command Successful: Channel 2
D1	0	No Deployment Event: Channel 1
	1	Deploy Command Successful: Channel 1
D0	0	No Deployment Event: Channel 0
	1	Deploy Command Successful: Channel 0

Diagnostic fault indication flag indicates if a fault exists during the on-chip diagnostic. This bit reports the fault status on channel/s enabled in the STATUS.FLT configuration register.

Diagnostic completion status flag indicates if the on-chip diagnostic is completed. This flag will be set when all the requested channels finish the diagnostic sequence (see Figure 15). This flag does not include the status of "short between loops" test.

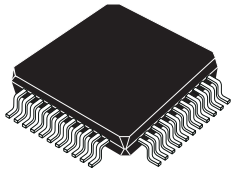
ARMx status flag indicates the state of the respective ARMx signal, including the pulse stretch timer. If the pulse stretch timer is initiated by a deployment command, it does not assert the ARMx status flag. This flag is de/asserted as soon as the de-glitch timer is expired.

Deploy command success bit indicates if the corresponding channel has finished its deployment sequence. This bit is set when deployment period, 2ms or 4ms, has expired. Once this bit is set, it inhibits the subsequent deployment command until OSD receives a SPI command to clear this deployment success flag. Refer to Figure 9, Figure 10, Figure 11, and Figure 12 for the operation of deployment success flag.

Figure 24. TQFP44 (10x10x1.4mm) Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0˚(min.), 3.5˚(typ.), 7˚(max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10 x 1.4mm)

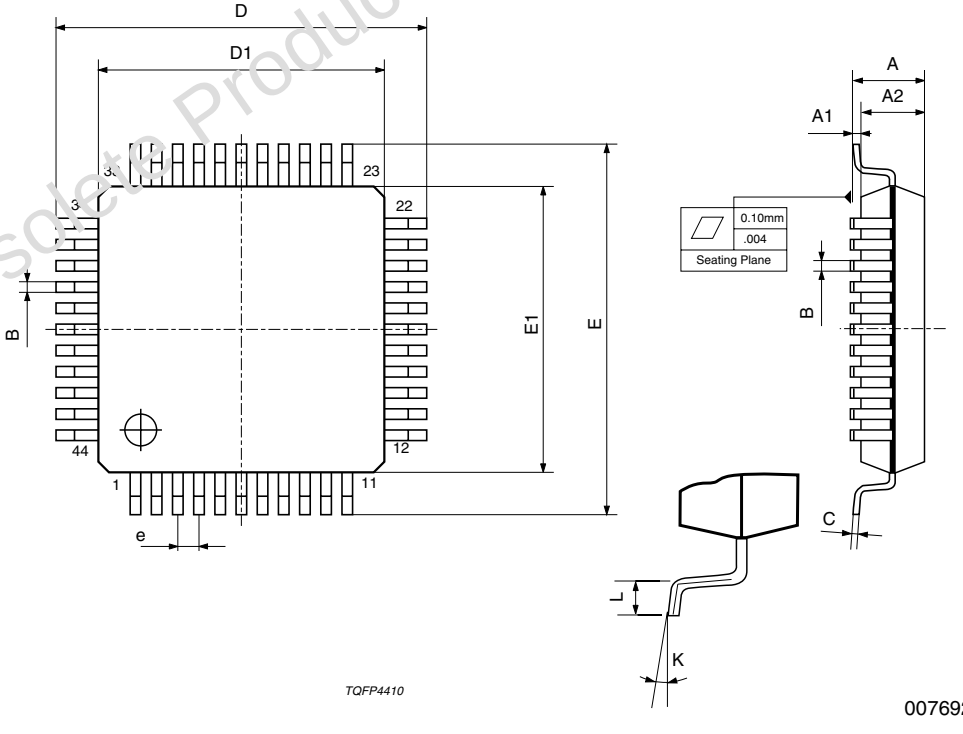


Table 32. Revision History

Date	Revision	Description of Changes
October 2004	1	First Issue