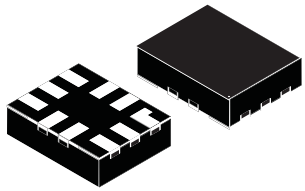
ST2329I

2-bit dual-supply level translator with auto-direction feature and integrated pull-up

Target specification

Features

- 18 Mbps (max.) data rate when driven by a totem pole driver
- 6.8 Mbps (max.) data rate when driven by an open drain pole driver
- Bidirectional level translation, without direction pin
- Wide V_L voltage range of 1.65 V to 3.6 V
- Wide V_{CC} voltage range of 1.80 V to 5.5 V
- Integrated 10 kΩ pull-up on both V_{CC} and V_L sides
- Power-down mode feature; when either supply is off, all I/Os are in high impedance
- Low quiescent current (max. 4 µA)
- Able to be driven by totem pole and open drain drivers
- 5.5 V tolerant enable pin
- ESD performance on all pins: ±2 kV HBM
- Small package and footprint - QFN10 (1.8 x 1.4 mm) package



QFN10 (1.8 x 1.4 mm)

Table 1. Device summary

Order code	Package	Packing
ST2329IQTR	QFN10 (1.8 x 1.4 mm)	Tape and reel (3000 parts per reel)

Applications

- Low voltage system level translation
- Mobile phones and other mobile devices
- I^2C level translation
- UART level translation

Contents

List of tables

List of figures

1 Description

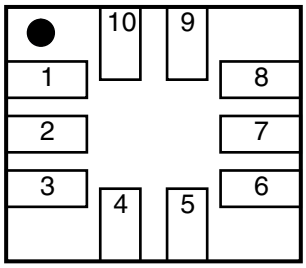
ST2329I is a 2-bit dual-supply level translator which provides the level shifting capability to allow data transfer in a multi-voltage system. Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. It utilizes a transmission gate based design that allows bidirectional level translation without a control pin.

The ST2329I accepts V_L from 1.65 V to 3.6 V and V_{CC} from 1.80 V to 5.5 V, making it ideal for data transfer between low-voltage ASICs/PLD and higher voltage systems. This device has a tri-state output mode which can be used to disable all the I/Os.

The ST2329I supports power-down mode when V_{CC} is grounded/floating and the device is disabled via the OE pin. The device has integrated 10 kΩ pull-ups on both sides.

2 Pin configuration

Figure 1. Pin configuration



QFN10L (top through view)

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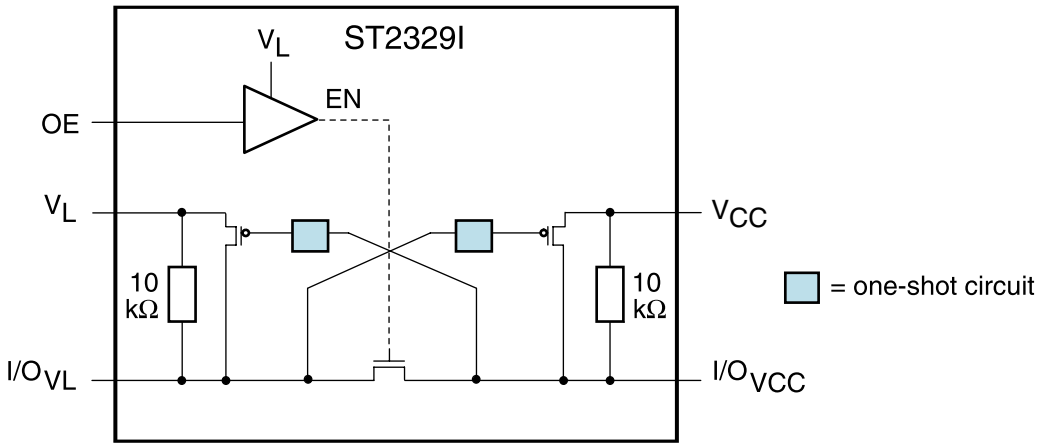
Table 2. Pin description

QFN10 pin no	Symbol	Name and function
1, 2	I/O_{VL1} to I/O_{VL2}	Data inputs/outputs
8, 7	I/O_{VCC1} to I/O_{VCC2}	Data inputs/outputs
3	OE	Output enable input
6	GND	Ground
10	V_L	Supply voltage
9	V_{CC}	Supply voltage
4, 5	NC	No connect

Figure 2. Device block diagram



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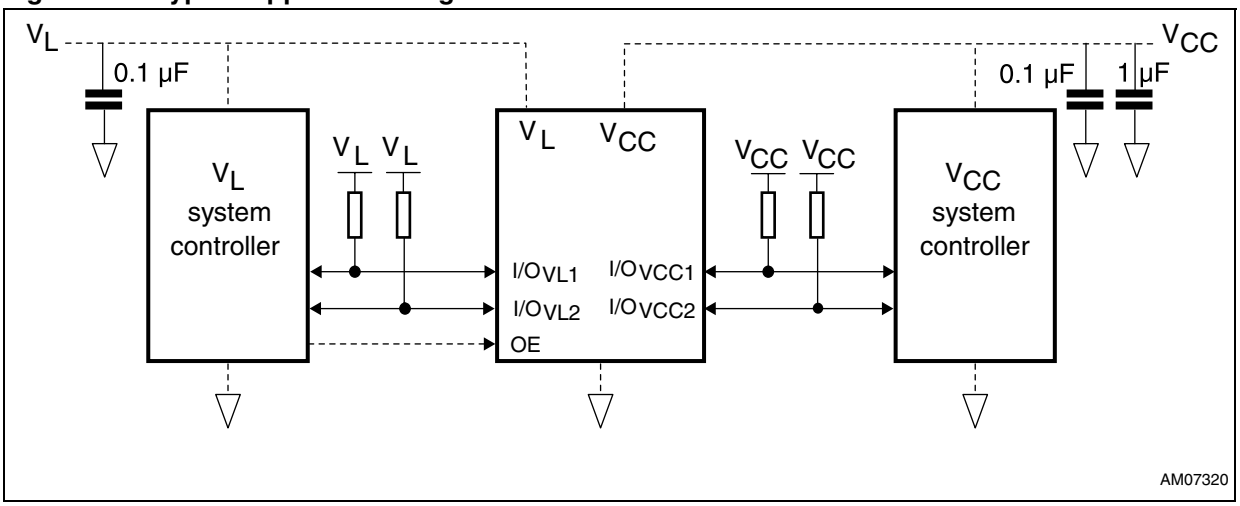
1. ST2329I has 2 channels. For simplicity, the diagram above shows only 1 channel.
2. When OE is LOW, all I/Os are in high impedance mode.

Figure 3. Typical application diagram



1. External pull-up resistors are optional. Only needed if a pull-up value lower than 10 kΩ is desired.

2.1 Supplementary notes

2.1.1 Driver requirements

The ST2329I may be driven by an open drain or totem pole driver and the nature of the device output is “open drain”. It must not be used to drive a pull-down resistor as the impedance of the output at HIGH state depends on the pull-up resistor placed at the I/Os.

As the device has pull-up resistors on both I/O_{VCC} and I/O_{VL} ports, the user needs to ensure that the driver is able to sink the required amount of current. For example, if the settings are V_{CC} = 5.5 V, V_L = 4.3 V, and the pull-up resistor is 10 kΩ, then the driver must be able to sink at least (5.5 V / 10 kΩ) + (4.3 V / 10 kΩ) ≈ 1 mA and still meet V_{IL} requirements of ST2329I.

2.1.2 Load driving capability

To support the open drain system, the one-shot transistor is turned on only during high transition at the output side. When it drives a high state, after the one-shot transistor turned off, only the pull-up resistor is able to maintain the state. In this case, the resistive load is not recommended.

2.1.3 Power-off feature

In some applications where it might be required to turn off one of the power supplies powering up the level translator, the user may turn OFF the V_{CC} only when the OE pin is low (device is disabled). There is no current consumption in V_L due to floating gates or other causes, and the I/Os are in a high impedance state in this mode.

Table 3. Truth table

Enable	Bidirectional input/output	
OE	I/O_{VCC}	I/O_{VL}
H(1)	H(2)	H(1)
H(1)	L	L
L	Z(3)	Z

1. High level V_L power supply referred.
2. High level V_{CC} power supply referred.
3. Z = high impedance.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_L	Supply voltage	–0.3 to 4.6	V
V_{CC}	Supply voltage	–0.3 to 6.5	V
V_{OE}	DC control input voltage	–0.3 to 6.5	V
$V_{I/OVL}$	DC I/O_{VL} input voltage (OE = GND or V_L)	–0.3 to V_L + 0.3	V
$V_{I/OVCC}$	DC I/O_{VCC} input voltage (OE = GND or V_L)	–0.3 to V_{CC} + 0.3	V
I_{IK}	DC input diode current	–20	mA
$I_{I/OVL}$	DC output current	±25	mA
$I_{I/OVCC}$	DC output current	±258	mA
I_{SCTOUT}	Short-circuit duration, continuous	40	mA
P_D	Power dissipation(1)	500	mW
T_{STG}	Storage temperature	–65 to 150	°C
TL	Lead temperature (10 seconds)	300	°C
ESD	Electrostatic discharge protection (HBM)	±2	KV

1. 500 mW: 65 °C derated to 300 mW by 10 mW/°C: 65 °C to 85 °C.

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_L	Supply voltage	1.65		3.6	V
V_{CC}(1)	Supply voltage	1.8		5.5	V
V_{OE}	Input voltage (OE output enable pin, V_L power supply referred)	0		3.6	V
$V_{I/OVL}$	I/O_{VL} voltage	0		V_L	V
$V_{I/OVCC}$	I/O_{VCC} voltage	0		V_{CC}	V
TOP	Operating temperature	–40		85	°C
dt/dV	Input rise and fall time	0		1	ns/V

1. V_{CC} must be greater than V_L.

Table 6. DC characteristics (over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25 °C)

Symbol	Parameter	Test conditions			Value					Unit
		V_L	V_{CC}		T_A = 25 °C			–40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IHL}	High level input voltage on V_L side (I/O_{VL})	1.65	V_L to 5.5	—	1.4			1.4		V
		2.0			1.6			1.6		
		2.5			2.0			2.0		
		3.0			2.4			2.4		
		3.6			2.8			2.8		
V_{ILL}	Low level input voltage on V_L side (I/O_{VL})	1.65	V_L to 5.5	—			0.3		0.3	V
		2.0					0.4		0.4	
		2.5					0.5		0.5	
		3.0					0.6		0.6	
		3.6					0.8		0.8	
V_{IHC}	High level input voltage on V_{CC} side (I/O_{VCC})	1.65 to V_{CC}	1.65	—		1.4		1.6		V
			2.0			1.6		2.3		
			2.5			2.3		2.7		
			3.0			2.7		3.3		
			3.6			3.3		3.5		
			5.5			4.2		4.2		
V_{ILC}	Low level input voltage on V_{CC} side (I/O_{VCC})	1.65 to V_{CC}	1.65	—			0.3			V
			2.0				0.3			
			2.5				0.3			
			3.0				0.5			
			3.6				0.5			
			5.5				0.5			
$V_{IH\text{-}OE}$	High level input voltage (OE)	1.65	V_L to 5.5	—	1.0			1.0		V
		2.0			1.2			1.2		
		2.5			1.4			1.4		
		3.0			1.6			1.6		
		3.6			2.0			2.0		

Table 6. DC characteristics (over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25 °C) (continued)

Symbol	Parameter	Test conditions			Value					Unit
		V_L	V_{CC}		T_A = 25 °C			–40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
V_{IL-OE}	Low level input voltage (OE)	1.65	V_L to 5.5	—			0.33		0.33	V
		2.0					0.40		0.40	
		2.5					0.50		0.50	
		3.0					0.60		0.60	
		3.6					0.75		0.75	
V_{OLL}	Low level output voltage (I/O_{VL})	1.65 to 3.6	V_L to 5.5	IO=1.0 mA $I/O_{VCC} \leq 0.15$ V			0.40		0.40	V
V_{OLC}	Low level output voltage (I/O_{VCC})	1.65 to 3.6	V_L to 5.5	IO=1.0 mA $I/O_{VL} \leq 0.15$ V			0.40		0.40	V
I_{OE}	Control input leakage current (OE)	1.65 to 3.6	V_L to 5.5	V_{OE} = GND or V_L			±0.1		±0.1	µA
I_{IO_LKG}	High impedance leakage current (I/O_{VL}, I/O_{VCC})	1.65 to 3.6	V_L to 5.5	OE = GND			±0.1		±0.1	µA
I_{QVCC}	Quiescent supply current V_{CC}	1.65 to 3.6	V_L to 5.5	Only pull-up resistor connected to I/O		3	3.5		6	µA
I_{QVL}	Quiescent supply current V_L	1.65 to 3.6	V_L to 5.5	Only pull-up resistor connected to I/O		0.01	0.1		1	µA
I_{Z-VCC}	High impedance quiescent supply current V_{CC}	1.65 to 3.6	V_L to 5.5	OE = GND; only pull-up resistor connected to I/O		3	3.5		6	µA
I_{Z-VL}	High impedance quiescent supply current V_L	1.65 to 3.6	V_L to 5.5	OE = GND; only pull-up resistor connected to I/O		0.01	0.1		1	µA

2.2 AC characteristics (device driven by open drain driver)

Table 7. For test conditions: V_L = 1.65 to 1.8 V (load C_L = 15 pF; R_{up} = 4.7 kΩ; driver $t_r = t_f \leq$ 2 ns) overtemperature range –40 °C to 85 °C

Symbol	Parameter		V_{CC} = 1.8 - 2.5 V		V_{CC} = 2.7 - 3.6 V		V_{CC} = 4.3 - 5.5 V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}			80		60		45	ns
t_{FVCC}	Fall time I/O_{VCC}			23.2		33.9		53.3	ns
t_{RVL}	Rise time I/O_{VL}			60		45		35	ns
t_{FVL}	Fall time I/O_{VL}			16.4		17.6		16.9	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}		3.4		2			ns
		t_{PLH}		13.9		19.1		30.2	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}		2		2		2.6	ns
		t_{PLH}		8.6		9		9.5	ns
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output enable and disable time	En		10		10		10	ns
		Dis		40		40		40	ns
D_R	Data rate(1)			1.8		2.2		3.4	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation is not less than 30%. Note that the R_{up} of 4.7 kΩ is an effective R pull-up value. Since the device has an integrated 10 kΩ pull-up resistor, an effective value of 4.7 kΩ is obtained by adding an external 8.9 kΩ pull-up resistor.

Table 8. For test conditions: V_L = 2.5 to 2.7 V (load C_L = 15 pF; R_{up} = 4.7 kΩ; driver $t_r = t_f \leq$ 2 ns) overtemperature range –40 °C to 85 °C

Symbol	Parameter		V_{CC} = 2.7 - 3.6 V		V_{CC} = 4.3 - 5.5 V		Unit
			Min.	Max.	Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}			70		50	ns
t_{FVCC}	Fall time I/OV_{VCC}			14.8		19.1	ns
t_{RVL}	Rise time I/O_{VL}			50		35	ns
t_{FVL}	Fall time I/O_{VL}			9.8		10	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}		2		2	ns
		t_{PLH}		8.2		11.6	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}		2		2	ns
		t_{PLH}		5.3		5.9	ns
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output enable and disable time	En		6		6	ns
		Dis		40		40	ns
D_R	Data rate(1)			2.2		3.0	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation is not less than 30%. Note that the R_{up} of 4.7 kΩ is an effective R pull-up value. Since the device has an integrated 10 kΩ pull-up resistor, an effective value of 4.7 kΩ is obtained by adding an external 8.9 kΩ pull-up resistor.

Table 9. For test conditions: V_L = 2.7 to 3.6 V (load C_L = 15 pF; R_{up} = 4.7 kΩ; driver $t_r = t_f \leq$ 2 ns) overtemperature range –40 °C to 85 °C

Symbol	Parameter		V_{CC} = 4.3 - 5.5 V		Unit
			Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}			55	ns
t_{FVCC}	Fall time I/O_{VCC}			17.2	ns
t_{RVL}	Rise time I/O_{VL}			40	ns
t_{FVL}	Fall time I/O_{VL}			9.7	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}		2	ns
		t_{PLH}		10.6	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}		2	ns
		t_{PLH}		4.8	ns
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output enable and disable time	En		6	ns
		Dis		40	ns
DR	Data rate(1)			3.0	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation is not less than 30%.
Note that the R_{up} of 4.7 kΩ is an effective R pull-up value. Since the device has an integrated 10 kΩ pull-up resistor, an effective value of 4.7 kΩ is obtained by adding an external 8.9 kΩ pull-up resistor.

2.3 AC characteristics (device driven by totem pole driver)

Table 10. For test conditions: V_L = 1.65 to 1.8 V (load C_L = 15 pF; R_{up} = 10 kΩ; driver $t_r = t_f \leq$ 2 ns) overtemperature range –40 °C to 85 °C

Symbol	Parameter		V_{CC} = 1.8 - 2.5 V		V_{CC} = 2.7 - 3.6 V		V_{CC} = 4.3 - 5.5 V		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}			7.2		4.6		1.4	ns
t_{FVCC}	Fall time I/O_{VCC}			23.2		33.9		53.3	ns
t_{RVL}	Rise time I/O_{VL}			5.9		5.7		5.5	ns
t_{FVL}	Fall time I/O_{VL}			16.4		17.6		16.9	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH}	t_{PLH}		5.5		4.1		3.6	ns
	I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}		13.9		19.1		30.2	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH}	t_{PLH}		4.5		3.9		3.6	ns
	I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}		8.6		9.0		9.5	ns
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output enable and disable time	En		10		10		10	ns
		Dis		40		40		40	ns
D_R	Data rate(1)			6.4		4.5		3.0	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation is not less than 30%. Note that the R_{up} of 4.7 kΩ is an effective R pull-up value. Since the device has an integrated 10 kΩ pull-up resistor, an effective value of 4.7 kΩ is obtained by adding an external 8.9 kΩ pull-up resistor.

Table 11. For test conditions: V_L = 2.5 to 2.7 V (load C_L = 15 pF; R_{up} = 10 kΩ; driver $t_r = t_f \leq$ 2 ns) overtemperature range –40 °C to 85 °C

Symbol	Parameter		V_{CC} = 2.7 - 3.6 V		V_{CC}= 4.3 - 5.5 V		Unit
			Min.	Max.	Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}			3.8		2.8	ns
t_{FVCC}	Fall time I/O_{VCC}			14.8		19.1	ns
t_{RVL}	Rise time I/O_{VL}			3.3		3.2	ns
t_{FVL}	Fall time I/O_{VL}			9.8		10.0	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH}	t_{PLH}		3.2		2.8	ns
	I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}		8.2		11.6	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH}	t_{PLH}		2.6		2.0	ns
	I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}		5.3		5.9	ns
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output enable and disable time	En		6		6	ns
		Dis		40		40	ns
DR	Data rate(1)			9		6.8	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation is not less than 30%. Note that the R_{up} of 4.7 kΩ is an effective R pull-up value. Since the device has an integrated 10 kΩ pull-up resistor, an effective value of 4.7 kΩ is obtained by adding an external 8.9 kΩ pull-up resistor.

Table 12. For test conditions: V_L = 2.7 to 3.6 V (load C_L = 15 pF; R_{up} = 10 kΩ; driver $t_r = t_f \leq$ 2 ns) overtemperature range –40 °C to 85 °C

Symbol	Parameter		V_{CC} = 4.3 - 5.5 V		Unit
			Min.	Max.	
t_{RVCC}	Rise time I/O_{VCC}			2.9	ns
t_{FVCC}	Fall time I/O_{VCC}			17.2	ns
t_{RVL}	Rise time I/O_{VL}			3.0	ns
t_{FVL}	Fall time I/O_{VL}			9.7	ns
$t_{I/OVL-VCC}$	Propagation delay time I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PHL}		2.7	ns
		t_{PHL}		10.6	ns
$t_{I/OVCC-VL}$	Propagation delay time I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PHL}		1.9	ns
		t_{PHL}		4.8	ns
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output enable and disable time	En		6	ns
		Dis		40	ns
D_R	Data rate(1)			7.2	MHz

1. The data rate is guaranteed based on the condition that the output I/O signal rise/fall time is less than 15% of the input I/O signal period; the input I/O signal is at 50% duty cycle and the output I/O signal duty cycle deviation is not less than 30%.
Note that the R_{up} of 4.7 kΩ is an effective R pull-up value. Since the device has an integrated 10 kΩ pull-up resistor, an effective value of 4.7 kΩ is obtained by adding an external 8.9 kΩ pull-up resistor.

Figure 4. Test circuit

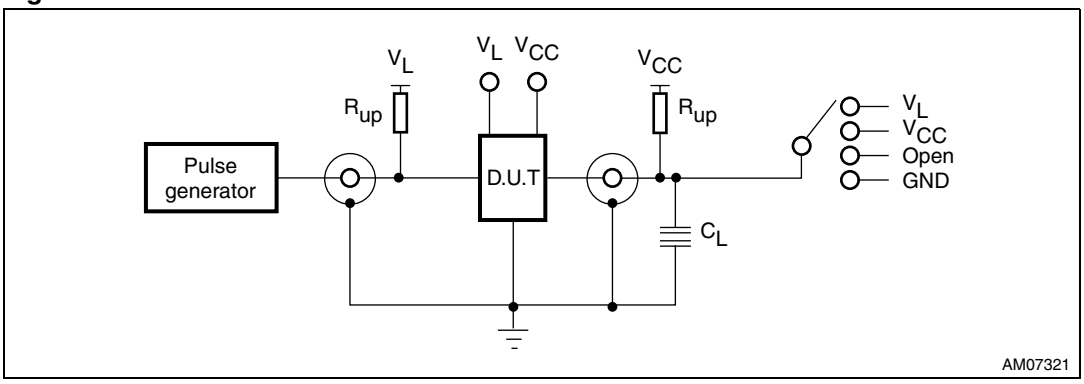


Table 13. Test circuit

Test	Switch		
	Driving I/O_{VL}	Driving I/O_{VCC}	Open drain driving
t_{PLH}, t_{PHL}	Open	Open	Open

Note: The pull-up resistors shown in the above test circuit are optional and are only needed if total pull-up on either end of the level translator needs to be lower than 10 kΩ. In applications where 10 kΩ is sufficient, the external pull-up resistor is not required.

Table 14. Waveform symbol value

Symbol	Driving I/O_{VL}		Driving I/O_{VCC}	
	1.8 V $\leq V_L \leq V_{CC} \leq$ 2.5 V	3.3 V $\leq V_L \leq V_{CC} \leq$ 5.0 V	1.8 V $\leq V_L \leq V_{CC} \leq$ 2.5 V	3.3 V $\leq V_L \leq V_{CC} \leq$ 5.0 V
V_{IH}	V_L	V_L	V_{CC}	V_{CC}
V_{IM}	50% V_L	50% V_L	50% V_{CC}	50% V_{CC}
V_{OM}	50% V_{CC}	50% V_{CC}	50% V_{CC}	50% V_{CC}
V_X	V_{OL} +15 V	V_{OL} +0.3 V	V_{OL} +0.15 V	V_{OL} +0.3 V
V_Y	V_{OH} –15 V	V_{OH} –0.3 V	V_{OH} –0.15 V	V_{OH} –0.3 V

Figure 5. Waveform - propagation delay (f = 1 MHz, 50% duty cycle)

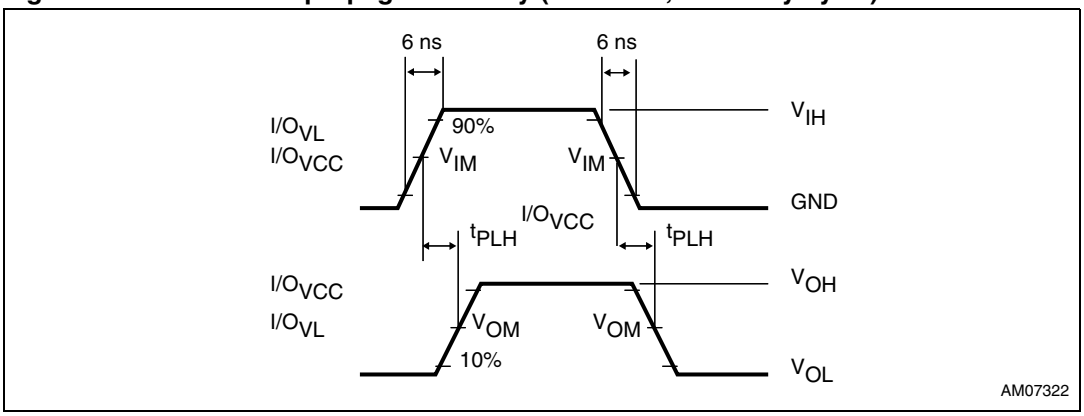
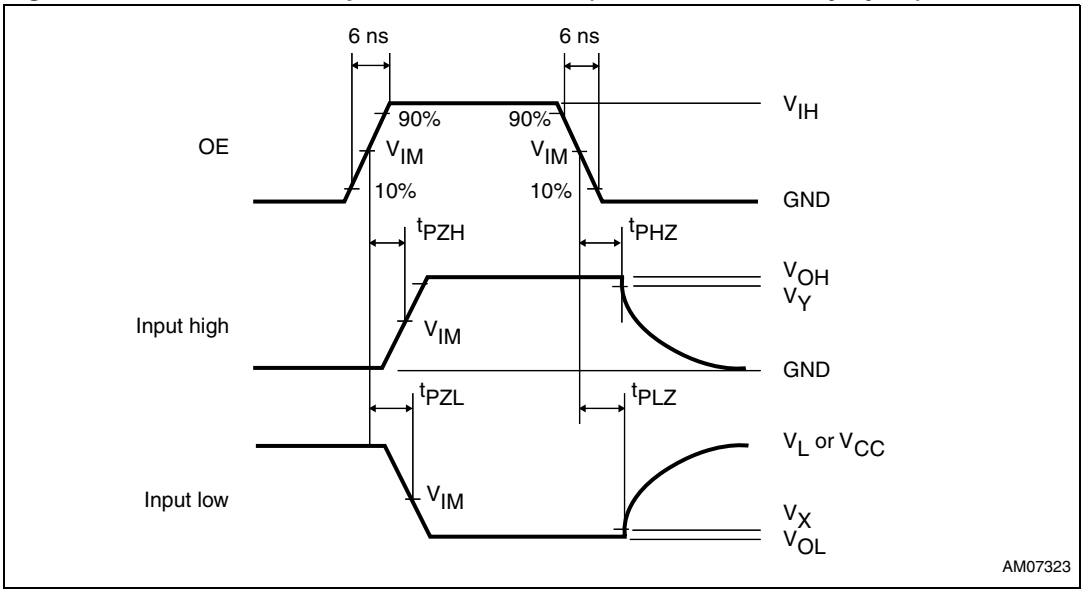


Figure 6. Waveform - output enable/disable (f = 1 MHz, 50% duty cycle)



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at *www.st.com*. ECOPACK is an ST trademark.

Figure 7. Package outline for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

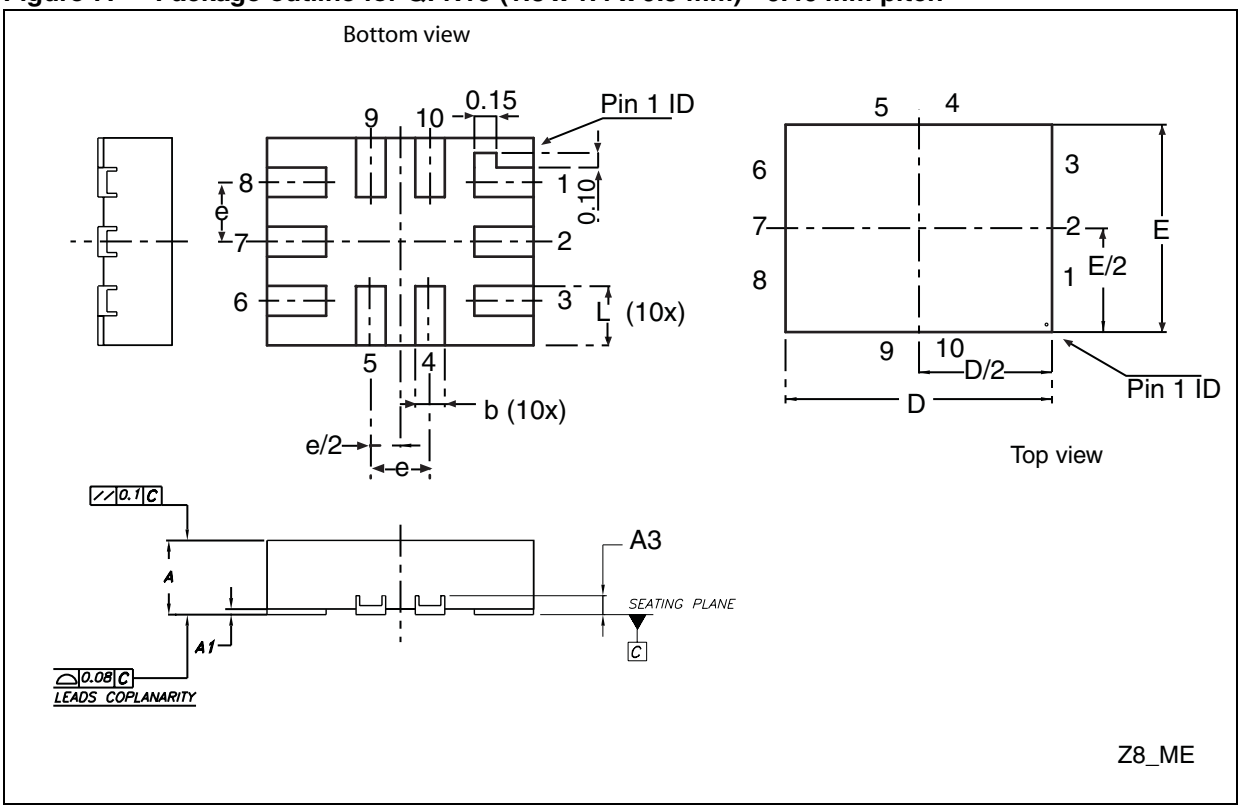


Table 15. Mechanical data for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

Symbol	millimeters			inches			Note
	Typ.	Min.	Max.	Typ.	Min.	Max.	
A	0.5	0.45	0.55	0.02	0.018	0.022	
A1	0.02	0	0.05	0.001	0	0.002	
A3	0.13			0.005			
b	0.2	0.15	0.25	0.008	0.006	0.01	
D	1.8	1.75	1.85	0.071	0.069	0.073	
E	1.4	1.35	1.45	0.055	0.053	0.057	
e	0.4			0.016			
L	0.4	0.35	0.45	0.016	0.014	0.018	

Figure 8. Footprint recommendation for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch

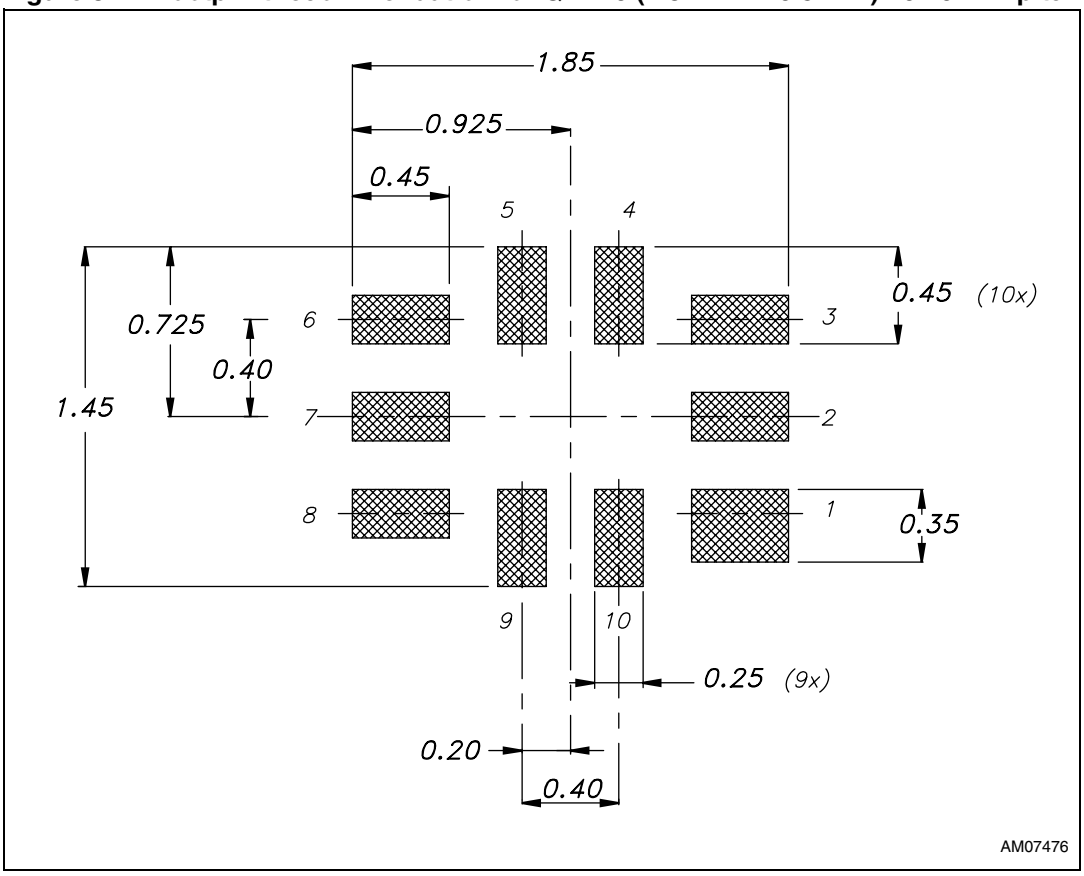
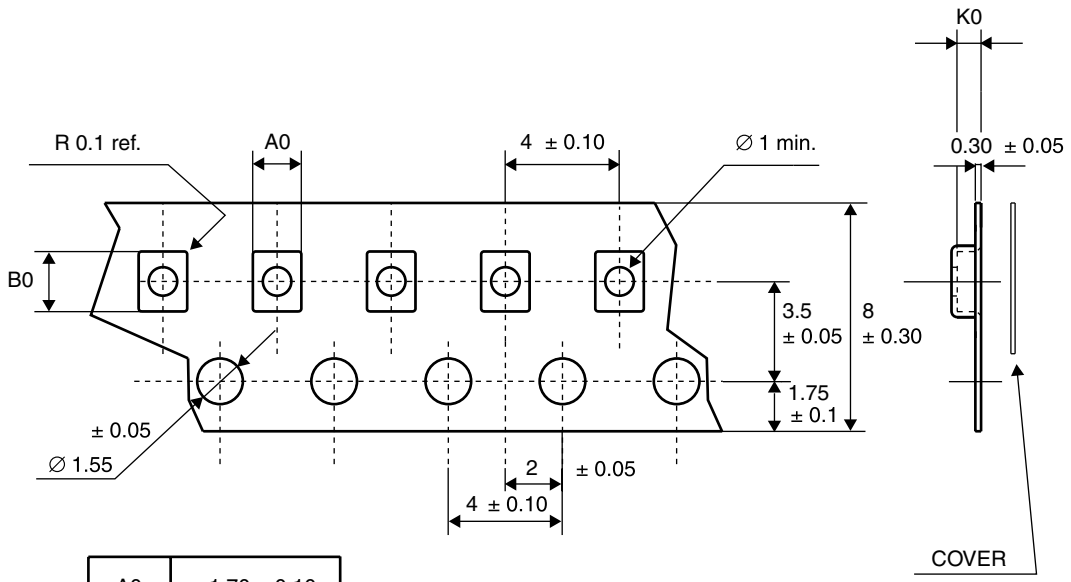


Figure 9. Carrier tape for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch



A0	1.70 ± 0.10
B0	2.10 ± 0.10
K0	0.70 ± 0.10

Figure 10. Reel information for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch - back view

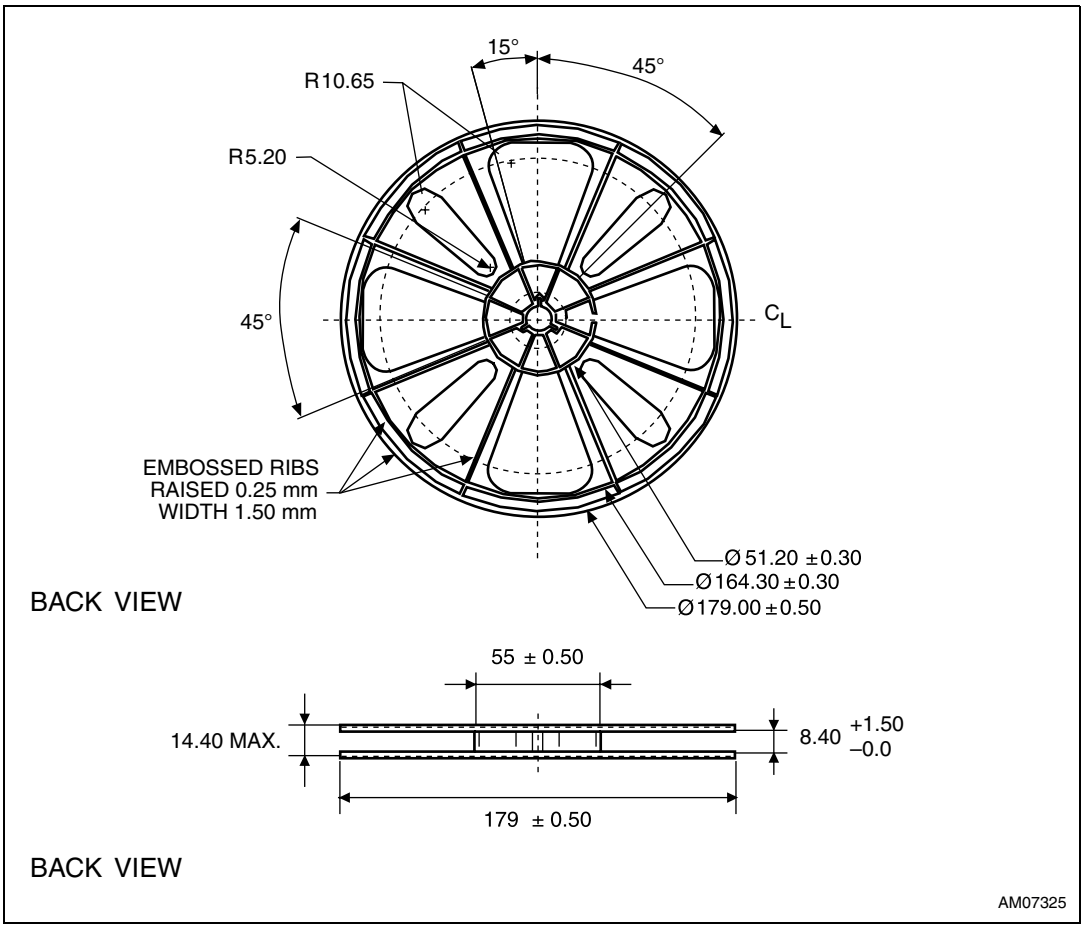
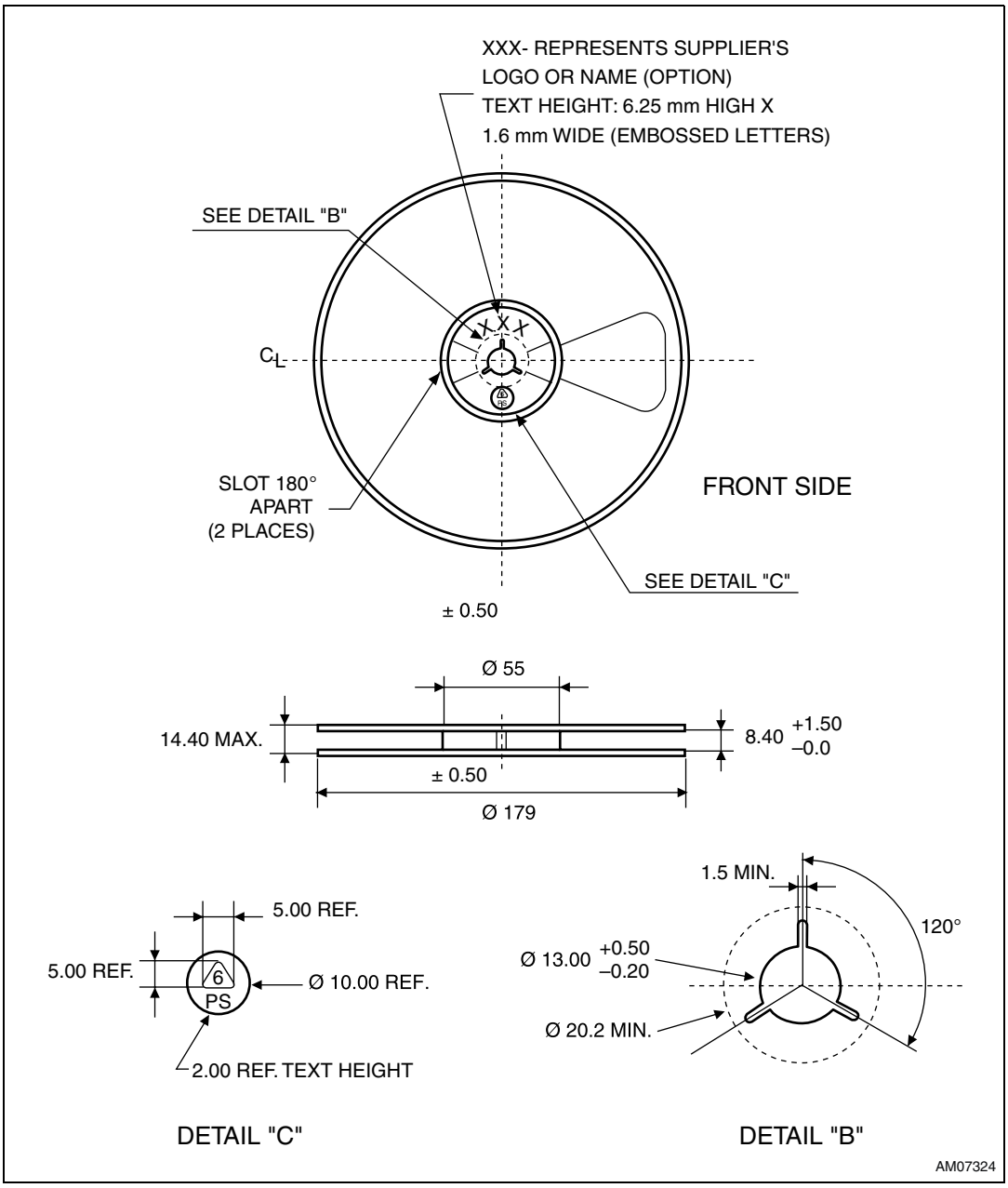


Figure 11. Reel information for QFN10 (1.8 x 1.4 x 0.5 mm) - 0.40 mm pitch - front view



4 Revision history

Table 16. Document revision history

Date	Revision	Changes
02-Mar-2011	1	Initial release.