

N-channel 600 V, 0.85 Ω typ., 7 A Zener-protected SuperFREDMESH™ Power MOSFET (with fast diode) in D²PAK

Datasheet - production data

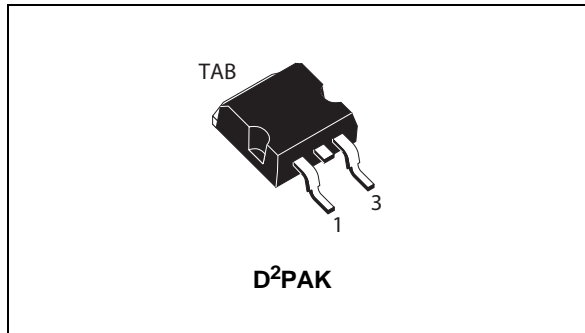
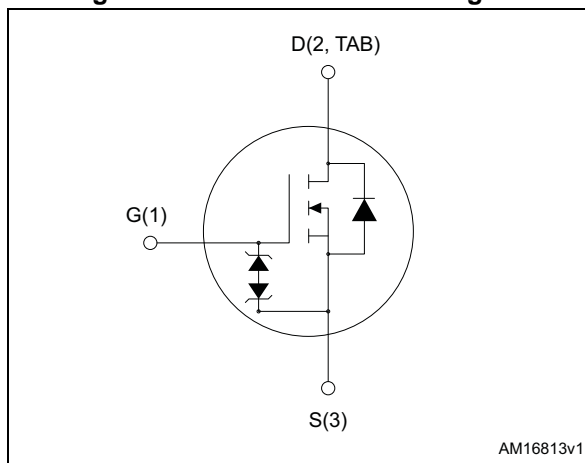


Figure 1. Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on) max.}	I _D	P _{TOT}
STB9NK60ZDT4	600 V	0.95 Ω	7 A	125 W

- Extremely high dv/dt capability
- Zener-protected
- 100% avalanche tested
- Gate charge minimized
- Low intrinsic capacitances
- Fast internal recovery diode

Applications

- Switching applications
- Fast internal recovery diode

Description

The device is developed using the revolutionary SuperFREDMesh™ technology. It associates all advantages of reduced on-resistance, Zener gate protection and very high dv/dt capability with a fast body-drain recovery diode. Such series complements the “FDmesh™” advanced technology.

Table 1. Device summary

Order code	Marking	Package	Packaging
STB9NK60ZDT4	B9NK60ZD	D ² PAK	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	7	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	4.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	125	W
	Derating factor	1	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate-source ESD (HBM-C=100 pF, R=1.5 k Ω)	4000	V
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_j	Max. operating junction temperature	- 55 to 150	$^\circ\text{C}$
T_{stg}	Storage temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 7\text{ A}$, $di/dt \leq 500\text{ A}/\mu\text{s}$; $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	1	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max. ⁽¹⁾	30	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board.

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	7	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$, $I_D=I_{AR}$; $V_{DD}=50$)	235	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$ $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$			1 50	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 3.5\text{ A}$		0.85	0.95	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 3.5\text{ A}$	-	5.3		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1110		pF
C_{oss}	Output capacitance		-	135		pF
C_{rss}	Reverse transfer capacitance		-	30		pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0$	-	72		pF
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 11\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 15)	-	41	53	nC
Q_{gs}	Gate-source charge		-	8.7		nC
Q_{gd}	Gate-drain charge		-	21		nC

1. Pulsed: pulse duration= 300 μs , duty cycle 1.5%.
2. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 3.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14 and Figure 19)	-	11.4	-	ns
t_r	Rise time		-	13.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	23.1	-	ns
t_f	Fall time		-	15	-	ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD} = 480\text{ V}$, $I_D = 7\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14 and Figure 19)	-	11	-	ns
t_f	Fall time		-	8	-	ns
t_c	Cross-overtime		-	20	-	ns

Table 8. Source - drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ (see Figure 16)	-	130		ns
Q_{rr}	Reverse recovery charge		-	550		nC
I_{RRM}	Reverse recovery current		-	8.4		A
t_{rr}	Reverse recovery time	$I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16)	-	176		ns
Q_{rr}	Reverse recovery charge		-	880		nC
I_{RRM}	Reverse recovery current		-	10		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration= 300 μs , duty cycle 1.5%.

Table 9. Gate - source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}^{(1)}$	Gate-source breakdown voltage	$I_{gs} = \pm 1\text{ mA}$ (open drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

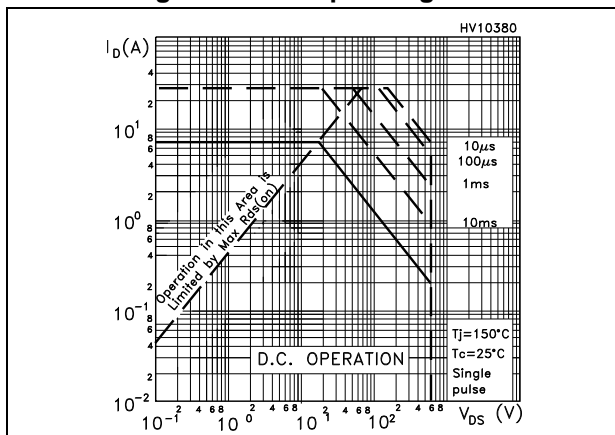


Figure 3. Thermal impedance

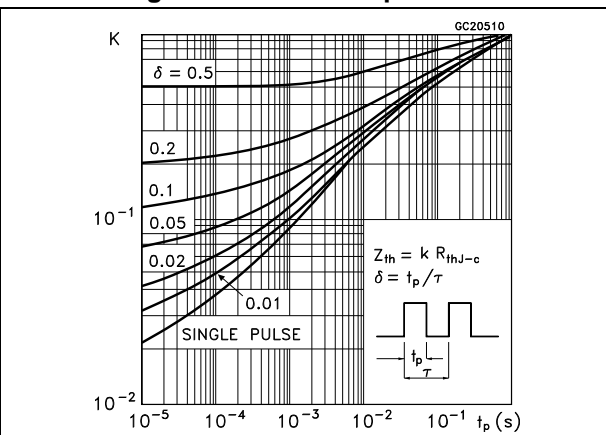


Figure 4. Output characteristics

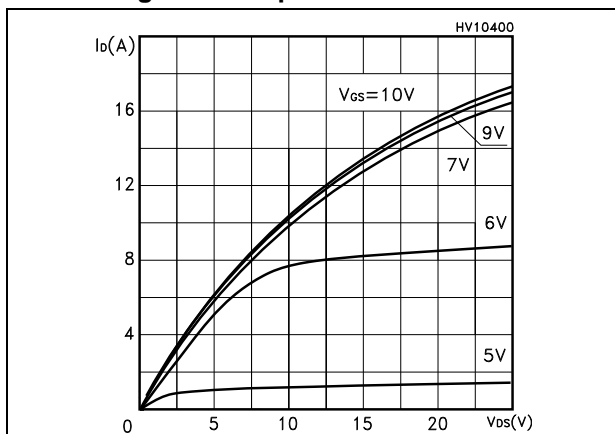


Figure 5. Transfer characteristics

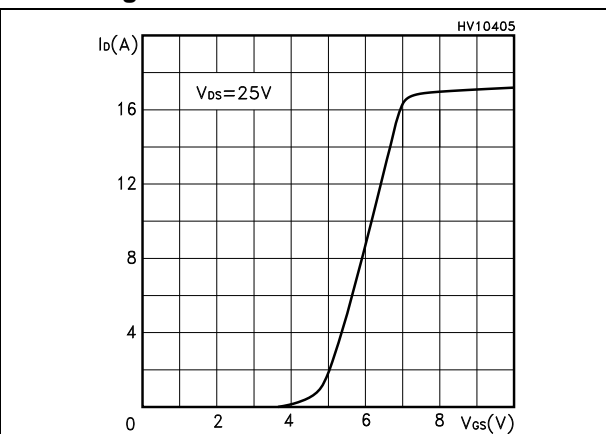


Figure 6. Normalized BVDSS vs temperature

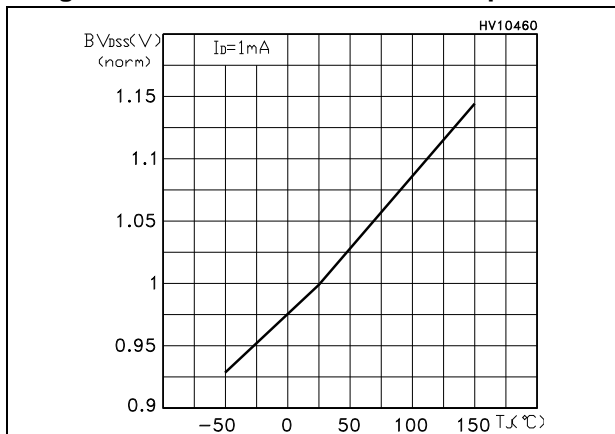


Figure 7. Static drain-source on-resistance

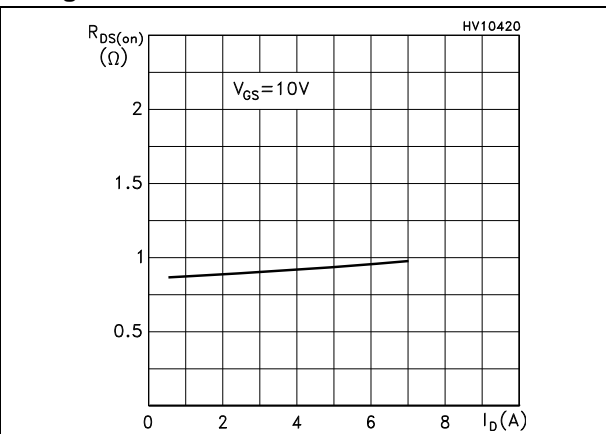


Figure 8. Gate charge vs gate-source voltage

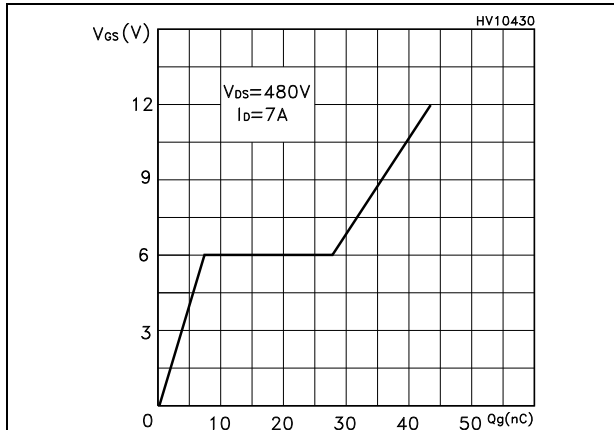


Figure 9. Capacitance variations

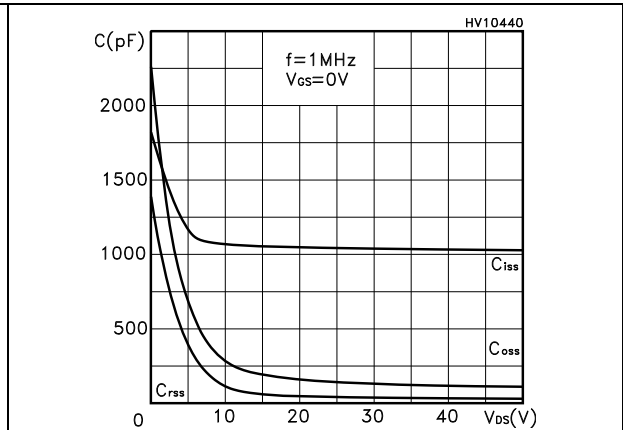


Figure 10. Normalized gate threshold voltage vs temperature

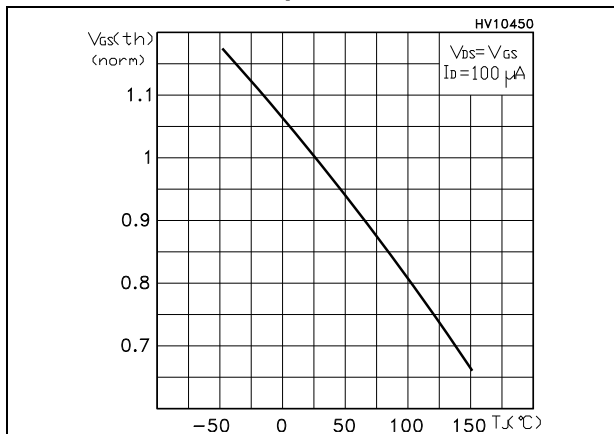


Figure 11. Normalized on-resistance vs temperature

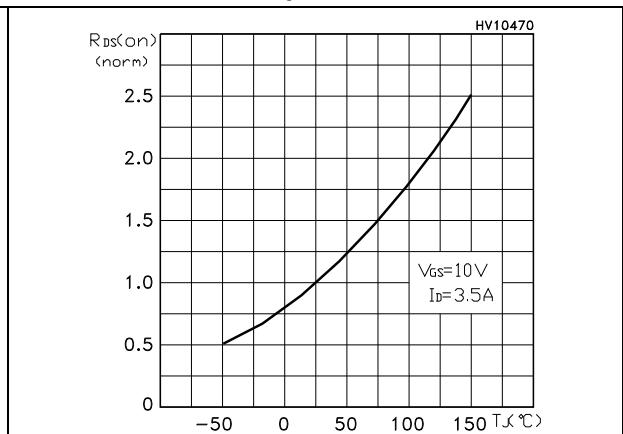


Figure 12. Source-drain diode forward characteristics

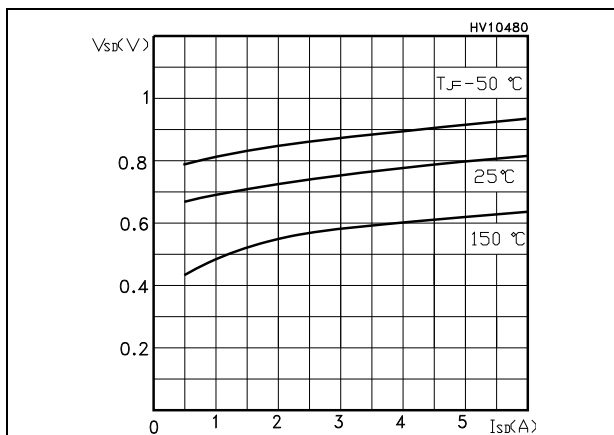
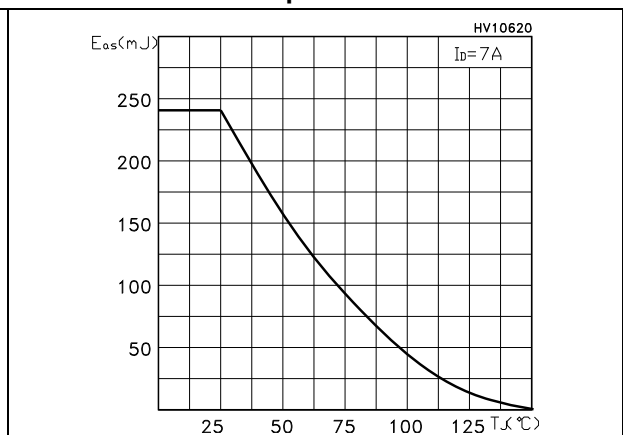
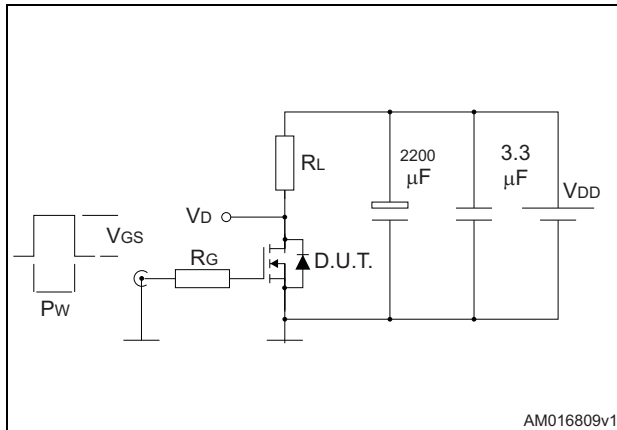


Figure 13. Maximum avalanche energy vs temperature



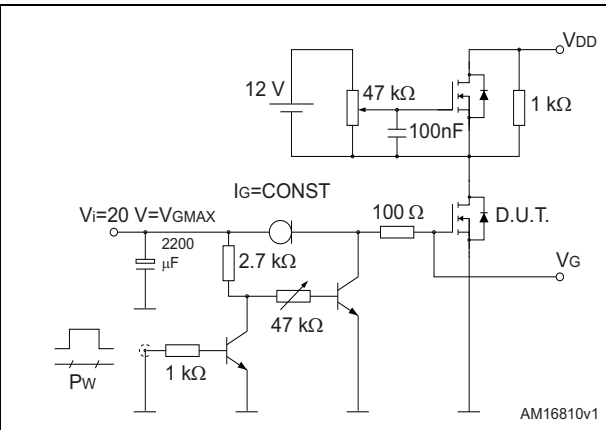
3 Test circuits

Figure 14. Switching time test circuit for resistive load



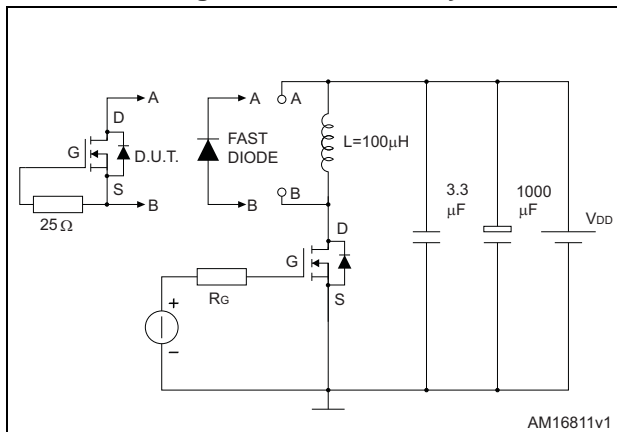
AM016809v1

Figure 15. Gate charge test circuit



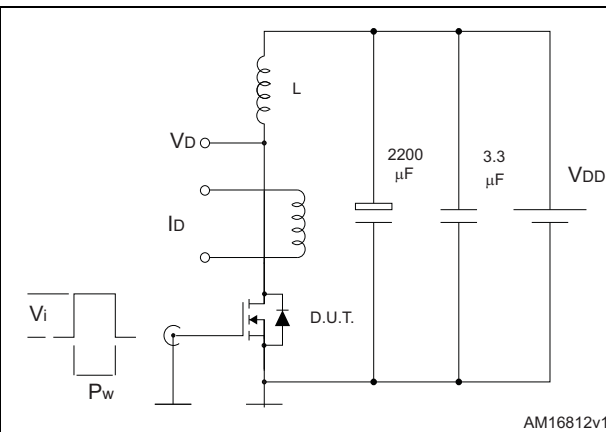
AM16810v1

Figure 16. Test circuit for inductive load switching and diode recovery times



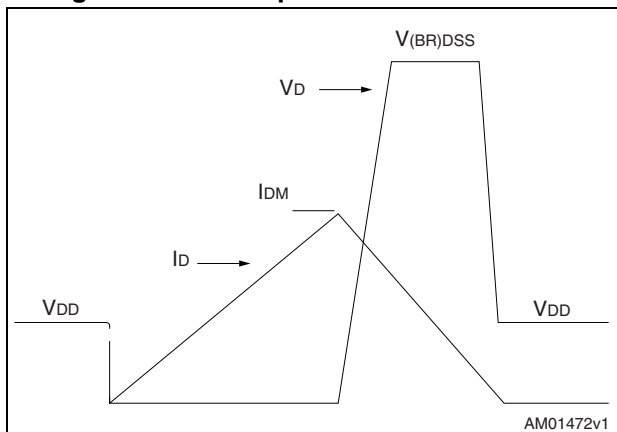
AM16811v1

Figure 17. Unclamped inductive load test circuit



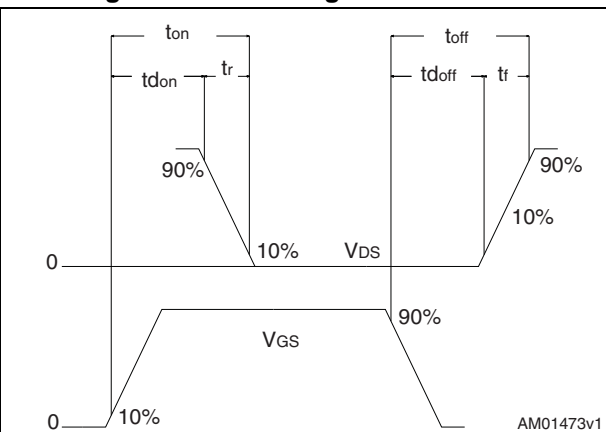
AM16812v1

Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 10. D²PAK (TO-263) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 20. D²PAK (TO-263) drawing

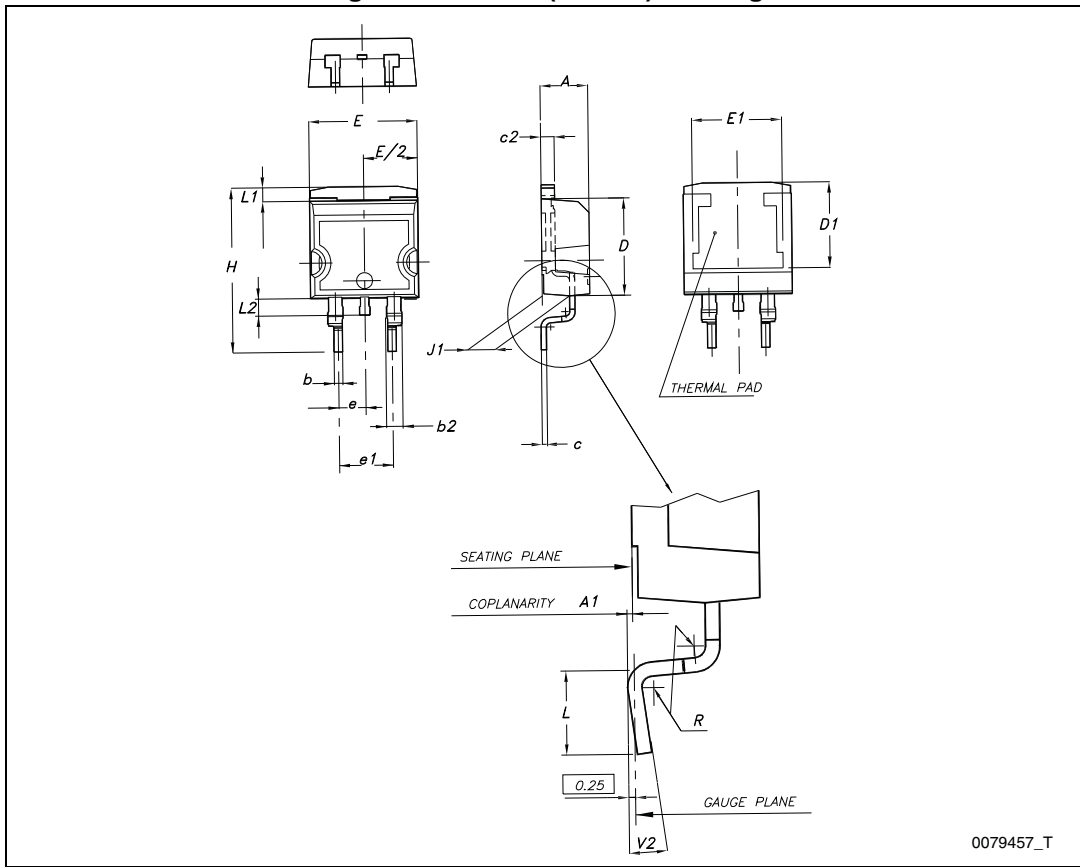
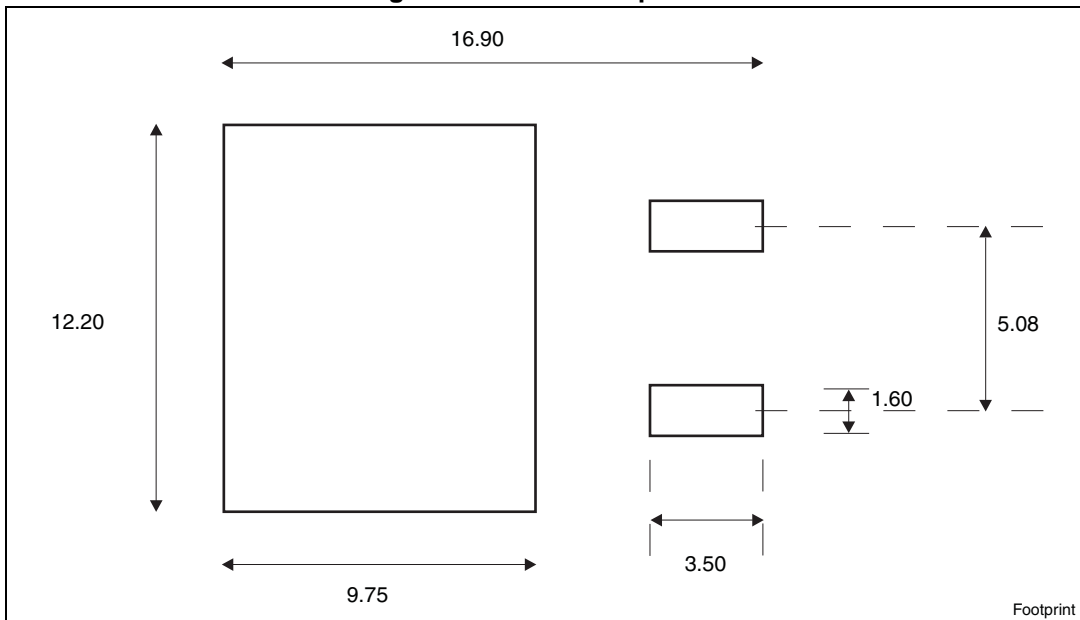


Figure 21. D²PAK footprint(a)



a. All dimensions are in millimeters.

5 Packaging mechanical data

Table 11. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 22. D²PAK (TO-263) tape

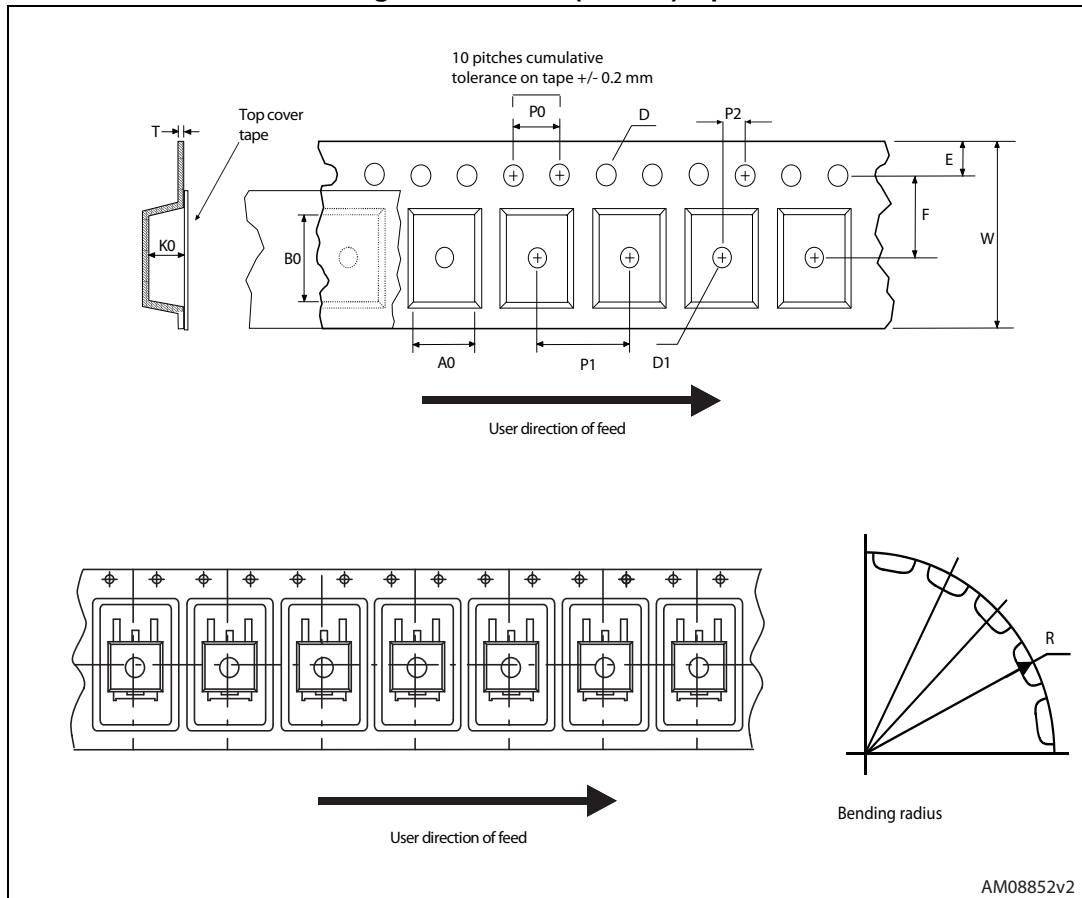
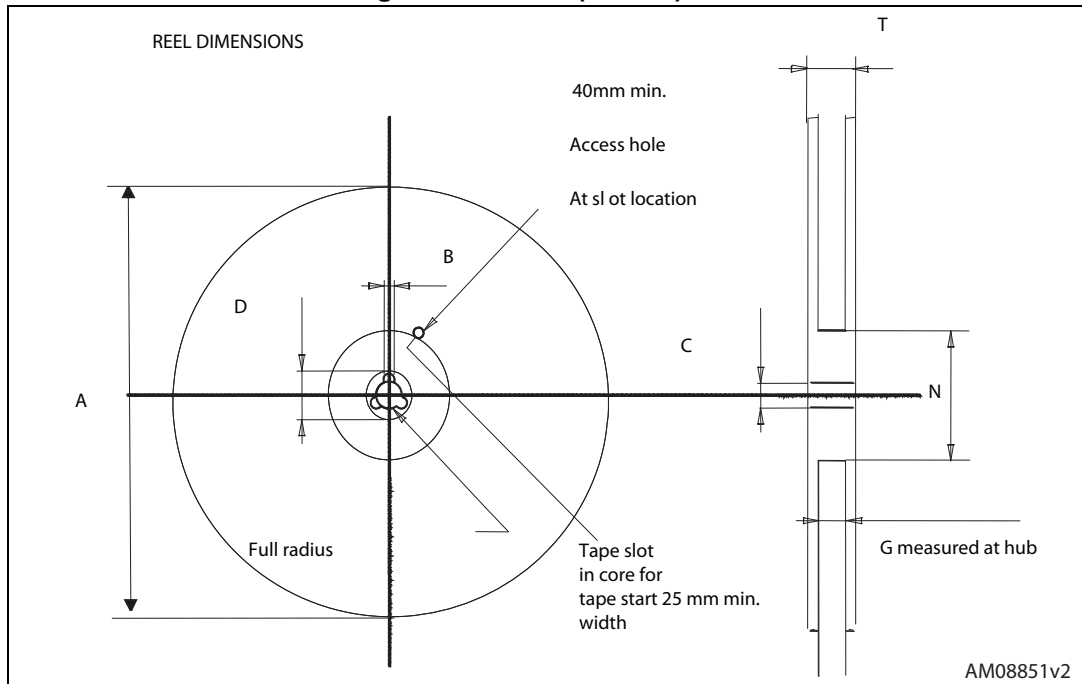


Figure 23. D²PAK (TO-263) reel



6 Revision history

Table 12. Document revision history

Date	Revision	Changes
29-Sep-2003	6	Data updated.
13-Jun-2006	7	The doc. has been reformatted.
14-Apr-2008	8	Table 8 has been corrected. Package mechanical data updated.
11-Jul-2013	9	-The part numbers: STF9NK60ZD and STP9NK60ZD have been moved to a separate datasheet. -Changed the title and Figure 1 . -Added Zener-protected to the features. -Minor text changes.

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