



# STD100NH02L STD100NH02L-1

N-channel 24V - 0.0042Ω - 60A - DPAK - IPAK  
STripFET™ II Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD100NH02L	24V	<0.0048Ω	60A <sup>(1)</sup>
STD100NH02L-1	24V	<0.0048Ω	60A <sup>(1)</sup>

1. Value limited by wire bonding

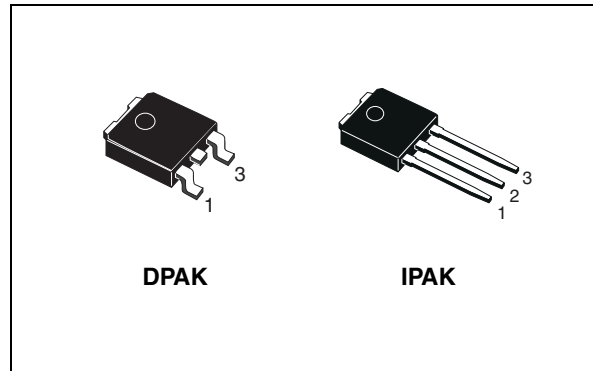
- R<sub>DS(on)</sub> \* Qg industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device

## Description

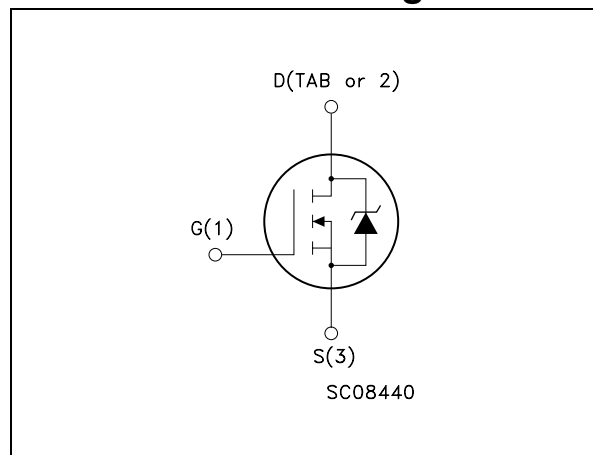
This device utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

## Applications

- Switching application



## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STD100NH02LT4	D100NH02L	DPAK	Tape & reel
STD100NH02L-1	D100NH02L	IPAK	Tube

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{\text{spike}}^{(1)}$	Drain-source voltage rating	30	V
$V_{\text{DS}}$	Drain-source voltage ( $V_{\text{GS}} = 0$ )	24	V
$V_{\text{DGR}}$	Drain-gate voltage ( $R_{\text{GS}} = 20\text{K}\Omega$ )	24	V
$V_{\text{GS}}$	Drain-source voltage	$\pm 20$	V
$I_{\text{D}}^{(2)}$	Drain current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$	60	A
$I_{\text{D}}^{(2)}$	Drain current (continuous) at $T_{\text{C}} = 100^{\circ}\text{C}$	60	A
$I_{\text{DM}}^{(3)}$	Drain current (pulsed)	240	A
$P_{\text{TOT}}$	Total dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$	100	W
	Derating factor	0.67	W/ $^{\circ}\text{C}$
$E_{\text{AS}}^{(4)}$	Single pulse avalanche energy	800	mJ
$T_{\text{stg}}$	Storage temperature	-55 to 175	$^{\circ}\text{C}$
$T_{\text{J}}$	Max. operating junction temperature		

1. Guaranteed when external  $R_{\text{g}} = 4.7\ \Omega$  and  $t_{\text{f}} < t_{\text{fmax}}$ .

2. Value limited by wire bonding.

3. Pulse width limited by safe operating area

4. Starting  $T_{\text{J}} = 25^{\circ}\text{C}$ ,  $I_{\text{D}} = 30\text{A}$ ,  $V_{\text{DD}} = 15\text{V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{\text{thJC}}$	Thermal resistance junction-case Max	1.5	$^{\circ}\text{C}/\text{W}$
$R_{\text{thJA}}$	Thermal resistance junction-ambient Max	100	$^{\circ}\text{C}/\text{W}$
$T_{\text{I}}$	Maximum lead temperature for soldering purpose	275	$^{\circ}\text{C}$

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 25\text{mA}$ , $V_{GS} = 0$	24			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 20$ $V_{DS} = 20$ , $T_C = 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	1	1.8		V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$ , $I_D = 30\text{A}$ $V_{GS} = 5\text{V}$ , $I_D = 15\text{A}$		0.0042 0.005	0.0048 0.009	$\Omega$ $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10\text{V}$ , $I_D = 30\text{A}$		50		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 15\text{V}$ , $f = 1\text{MHz}$ , $V_{GS} = 0$		3940 1020 110		pF pF pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 10\text{V}$ , $I_D = 30\text{A}$ $V_{GS} = 10\text{V}$		62 12 8	84	nC nC nC
$Q_{oss}^{(2)}$	Output charge	$V_{DS} = 16\text{V}$ , $V_{GS} = 0\text{V}$		24		nC
$Q_{gls}^{(3)}$	Third-quadrant gate charge	$V_{DS} < 0\text{V}$ , $V_{GS} = 10\text{V}$		56.5		nC
$R_G$	Gate input resistance	$f = 1\text{MHz}$ gate DC Bias = 0 Test signal level = 20mV Open drain		1.1		$\Omega$

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%
2.  $Q_{oss} = C_{oss} \cdot \Delta V_{in}$ ,  $C_{oss} = C_{gd} + C_{ds}$ . See [Chapter Appendix A](#)
3. Gate charge for synchronous operation

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10V, I_D = 30A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ <i>Figure 13 on page 8</i>		15	47	ns
$t_r$	Rise time			200		ns
$t_{d(off)}$	Turn-off delay time			60		ns
$t_f$	Fall time			35		ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				60	A
$I_{SDM}$	Source-drain current (pulsed)				240	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 30A, V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 60A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 15V, T_J = 150^\circ C$ <i>Figure 15 on page 8</i>		47		ns
$Q_{rr}$	Reverse recovery charge			58		$\mu C$
$I_{RRM}$	Reverse recovery current			2.5		A

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

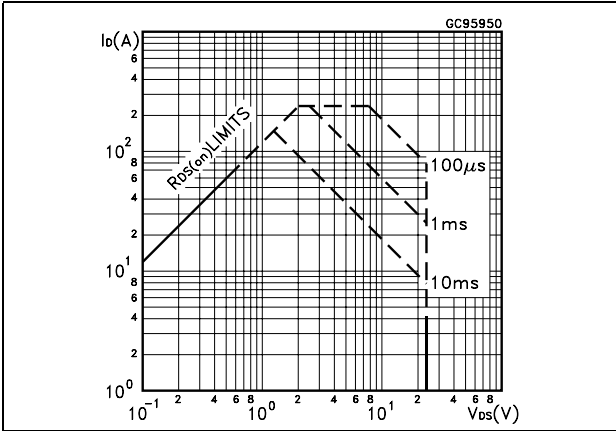


Figure 2. Thermal impedance

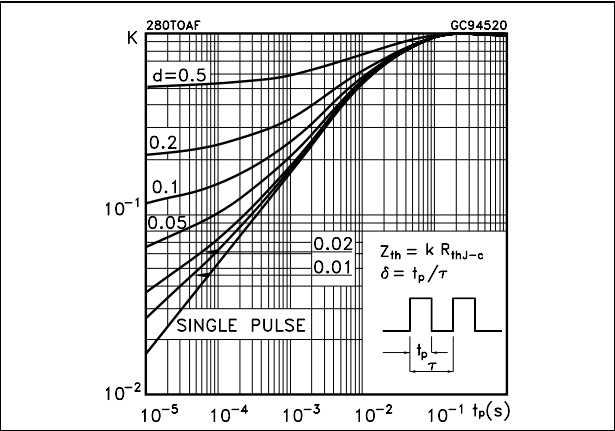


Figure 3. Output characteristics

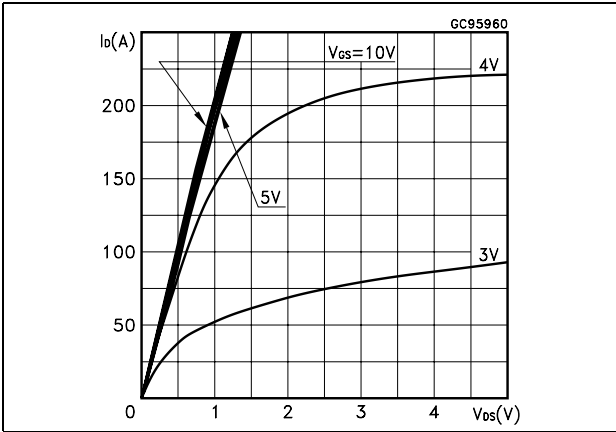


Figure 4. Transfer characteristics

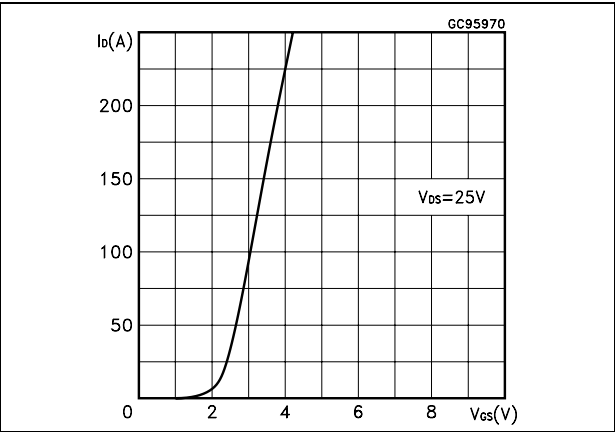


Figure 5. Transconductance

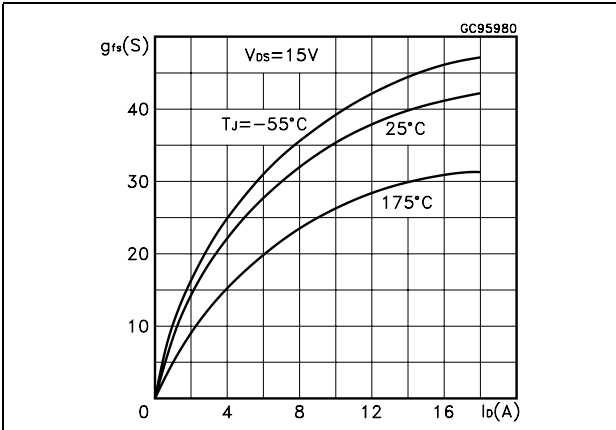


Figure 6. Static drain-source on resistance

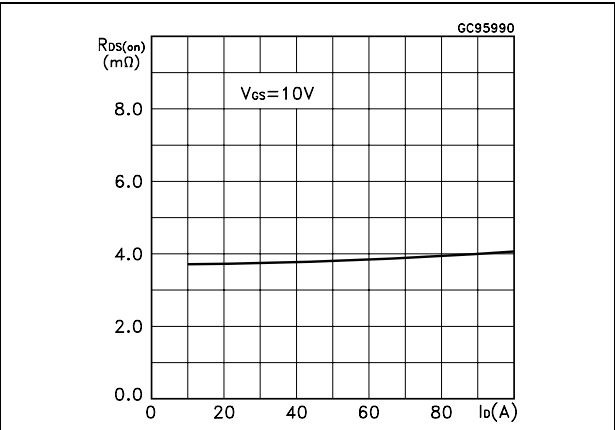


Figure 7. Gate charge vs gate-source voltage      Figure 8. Capacitance variations

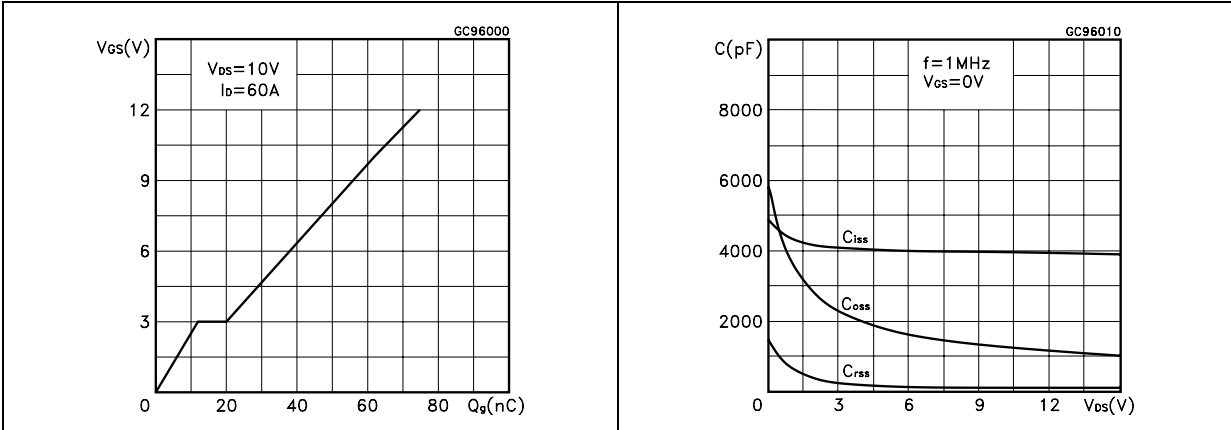


Figure 9. Normalized gate threshold voltage vs temperature      Figure 10. Normalized on resistance vs temperature

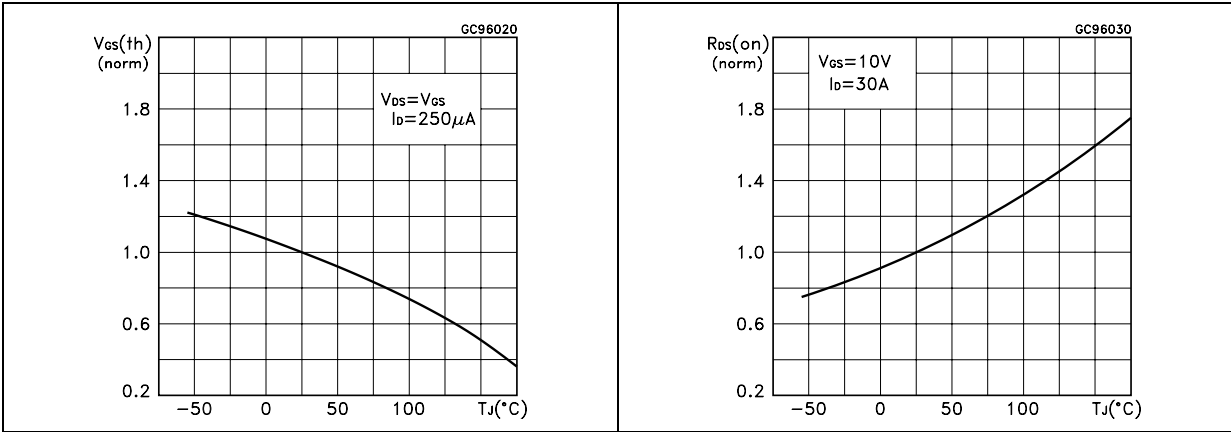
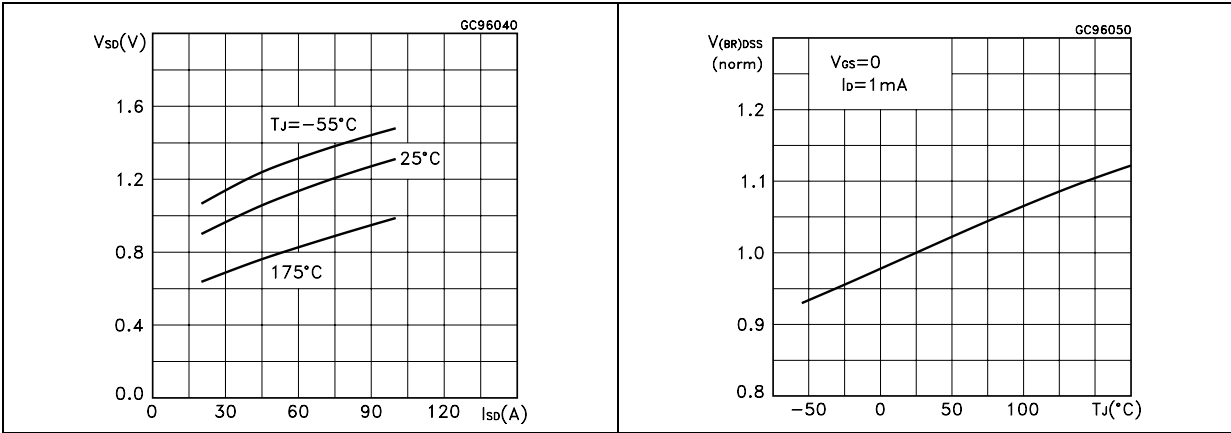
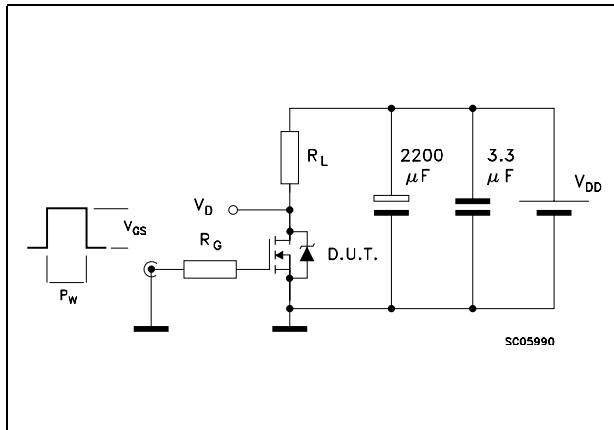


Figure 11. Source-drain diode forward characteristics      Figure 12. Normalized breakdown voltage vs temperature

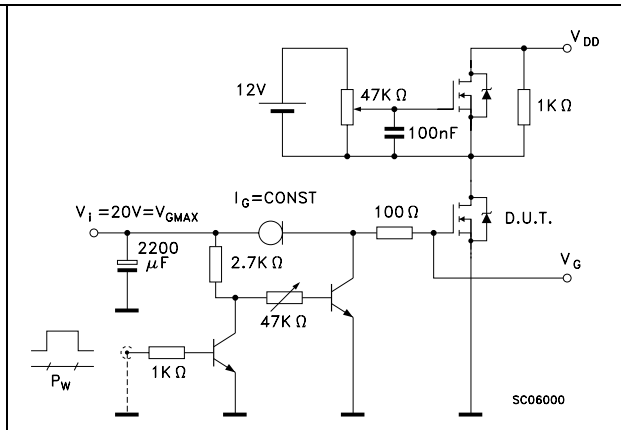


### 3 Test circuit

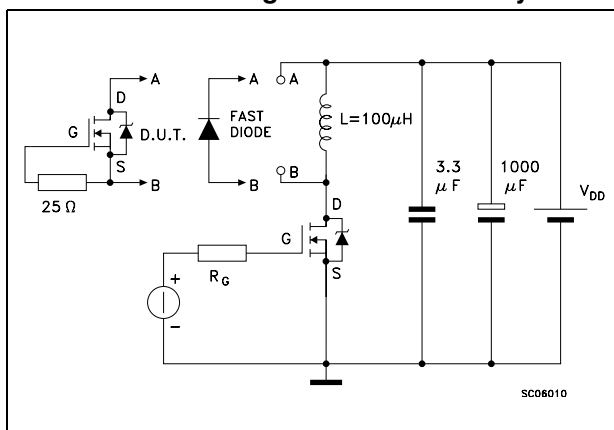
**Figure 13. Switching times test circuit for resistive load**



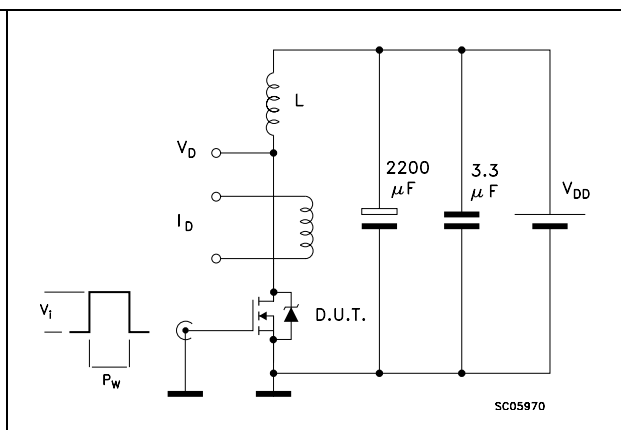
**Figure 14. Gate charge test circuit**



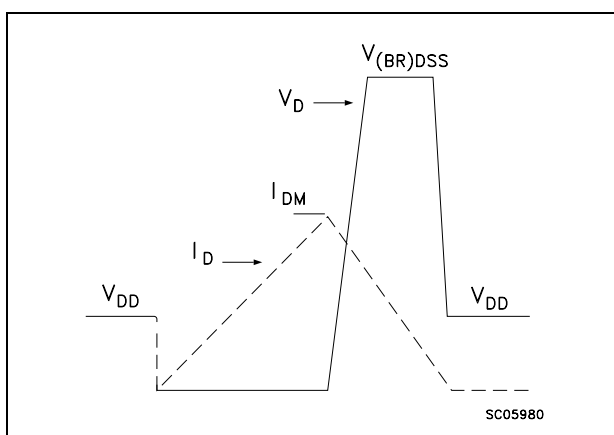
**Figure 15. Test circuit for inductive load switching and diode recovery times**



**Figure 16. Unclamped Inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



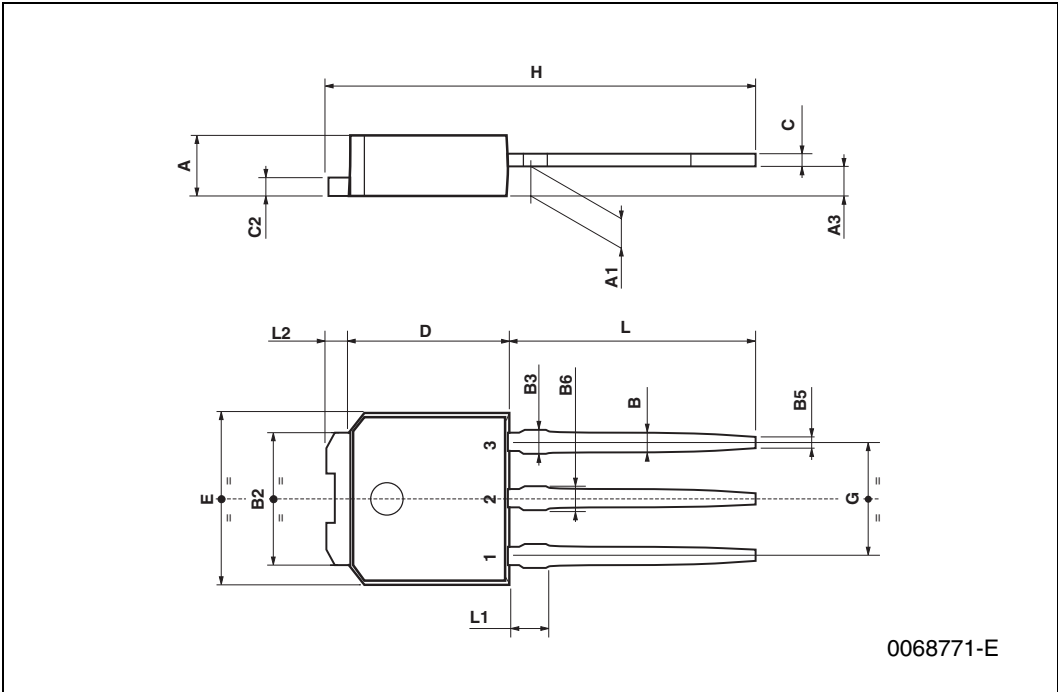


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



DPAK MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°

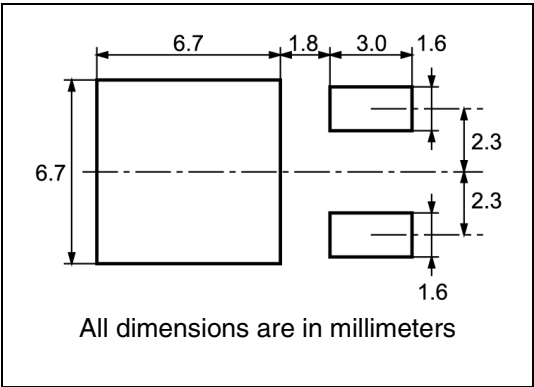
  

The mechanical drawing illustrates the STD100NH02L DPAK package. It includes a top view showing dimensions E, b4, L2, L4, H, e, e1, and b(2x). A side view shows dimensions A, c2, D, A1, c, and R. A detail view of the thermal pad shows dimensions E1, D1, and a thermal pad symbol. A circular detail view shows the lead profile with dimensions A2, L, (L1), V2, and a gauge plane at 0.25 mm. The seating plane is also indicated.

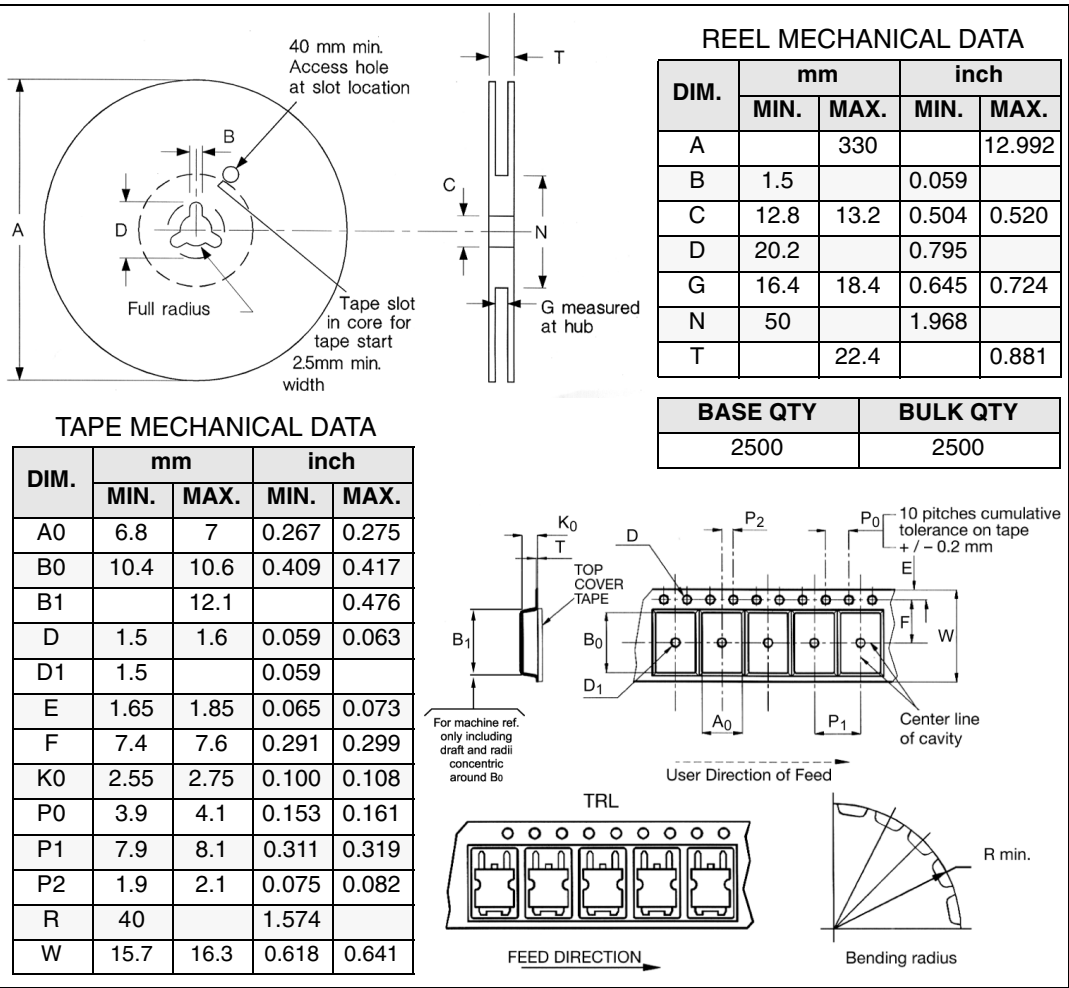
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# 5 Packaging mechanical data

## DPAK FOOTPRINT

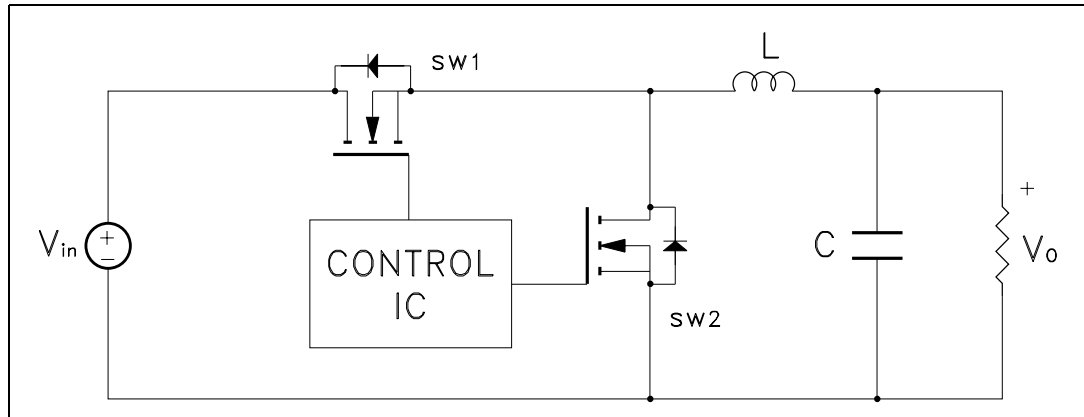


## TAPE AND REEL SHIPMENT



## Appendix A Buck converter - power losses estimation

Figure 18. Buck converter: power losses estimation



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
  - Very low  $R_{DS(on)}$  to reduce conduction losses
  - Small  $Q_{gl}$  to reduce the gate charge losses
  - Small  $C_{oss}$  to reduce losses due to output capacitance
  - Small  $Q_{rr}$  to reduce losses on SW1 during its turn-on
  - The  $C_{gd}/C_{gs}$  ratio lower than  $V_{th}/V_{gg}$  ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
  - Small  $R_g$  and  $L_s$  to allow higher gate current peak and to limit the voltage feedback on the gate
  - Small  $Q_g$  to have a faster commutation and to reduce gate charge losses
  - Low  $R_{DS(on)}$  to reduce the conduction losses.

**Table 7. Power losses calculation**

		High side switching (SW1)	Low side switch (SW2)
Pconduction		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1 - \delta)$
Pswitching		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
Pdiode	Recovery <sup>(1)</sup>	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
Pgate(Q <sub>G</sub> )		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P <sub>Qoss</sub>		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

**Table 8. Paramiters meaning**

Parameter	Meaning
d	Duty-cycle
Q <sub>gsth</sub>	Post threshold gate charge
Q <sub>gls</sub>	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P <sub>Qoss</sub>	Output capacitance losses

## 6 Revision history

**Table 9. Revision history**

Date	Revision	Changes
09-Sep-2004	9	Complete version
08-Aug-2006	10	The document has been reformatted, updated SOA <a href="#">Figure 1</a> .
18-Dev-2006	11	Typo mistake on <a href="#">Table 3</a> .

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