AN3319
Application note

STEVAL-ISV006V1: solar battery charger using the SPV1040

Introduction

The SPV1040 is a high efficiency, low power and low voltage DC-DC converter that provides a single output voltage up to 5.5 V. Startup is guaranteed at 0.3 V and the device operates down to 0.45 V when coming out from MPPT mode. It is a 100 kHz fixed frequency PWM step-up (or boost) converter able to maximize the energy generated even by one single solar cell (such as a polycrystalline or amorphous PV cells). The duty cycle is controlled by an embedded unit running an MPPT with the goal of maximizing the power generated from the panel by continuously tracking its output voltage and current.

The SPV1040 guarantees the safety of the application device or of the converter itself by stopping the PWM switching in the case of an overcurrent or overtemperature condition.

The IC integrates an 80 mΩ N-channel MOSFET power switch and a 120 mΩ P-channel MOSFET synchronous rectifier.

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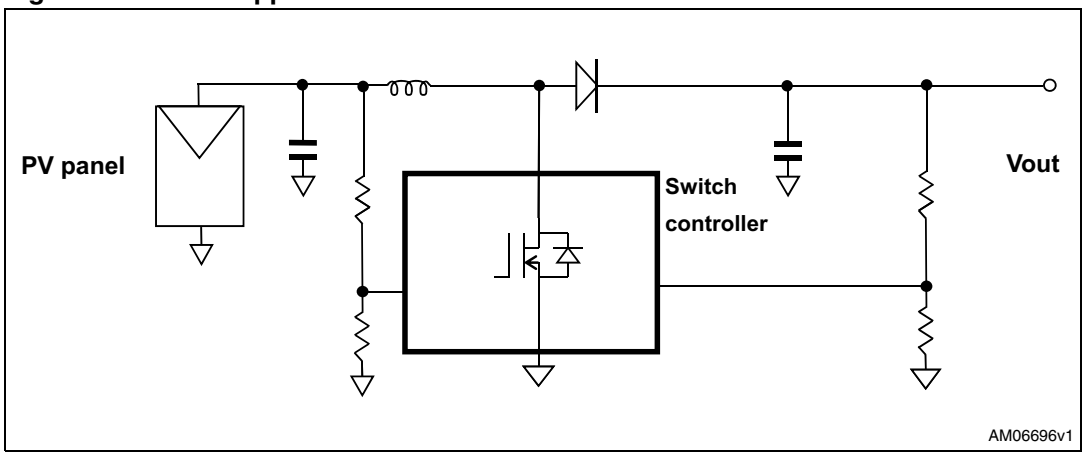
1 Application overview

Figure 1 shows the typical architecture of a boost converter based solar battery charger:

Figure 1. Boost application schematic

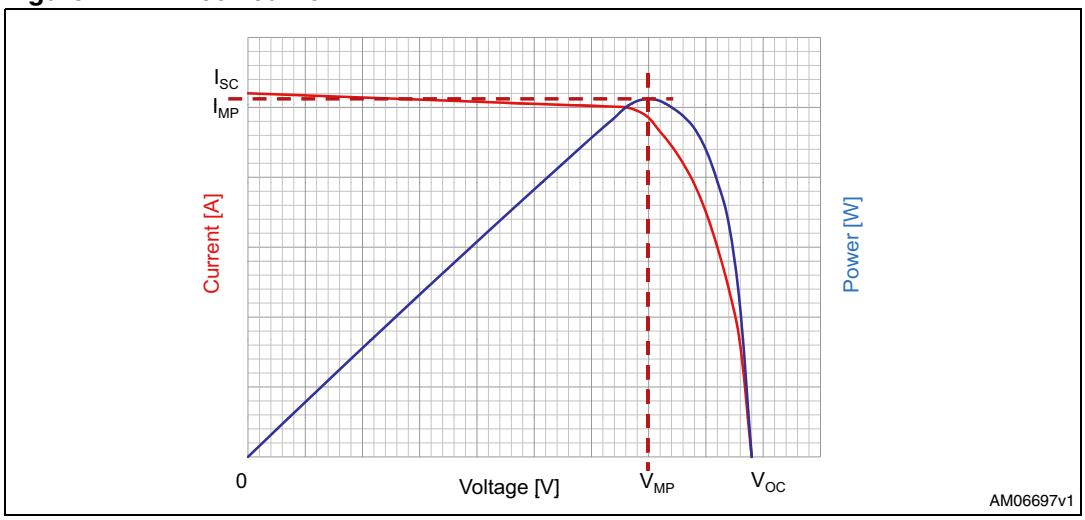


The SPV1040 adapts the characteristics of load to those of panel. In fact, a PV panel is made up of a series of PV cells. Each PV cell provides voltage and current which depend on the PV cell size, on its technology, and on the light irradiation power. The main electrical parameters of a PV panel (typically provided at light irradiation of 1000 W/m^2, T_{amb}=25 °C) are:

- Voc (open circuit voltage)
- Vmp (voltage at maximum power point)
- Isc (short-circuit current)
- Imp (current at maximum power point)

Figure 2 shows the typical characteristics of a PV cell:

Figure 2. PV cell curve



MPP (maximum power point) is the working point of the PV cell at which the product of the extracted voltage and current provides the maximum power.

2 Boost switching application

A step-up (or boost) converter is a switching DC-DC converter able to generate an output voltage higher than (or at least equal to) the input voltage.

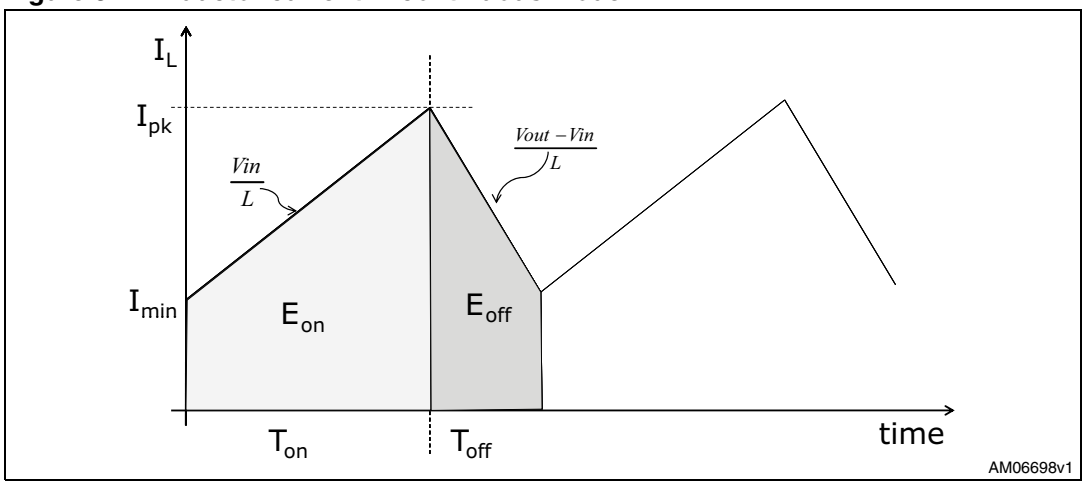
Referring to *Figure 1*, the switching element (Sw) is typically driven by a fixed frequency square waveform generated by a PWM controller.

When Sw is closed (T_{on}) the inductor stores energy and its current increases with a slope depending on the voltage across the inductor and its inductance value. During this time the output voltage is sustained by Cout and the diode does not allow any charge transfer from the output to input stage.

When Sw is open (T_{off}), the current in the inductor is forced, flowing toward the output until voltage at the input is higher than the output voltage. During this phase the current in the inductor decreases while the output voltage increases.

Figure 3 shows the behavior of inductor current.

Figure 3. Inductor current in continuous mode



The energy stored in the inductor during T_{on} is ideally equal to the energy released during T_{off}, therefore the relation between T_{on} and T_{off} can be written as follows:

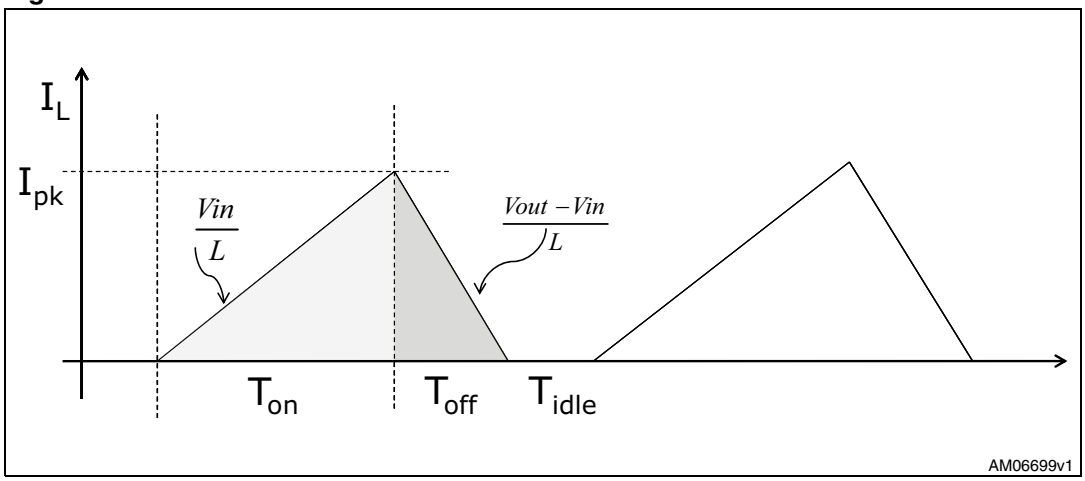
$$D = \frac{Ton}{(Ton + Toff)}$$

where “D” is the duty cycle of the square waveform driving the switching element.

Boost applications can work in two different modes depending on the minimum inductor current within the switching period, that is if it is not null or null respectively:

- Continuous mode (CM)
- Discontinuous mode (DCM)

Figure 4. Inductor current in discontinuous mode



Obviously the efficiency is normally higher in CM.

Inductance and switching frequency (F_{sw}) impact the working mode. In fact, in order to have the system working in CM, the rule below should be followed:

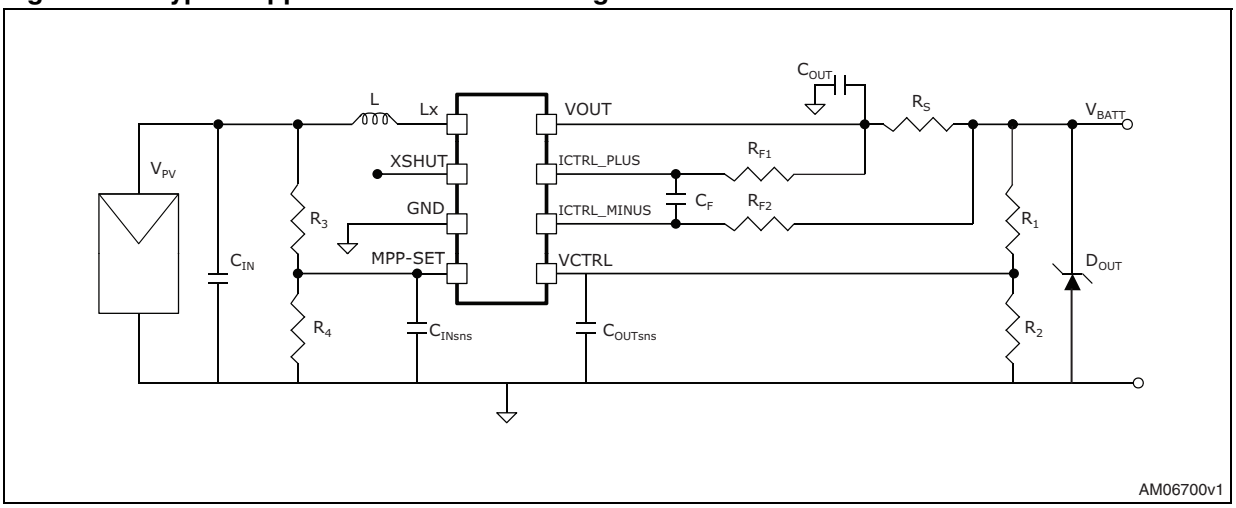
$$L > \frac{Vout^2}{Pin} * \frac{(D * (1-D))^2}{2 * Fsw}$$

According to the above, L is minimum for D = 50 %.

3 SPV1040 description

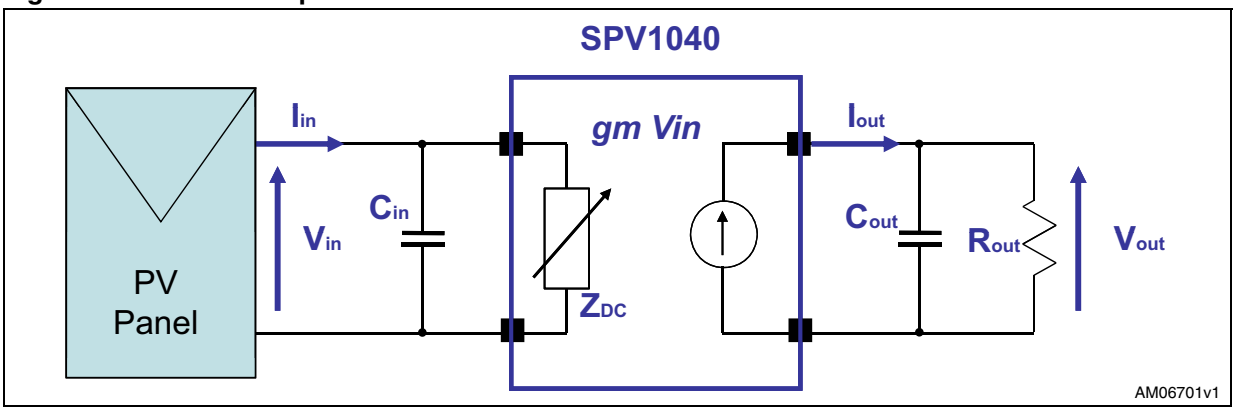
The following is a quick overview of SPV1040 functions, features, and operating modes.

Figure 5. Typical application schematic using the SPV1040



The SPV1040 acts as an impedance adapter between the input source and output load which is:

Figure 6. SPV1040 equivalent circuit



Through the MPPT algorithm, it sets up the DC working point properly by guaranteeing $Z_{in} = Z_m$ (assuming Z_m is the impedance of the supply source). In this way, the power extracted from the supply source ($P_{in} = V_{in} * I_{in}$) is maximum ($P_M = V_M * I_M$).

The voltage-current curve shows all the available working points of the PV panel at a given solar irradiation. The voltage-power curve is derived from the voltage-current curve by plotting the product V*I for each voltage generated.

Figure 7. MPPT working principle

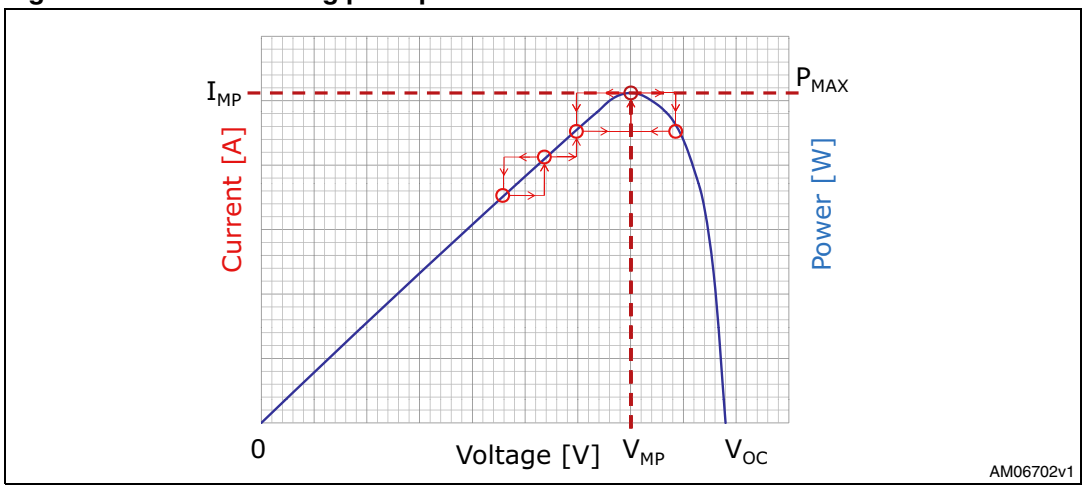
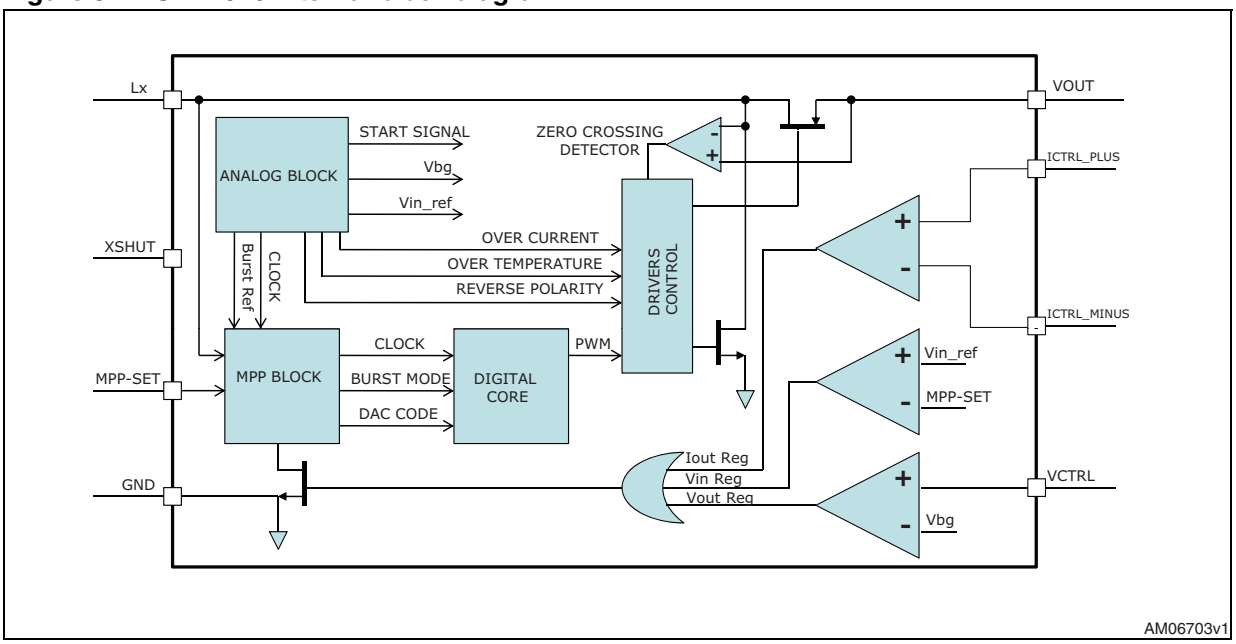


Figure 7 shows the logical sequence followed by the device which proceeds for successive approximations in the search for the MPP. This method is called “Perturb and Observe”. The diagram shows that a comparison is made between the digital value of the power Pn generated by the solar cells and sampled at instant n, and the value acquired at the previous sampling period Pn-1. This allows the MPPT algorithm to determine the sign of duty cycle and to increment or decrement it by a predefined amount. In particular, the direction of adjustment (increment or decrement of duty cycle) remains unchanged until condition Pn≥Pn-1 occurs, that is, for as long as it registers an increase of the instantaneous power extracted from the cells string. On the contrary, when it registers a decrease of the power Pn<Pn-1, the sign of duty cycle adjustment is inverted.

In the meantime, SPV1040 sets its own duty cycle according to the MPPT algorithm, other controls are simultaneously executed in order to guarantee complete application safety. These controls are mainly implemented by integrated voltage comparators whose thresholds are properly set.

Figure 8. SPV1040 internal block diagram



The duty cycle set by the MPPT algorithm can be overwritten if one of the following is triggered:

- Overcurrent protection (OVC), peak current on low side switch ≥ 1.7 A
- Overtemperature protection (OVT), internal temperature ≥ 155 °C
- Output voltage regulation, V_{ctrl} pin triggers 1.25 V
- Output current regulation $R_s * (I_{ctrl}+ - I_{ctrl}-) \geq 50$ mV
- MPP-SET voltage 300 mV ≤ $V_{MPP-SET}$ ≤ 450 mV.

Application components must be carefully selected to avoid any undesired trigger of the above thresholds.

In order to improve the overall system efficiency, and to reduce the BOM, the SPV1040 also integrates a zero crossing block whose role is to turn off the synchronous rectifier to prevent reverse current flowing from output to input.

4 Application example

Figure 9 and *10* show the demonstration board of a solar battery charger based on SPV1040 and on a status of charge indication circuit.

Figure 9. STEVAL-ISV006V1 top view

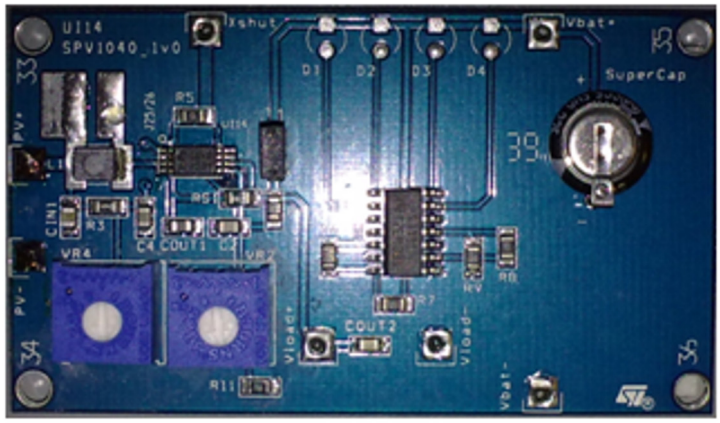
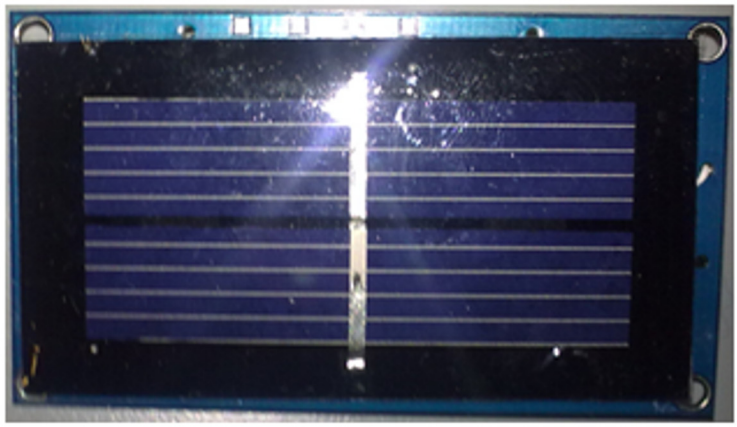


Figure 10. STEVAL-ISV006V1 bottom view



STEVAL-ISV006V1 has been designed to work with a 200 mW PV panel (Vmp=1 V, Imp=200 mA) and to regulate the output voltage up to 5.3 V. In order to guarantee the reliability of the application, Vout max. must be regulated at 4.8 V if DCM is triggered.

Two trimmers allow to regulate the voltage on the $V_{MPP\text{-}SET}$ and V_{ctrl} pins with a very high flexibility level either at PV panel or at battery side.

PV panels with higher voltage and/or current can be used, but it is suggested to verify that the soldered inductor matches the application requirements (for more details please refer to *Section 6*).

5 Schematic and bill of material

Figure 11. STEVAL-ISV006V1 schematic

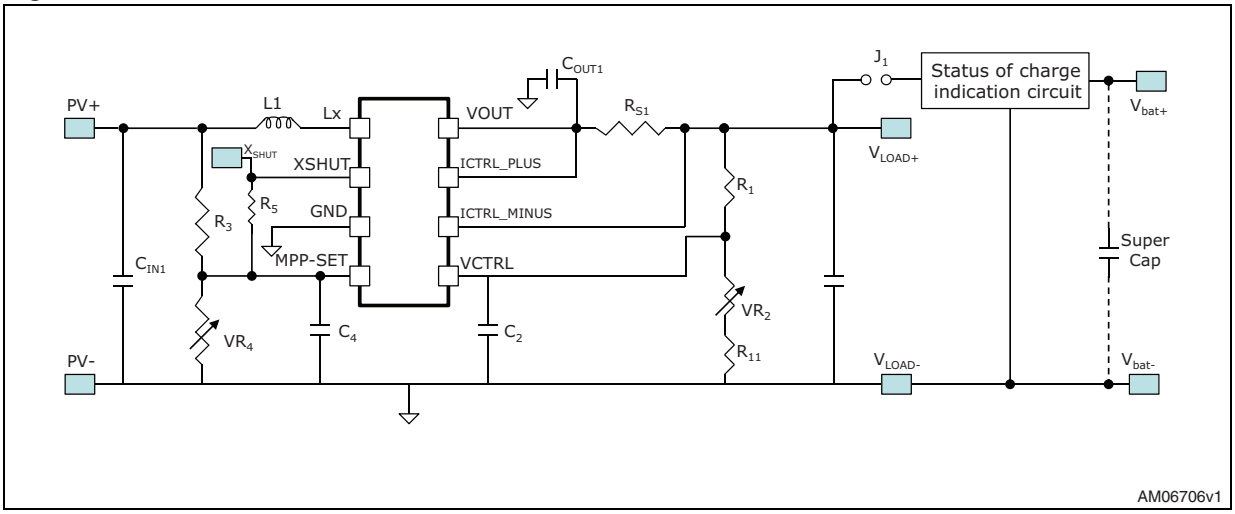


Table 1 shows the list of external components used in the demonstration board.

Table 1. BOM

Component (alternate label)	Name	Value	Supplier	Serial number
CIN1	Input capacitor	4.7 µF	EPCOS muRata	GRM21BR71A475KA73
C4	Voltage sensing capacitor	1 nF	EPCOS muRata	C2012X7R1C105K GRM033R71A103KA01
C2	Voltage sensing capacitor	1 nF	EPCOS muRata	C2012X7R1C105K GRM033R71A103KA01
COUT1	Output capacitor	4.7 µF	EPCOS muRata	C2012X7R1C475K GRM21BR71A475KA73
R3	Input voltage partitioning resistor	50 kΩ	Cyntec	RR0816R-501-DN-11
VR4	Input voltage partitioning resistor	0-100 kΩ	VISHAY	63M-104
R1	Output voltage partitioning resistor	100 kΩ	Cyntec	RR0816R-102-DN-11
VR2	Output voltage partitioning resistor	0-100 kΩ	VISHAY	63M-104
R11	Output voltage partitioning resistor	33 kΩ	Cyntec	RR0816R-331-DN-11
L1	Inductor	22 µH	EPCOS Cyntec Coilcraft	B82432T PSI25201B-220MS-11 LPS6225-223

Table 1. BOM (continued)

Component (alternate label)	Name	Value	Supplier	Serial number
SuperCap	Super capacitor	220 mF	Panasonic	EECS0HD224H
PV panel	Polycrystalline solar cell	175 mW, 1 V, 175 mA	NBSZGD	SZGD6535

6 External component selection

SPV1040 requires a set of external components and their proper selection guarantees both the best chip functionality and system efficiency.

Input voltage capacitor

Cin1 is the input capacitor connected to the input rail in order to reduce the voltage ripple.

According to the maximum current (Isc) provided by the PV panel connected at the input, the following formula should be considered to select the proper capacitance value for a specified maximum input voltage ripple (Vin_rp_max):

$$Cin \geq \frac{Isc}{Fsw * Vin\_rp\_max}$$

Maximum voltage of this capacitor is strictly dependent on the input source (typically between 1 V and 3 V).

Low-ESR capacitors are a good choice to increase the whole system efficiency. In order to reduce the ESR effect, it is suggested to split the input capacitance into two capacitors placed in parallel.

Input voltage partitioning

$V_{MPP\text{-}SET}$ is the pin used to monitor the voltage generated by the solar cells.

Depending on the Voc of the PV panel, the $V_{MPP\text{-}SET}$ pin can be directly connected to PV+ rail (if Voc < 1.25 V) or biased through a resistor divider (R3 and R4) tied to PV+ rail.

In fact, $V_{MPP\text{-}SET}$ is referred to as an internal voltage reference (Vref = 1.25 V) to allow proper MPP tracking. Consequently, the resistor divider must be identified according to the following rule:

$$\frac{R3}{R4} = \frac{Voc}{Vref} - 1 = \frac{Voc}{1.25} - 1$$

With regard to the $V_{MPP\text{-}SET}$ pin, two more constraints must be taken into account:

- When SPV1040 is OFF, $V_{MPP\text{-}SET}$ voltage must be ≥0.3 to turn ON the device
- When SPV1040 is in operating mode, it enters BURST MODE if $V_{MPP\text{-}SET}$ decreases triggering the 450 mV threshold.

R3 and R4 should be selected in the range of 100 kΩ - 10 MΩ to increase the system efficiency.

Input voltage sensing capacitor

C4 is placed in parallel to R4 and as close as possible to the $V_{MPP\text{-}SET}$ pin to reject noise on $V_{MPP\text{-}SET}$ voltage.

However, $V_{MPP\text{-}SET}$ must be able to follow the V_{IN} waveform to allow SPV1040 to monitor input voltage variations.

It means that the time constant [(R3//R4)*C4] must be chosen according to system properties, which is the MPPT tracking time (Tmpp~=1 ms). The rule below must be followed in order to select C4 capacitance:

$$C4 \geq T_{mpp} * \frac{1}{R3 // R4} = 1m * \frac{1}{R3 // R4}$$

For example, if R3//R4 = 100 kΩ then: $C4 \geq 10nF$

Inductor selection

Inductor selection is a crucial point for this application. The following application constraints must be taken into account:

- Maximum input current (i.e. Imp and Isc of PV panel)
- Maximum input voltage (i.e. Vmp and Voc of PV panel)
- Overcurrent threshold of SPV1040 (1.7A)
- Maximum duty cycle of SPV1040 (90 %).

The input current from the PV panel flows into the inductor, so:

$$I_{L1}(rms) \cong I_{mp} < I_{sc}$$

According to *Figure 3*, during the charge phase (switch ON), peak current on the inductor depends on the applied voltage (Vin) on the inductance (L_1), and on the duty cycle (T_{on}).

Considering the maximum duty cycle (90 %):

$$I_{L1}(pk) \cong I_{L1}(rms) + \frac{1}{2} * \frac{V_{mp}}{L_1} * 9\mu s$$

Taking into account the overcurrent threshold:

$$I_{L1}(pk) < 1.7A$$

Finally, inductance should be chosen according to the following formula:

$$L_1 > \frac{1}{2} * \frac{V_{mp} * 9\mu s}{2 - I_{L1}(rms)} = \frac{1}{2} * \frac{V_{mp} * 9\mu s}{2 - I_{mp}}$$

A safer choice is to replace Vmp with Voc.

Usually, inductances ranging between 10 µH to 100 µH satisfy most application requirements.

Other critical parameters for the inductor choice are Irms, saturation current, and size.

Irms is the self rising temperature of the inductor, affecting the nominal inductance value. In particular, the inductance decreases with Irms and the temperature increases. As a consequence the inductor current peak can reach or surpass 1.7 A.

Inductor size also affects the maximum current deliverable to the load. In any case, the saturation current of the choke should be higher than the peak current limit of the input source. Hence, the suggested saturation current must be > 1.7 A.

At the same size, small inductance values guarantee both faster response to load transients and higher efficiency.

Inductors with low series resistance are suggested in order to guarantee high efficiency.

Output voltage capacitor

A minimum output capacitance must be added at the output in order to reduce the voltage ripple.

Critical parameters for capacitors are: capacitance, maximum voltage, and ESR.

According to the maximum current (Isc) provided by the PV panel connected at the input, the following formula can be used to select the proper capacitance value (C_{out1}) for a specified maximum output voltage ripple (Vout_rp_max):

$$Cout1 \geq \frac{Iout}{Fsw * Vout\_rp\_max}$$

Maximum voltage of this capacitor is strictly dependent on the output voltage range. SPV1040 can support up to 5.5 V, so the suggested maximum voltage for these capacitors is 10 V.

Low-ESR capacitors are a good choice to increase the whole system efficiency.

Output voltage partitioning

R1 and R2 are the two resistors used for partitioning the output voltage.

The said V_{OUT_MAX} the maximum output voltage of the battery, R1 and R2 must be selected according to the following rule:

$$\frac{R1}{R2} = \frac{V_{out\_max}}{1.25} - 1$$

Also, in order to optimize the efficiency of the whole system, when selecting R1 and R2, their power dissipation must be taken into account.

Assuming a negligible current flowing into the V_{ctrl} pin, maximum power dissipation on the series R1+R2 is:

$$P_{vout\_sns} = \frac{(V_{out\_max})^2}{R1 + R2}$$

As an empirical rule, R1 and R2 should be selected to get:

$$P_{vout\_sns} << 1\%(V_{out\_max} * I_{out\_max})$$

Note: In order to guarantee proper functionality of the V_{ctrl} pin, the current flowing into the series R1+R2 should be in the range between 20 µA and 200 µA.

Output voltage sensing capacitor

C2 is placed in parallel to R2 and as close as possible to the V_{ctrl} pin.

Its role is to reject the noise on the voltage sensed by the V_{ctrl} pin.

Capacitance value depends on the time constant resulting from R2 (τ_{out}= C2*R1//R2) and from the system switching frequency (100 kHz), as follows:

$$\tau out \cong 10 * \frac{1}{Fssw}$$

$$C2 \cong 10 * \frac{1}{Fssw} * \frac{1}{R1//R2}$$

Output current sensing filter

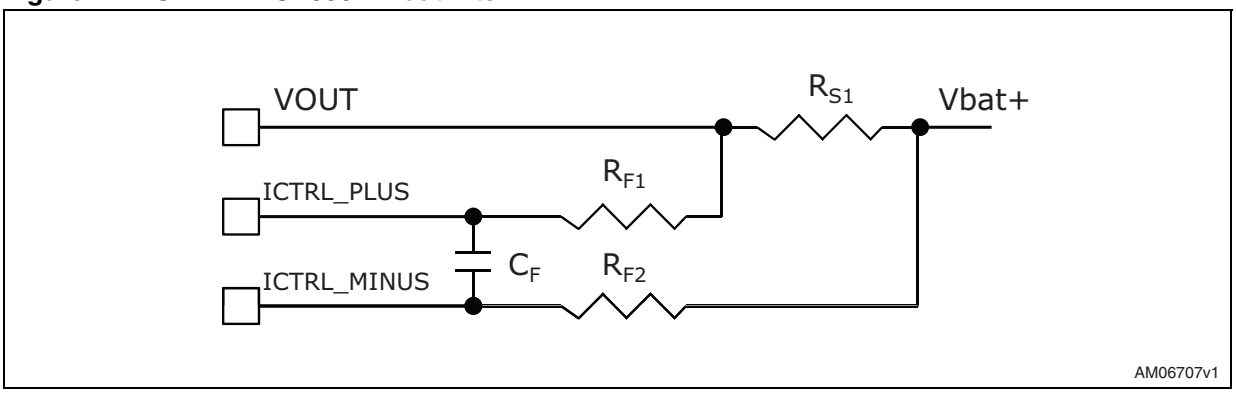
RS1 is placed in the output rail between the I_{ctrl}- and I_{ctrl}+ pins.

Its role is to sense the output current (Iout) flowing toward the load. Voltage drop on RS1 is sensed by the I_{ctrl-} and I_{ctrl+} pins and compared with the 50 mV internal threshold.

$$R_{S1} \cong \frac{50mV}{Iout\_max}$$

The triangular waveform of the current and noise may cause unexpected triggering of the 50 mV threshold. This can be avoided with a filter such as the one shown below:

Figure 12. STEVAL-ISV006V1 Iout filter



Suggested values are:

R_{F1}=R_{F2} = 1 kΩ

C_F = 1 µF

Output protection diode

D_{OUT} is placed in parallel to the output load. Its role is to protect the devices in case a PV cell providing Imp > 0.5 A is connected when very low load is connected.

In fact, SPV1040 is supplied by the Vout pin, so in the above condition the device is still OFF when the PV cell is connected and a voltage spike can occur damaging the converter and the battery.

In order to guarantee the best system performance and reliability, D_{OUT} should be selected as follows:

V_{BR} > 5.2 V and

V_{CL} < 7 V

Dout must be able to dissipate the following maximum power:

$P_{max} = I_{sc}*V_{CL}$

XSHUT resistor

The XSHUT pin controls SPV1040 turn-on (0.3 V ≤ XSHUT ≤ 5.5 V) or turn-off (XSHUT < 0.3 V).

R_5 is a 0 Ω pull-up resistor shorting the XSHUT and MPP-SET pins.

Removing R5 enables the external control of the XSHUT pin to turn the SPV1040 on/off.

7 Layout

Figure 13. STEVAL-ISV006V1 PCB top view

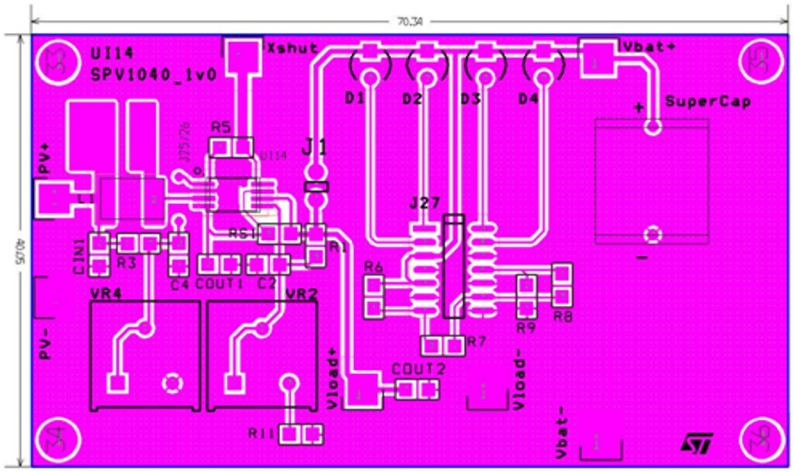
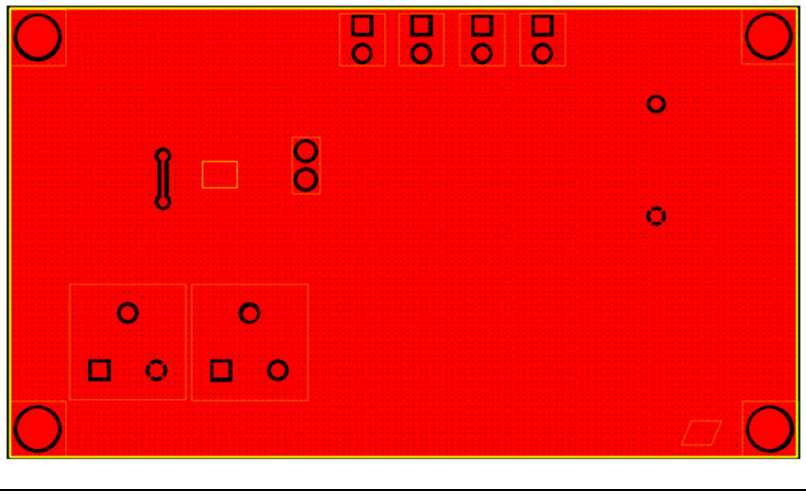


Figure 14. STEVAL-ISV006V1 PCB bottom view



Layout guidelines

PCB layout is very important in order to minimize voltage and current ripple, high frequency resonance problems, and electromagnetic interference. It is essential to keep the paths where the high switching current circulates as small as possible in order to reduce radiation and resonance problems.

Large traces for high current paths and an extended ground plane reduce noise and increase efficiency.

The output and input capacitors should be placed as close as possible to the device.

The external resistor dividers, if used, should be as close as possible to the $V_{MPP\text{-}SET}$ and V_{ctrl} pins of the device, and as far as possible from the high current circulating paths, in order to avoid picking up noise.

Appendix A SPV1040 parallel and series connection

Output pins of many SPV1040s can be connected either in parallel or in series. In both cases the output power (Pout) depends on light irradiation of each panel, on application efficiency, and on the specific constraints of the selected topology.

The objective of this section is to explain how the output power is impacted by the selected topology.

An example with 3 PV panels (Panel1, Panel2, Panel3) is presented, but the conclusion can be extended to a larger number of PV panels.

If the panel is lighted and the SPV1040 is on (it means that light irradiation intensity is such that $V_{MPP\text{-}SET} \geq 0.3$ V):

$$Poutx = \eta Pinx \qquad [x = 1..3]$$

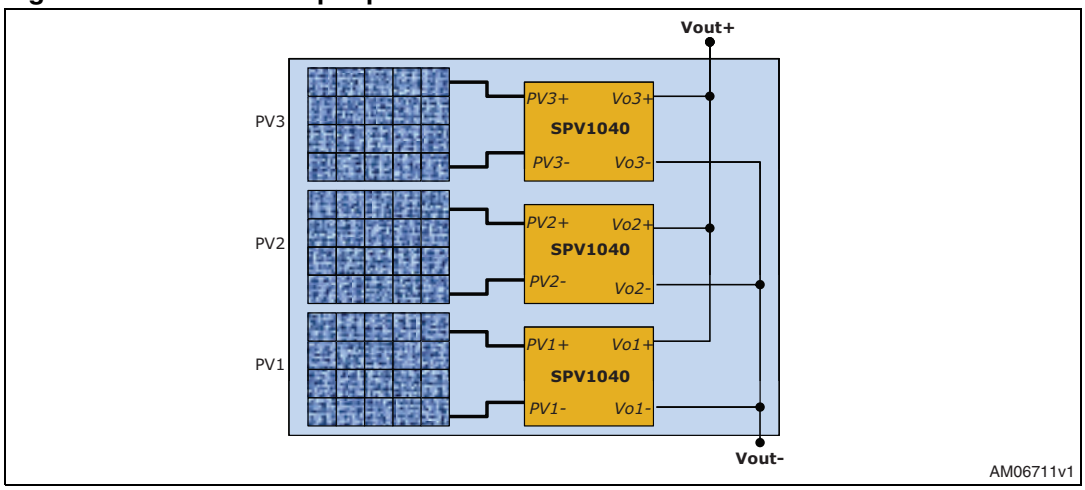
If the panel is completely shaded: $P_{outx}=0$

SPV1040 parallel connection

This topology guarantees the desired output voltage even when only one panel is irradiated. The obvious constraint of this topology is that Vout is limited to the SPV1040 maximum output voltage.

Figure 15 shows the parallel connection topology:

Figure 15. SPV1040 output parallel connection



The output partitioning (R1/R2) of each SPV1040 must be coherent with the desired Voutx.

According to the topology:

Vout=Vout1=Vout2=Vout3

Iout=Iout1+Iout2+Iout3

According to the light irradiation on each panel and to the system efficiency (η), the output power results:

$$Pout = Pout1 + Pout2 + Pout3$$

$$Poutx = Voutx * Ioutx \quad [x = 1..3]$$

$$Pinx = Vinx * Iinx \quad [x = 1..3]$$

Therefore:

$$Pout = Vout(Iout1 + Iout2 + Iout3) = \eta Pin1 + \eta Pin2 + \eta Pin3$$

Each SPV1040 contributes to the output power providing Ioutx.

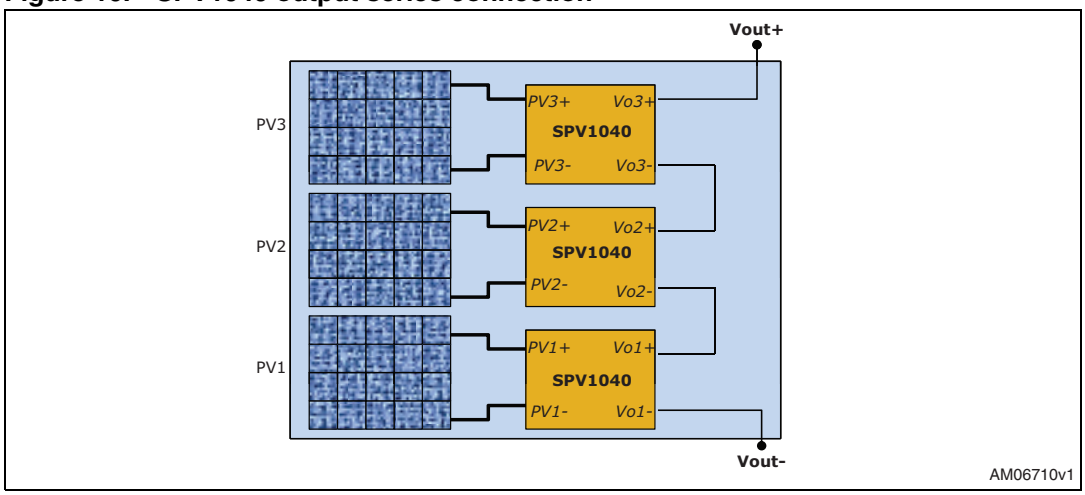
Finally, the desired Vout is guaranteed if at least one of the 3 PV panels provides enough power to turn on the SPV1040 relating to it.

SPV1040 series connection

This topology provides an output voltage that is the sum of the output voltages of the SPV1040 connected in series. The objective of this section is to explain how the output power is impacted by the selected topology.

Figure 16 shows the series connection topology:

Figure 16. SPV1040 output series connection



In this case, the topology imposes:

$$Iout = Iout1 = Iout2 = Iout3$$

$$Vout = Vout1 + Vout2 + Vout3$$

In case irradiation is the same for each panel:

$$Pin1 = Pin2 = Pin3$$

$$Pout = 3 * Poutx \quad [x = 1..3]$$

$$Poutx = \frac{1}{3} Pout$$

$$Poutx = Voutx * Ioutx = Vout1 * Iout$$

Therefore:

$$Voutx = \frac{1}{3}Vout$$

For example, assuming Pout = 3 W and Vout = 12 V, then

Voutx = 4 V.

Lower irradiation for one panel, for example on panel 2, causes lower output power, so lower Vout2 due to the Iout imposed by the topology:

$$Voutx = \frac{Poutx}{Iout}$$

The output voltage required by the load can be provided by the 1st and the 3rd SPV1040 but only up to the limit imposed by each of their R1/R2 partitionings.

Some examples can help in understanding the various scenarios assuming that each R1/R2 limits Voutx to 4.8 V.

Example 1:

Panel 2 has 75 % irradiation of panels 1 and 3:

$$Vout2 = \frac{3}{4} * Vout1 = \frac{3}{4} * Vout3$$

$$Pout1 = Pout3 = 1W$$

$$Pout2 = \frac{3}{4}Pout1 = 0.75W$$

$$Pout = Pout1 + Pout2 + Pout3 = 2.75W$$

$$Iout = \frac{Pout}{Vout} = \frac{2.75}{12} = 0.23A$$

$$Vout1 = Vout3 = \frac{1}{0.23} = 4.35V$$

$$Vout2 = \frac{0.75}{0.23} = 3.26V$$

Two SPV1040s (1st and 3rd) supply the voltage drop caused by the lower irradiation on panel 2.

Warning: **SPV1040 is a boost controller, so Voutx must be higher than Vinx, otherwise the SPV1040 turns off and the input power is transferred to the output stage through the integrated P-channel MOS without entering the switching mode.**

Example 2:

Panel 2 has 50 % irradiation of panels 1 and 3:

$$Pout2 = \frac{1}{2} * Pout1 = \frac{1}{2} * Pout3$$

$$Pout1 = Pout3 = 1W$$

$$Pout2 = \frac{1}{2} Pout1 = 0.5W$$

$$Pout = Pout1 + Pout2 + Pout3 = 2.5W$$

$$Iout = \frac{Pout}{Vout} = \frac{2.5}{12} = 0.21A$$

$$Vout1 = Vout3 = \frac{1}{0.21} = 4.76V$$

$$Vout2 = \frac{0.5}{0.21} = 2.38V$$

In this case the system is close to its maximum voltage limit, in fact, a lower irradiation on panel 2 impacts Vout1 and/or Vout3 which are very close to the maximum output voltage threshold (4.8 V) imposed by R1/R2 partitioning.

Example 3:

Panel 2 completely shaded.

In this case the maximum Vout can be 9.6 V (Vout1+Vout3).

The current flow is guaranteed by the body diodes of the power MOSFETs integrated in the SPV1040 (or by the bypass diodes, if any, placed between Vout- and Vout+).

Revision history

Table 2. Document revision history

Date	Revision	Changes
02-Feb-2011	1	Initial release.