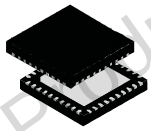
STMPE1208S

S-Touch™ 12-channel capacitive touchkey controller

Features

- 12 touchkey capacitive sensor inputs
- 12-bit general purpose input/output (GPIO)
- Operating voltage 3.0 – 5.5 V
- 98 µA in active mode, 60 µA in idle mode
- Dual interrupt output pin
- I^2C interface (up to 400 kHz)
- 7 kV HBM ESD protection
- Idle and sleep mode for low power operation
- Advanced data filtering (AFS)
- Environment tracking calibration (ETC)
- Individually adjustable touch variance (TVR) setting for all channels
- Adjustable environmental variance (EVR) for optimal calibration



QFN40

Applications

- Notebook computers
- Monitors
- Set-top boxes
- Televisions
- Portable media players and game consoles
- Mobile and smart phones
- Home entertainment systems
- Domestic appliances

Description

The STMPE1208S is a 12-channel GPIO capacitive touchkey sensor able to interface a main digital ASIC via the two-line bidirectional bus (I^2C). It senses changes in capacitance using a fully digital architecture, giving fast and accurate results at very low power consumption. Automatic impedance calibration ensures that changes in environment will never affect the correct operation of the capacitive touchkeys.

Table 1. Device summary

Order code	Package	Packing
STMPE1208SQTR	QFN40	Tape and reel

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1 Pin configuration and function

Figure 1. STMPE1208S pin configuration

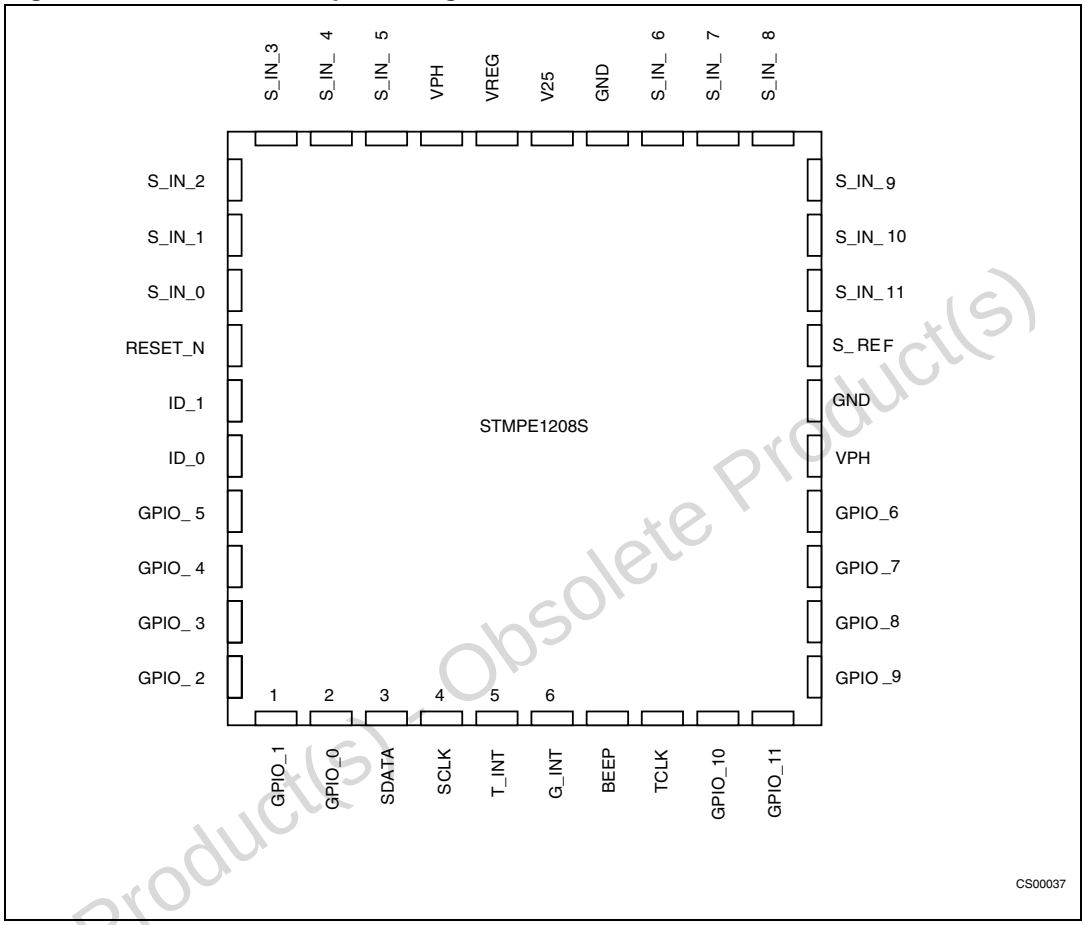


Table 2. Pin assignments and description

Pin number	Pin name	Description
1	GPIO_1	General purpose I/O
2	GPIO_0	General purpose I/O
3	SDATA	I^2C data
4	SCLK	I^2C clock
5	T_INT	Touch interrupt
6	G_INT	General interrupt
7	BEEP	Beep output
8	TCLK	Test pin (to be grounded)
9	GPIO_11	General purpose I/O
10	GPIO_10	General purpose I/O
11	GPIO_9	General purpose I/O

Table 2. Pin assignments and description (continued)

Pin number	Pin name	Description
12	GPIO_8	General purpose I/O
13	GPIO_7	General purpose I/O
14	GPIO_6	General purpose I/O
15	VPH	3 –5.5 V power supply (regulator input) Supply to this pin is also used for powering the GPIO
16	GND	Ground
17	S_REF	Touch sensing reference.
18	S_IN_11	Capacitance sensing input 11
19	S_IN_10	Capacitance sensing input 10
20	S_IN_9	Capacitance sensing input 9
21	S_IN_8	Capacitance sensing input 8
22	S_IN_7	Capacitance sensing input 7
23	S_IN_6	Capacitance sensing input 6
24	GND	Ground
25	V25	2.5 V supply
26	VREG	Internal regulator output
27	VPH	3 –5.5 V power supply (regulator input)
28	S_IN_5	Capacitance sensing input 5
29	S_IN_4	Capacitance sensing input 4
30	S_IN_3	Capacitance sensing input 3
31	S_IN_2	Capacitance sensing input 2
32	S_IN_1	Capacitance sensing input 1
33	S_IN_0	Capacitance sensing input 0
34	RESET_IN	Active low reset pin. This pin should be held ‘low’ for 10 mS from power stable state. Recommended: 47 K resistor with 0.47 µF capacitor
35	ID_1	I^2C address
36	ID_0	I^2C address
37	GPIO_5	General purpose I/O
38	GPIO_4	General purpose I/O
39	GPIO_3	General purpose I/O
40	GPIO_2	General purpose I/O

Figure 2. STMPE1208S block diagram

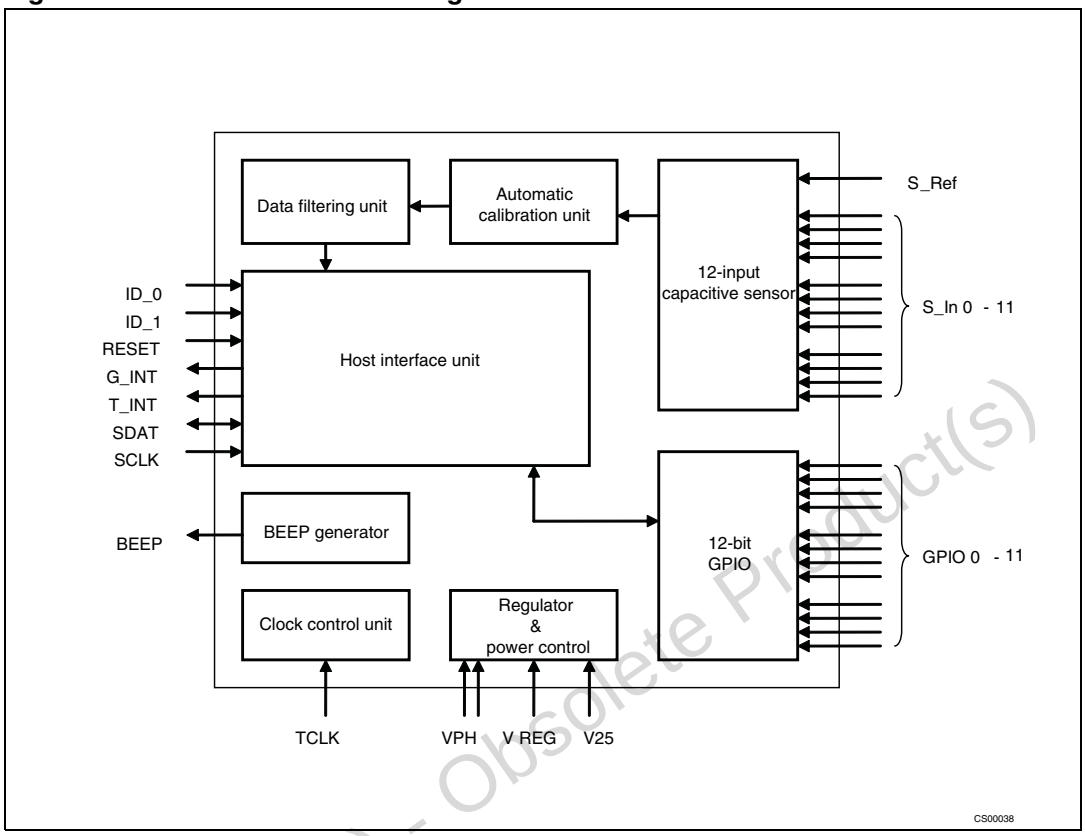
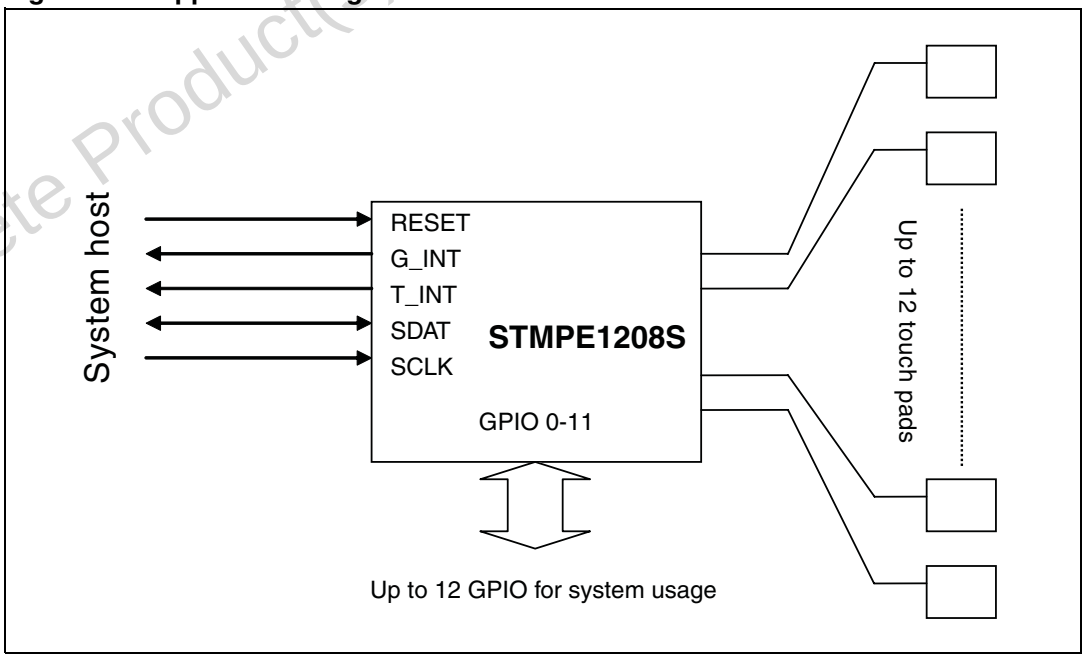


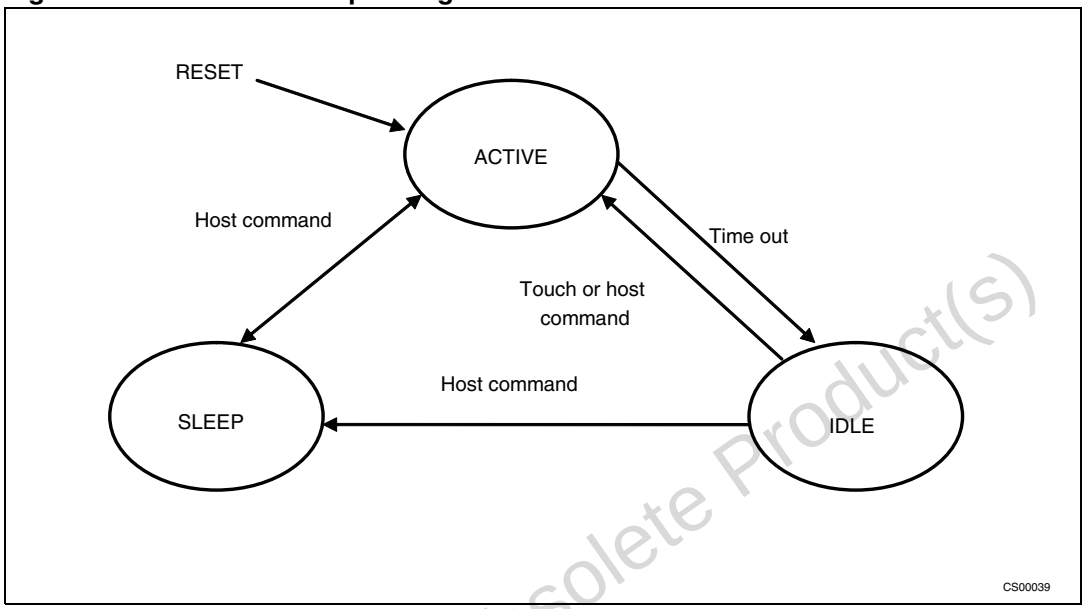
Figure 3. Application diagram



1.1 Power management

The STMPE1208S operates in 3 states.

Figure 4. STMPE1208S operating states



On reset, the STMPE1208S enters the active state immediately.

Upon a fixed period of inactivity, the device enters into the IDLE state. Any touch activity in IDLE state would cause the device to go back to active state.

In IDLE state, the calibration will not run. If the calibration is required at all time, set F2A bit to '1'.

If no touch activity is expected, the host may set the device into SLEEP state to save power.

2 Clock setting

The STMPE1208S uses a flexible clocking system that allows the user to adjust the clock speed for optimization of power consumption.

Table 3. Clocking system

OSC	PDIV	Clock	NDIV	Active	Idle
				Sensor clock	
1.6 MHz	00	1.6 MHz	0	20 kHz	100 Hz
			1	10 kHz	50 Hz
	01	800 kHz	0	10 kHz	50 Hz
			1	5 kHz	25 Hz
	10	400 kHz	0	5 kHz	25 Hz
			1	2.5 kHz	12.5 Hz
	11	200 kHz	0	2.5 kHz	12.5 Hz
			1	1.25 kHz	6.25 Hz

The clock frequency must be set to value higher than the expected I^2C frequency.

3 I²C interface

The features that are supported by the I²C interface are the following ones:

- I²C slave device
- Compliant to Philips I²C specification version 2.1
- Supports standard (up to 100 kbps) and fast (up to 400 kbps) modes.
- 7-bit and 10-bit device addressing modes
- General call
- Start/restart/stop

The address is selected by the state of 2 pins.The state of the pins is read upon reset and then the pins can be configured for normal operation.The pins have a pull-up or down to set the address.The I²C interface module allows the connected host system to access the registers in the STMPE1208S.

Table 4. I²C addresses

ID_1	ID_0	7-bit address	7-bit address	
			Write	Read
0	0	0x58	0xB0	0xB1
0	1	0x59	0xB2	0xB3
1	0	0x5A	0xB4	0xB5
1	1	0x5B	0xB6	0xB7

3.1 Start condition

A start condition is identified by a falling edge of SDATA while SCLK is stable at high state. A start condition must precede any data/command transfer.The device continuously monitors for a start condition and will not respond to any transaction unless one is encountered.

3.2 Stop condition

A stop condition is identified by a rising edge of SDATA while SCLK is stable at high state. A stop condition terminates communication between the slave device and bus master. A read command that is followed by NoAck can be followed by a stop condition to force the slave device into idle mode. When the slave device is in idle mode, it is ready to receive the next I2C transaction. A Stop condition at the end of a write command stops the write operation to registers.

3.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter releases the SDATA after sending eight bits of data. During the ninth bit, the receiver pulls

the SDATA low to acknowledge the receipt of the eight bits of data.The receiver may leave the SDATA in high state if it would to not acknowledge the receipt of the data.

3.4 Data Input

The device samples the data input on SDATA on the rising edge of the SCLK. The SDATA signal must be stable during the rising edge of SCLK and the SDATA signal must change only when SCLK is driven low.

3.5 Slave device address

The slave device address is a 7 or 10-bit address, where the least significant 3-bit are programmable. These 3-bit values will be loaded in once upon reset and after that these 3 pins no longer be needed with the exception during general call. Up to 4 STMPE1208S devices can be connected on a single I^2C bus.

3.6 Memory addressing

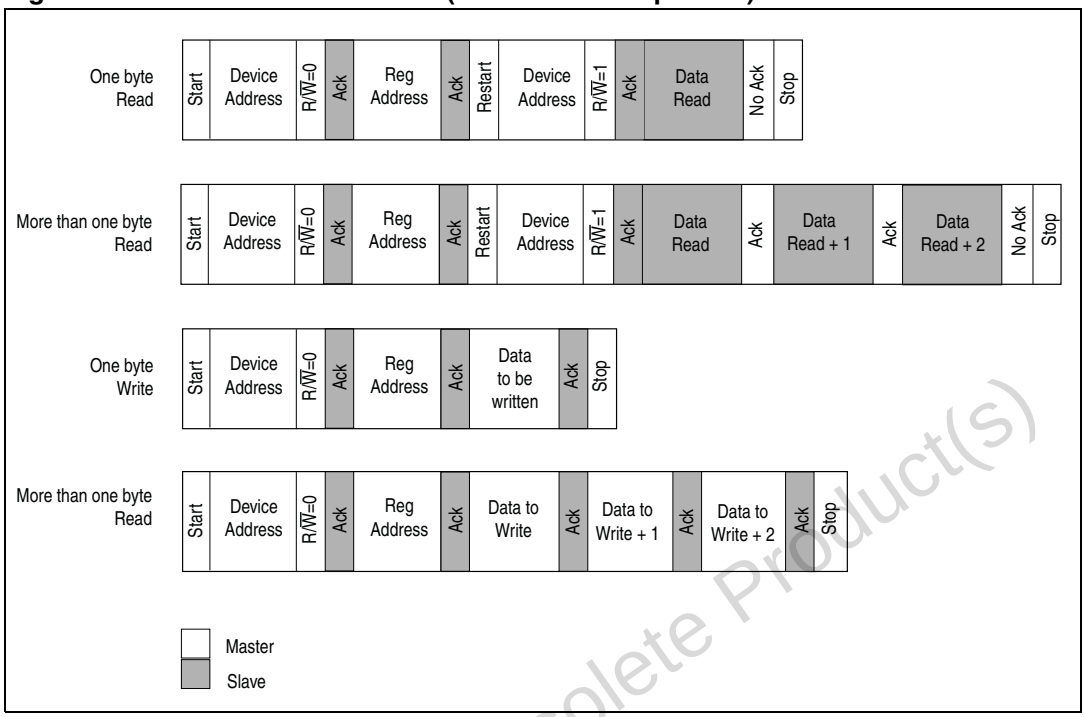
For the bus master to communicate to the slave device, the bus master must initiate a start condition and followed by the slave device address. Accompanying the slave device address, there is a read/bit (R/). The bit is set to 1 for read and 0 for write operation.

If a match occurs on the slave device address, the corresponding device gives an acknowledgement on the SDA during the 9th bit time. If there is no match, it deselects itself from the bus by not responding to the transaction.

Table 5. Operation modes

Mode	Byte	Programming sequence
Read	≥1	Start, device address, R/$\overline{W}$ = 0, register address to be read
		Restart, device address, R/$\overline{W}$ = 1, data read, stop
		If no stop is issued, the data read can be continuously performed. If the register address falls within the range that allows an address auto-increment, then the register address auto-increments internally after every byte of data being read. For those register addresses that fall within a non-incremental address range, the address will be kept static throughout the entire write operations. Refer to the memory map table for the address ranges that are auto and non-increment. An example of such a non-increment address is FIFO
Write	≥1	Start, device address, R/$\overline{W}$ = 0, register address to be written, data write, stop
		If no stop is issued, the data write can be continuously performed. If the register address falls within the range that allows address auto-increment, then the register address auto-increments internally after every byte of data being written in. For those register addresses that fall within a non-incremental address range, the address will be kept static throughout the entire write operations. Refer to the memory map table for the address ranges that are auto and non-increment.

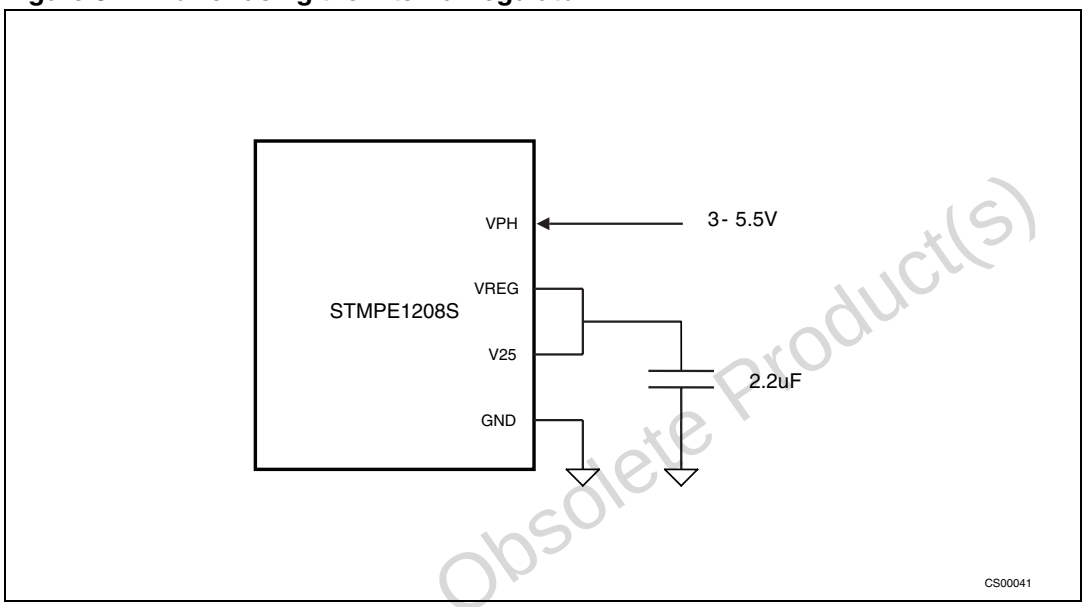
Figure 5. Read and write modes (random and sequential)



4 Power schemes

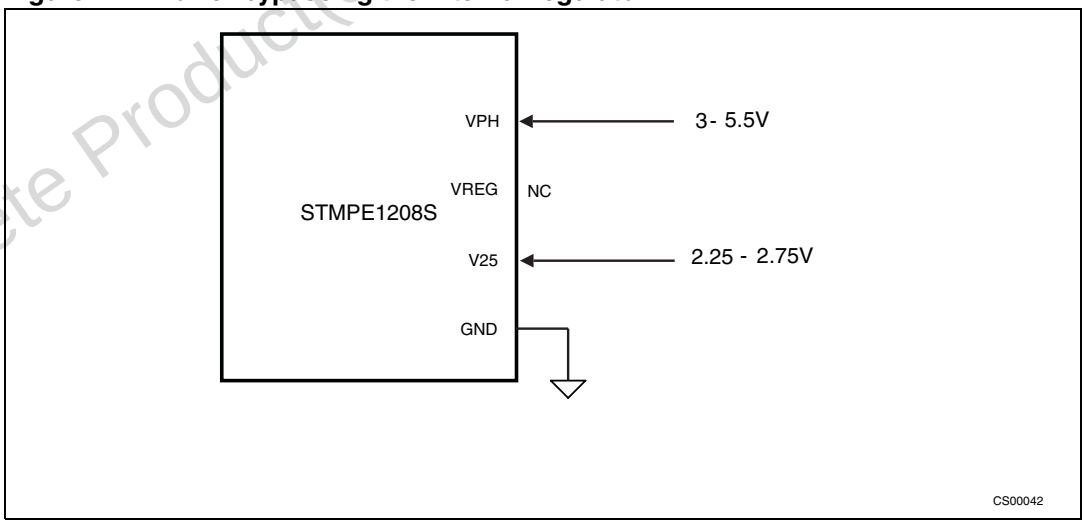
The STMPE1208S can be powered by a 2.5 V supply directly, or 3.0 - 5.5 V supply through the internal voltage regulator.

Figure 6. Power using the internal regulator



1. REG_DISABLE bit in CTRL_2 register = 0

Figure 7. Power bypassing the internal regulator

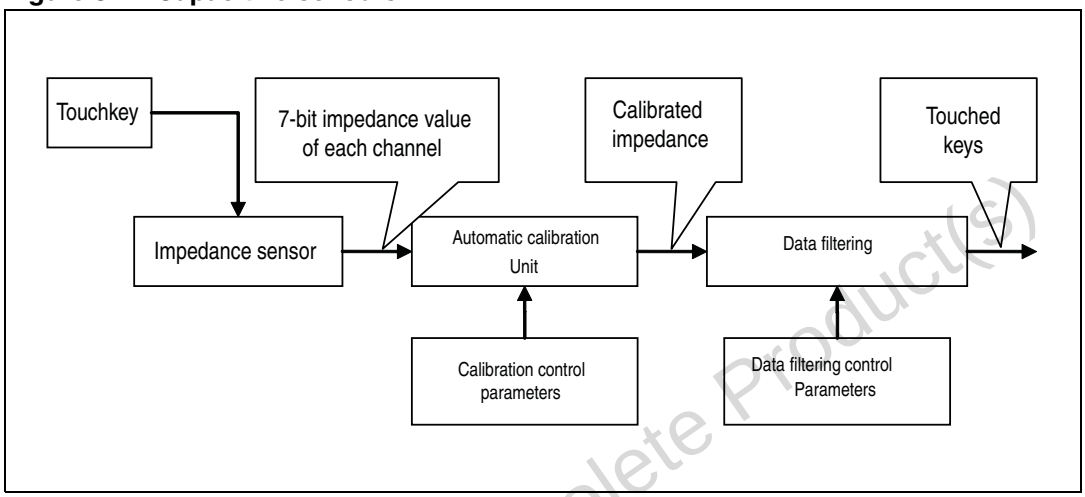


1. REG_DISABLE bit in CTRL_2 register = 1

5 Capacitive sensors

The STMPE1208S capacitive sensor is based on fully digital, impedance change detection engine that is capable of detecting very small change in capacitance.

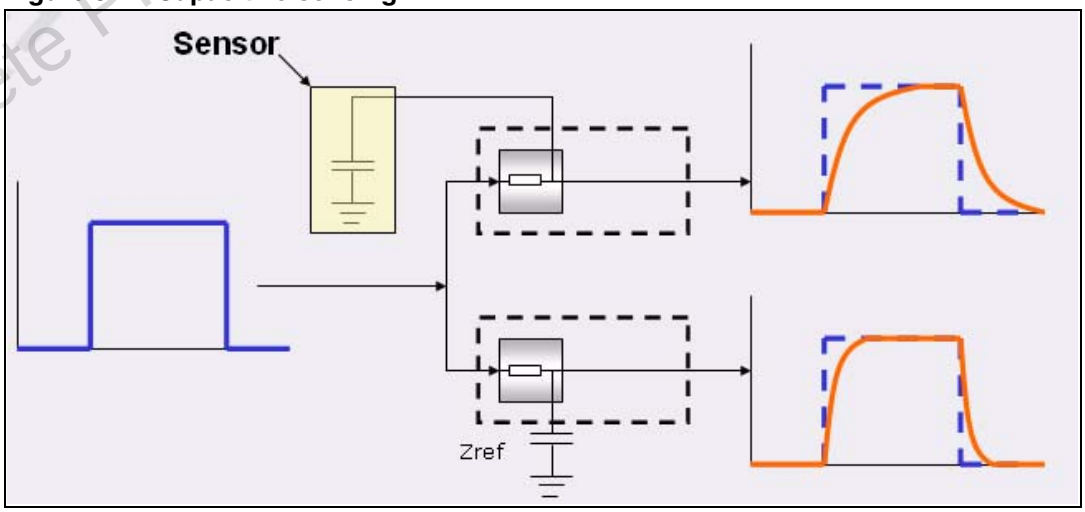
Figure 8. Capacitive sensors



5.1 Capacitive sensing

The STMPE1208S senses a human touch by the additional capacitance introduced to the pad (with respect to ground). This capacitance causes a delay in a clock signal on the sensing pad, and the delay in the sensing pad is compared with a reference clock and the difference is a direct representation of the additional capacitance introduced by the proximity/touch of finger.

Figure 9. Capacitive sensing

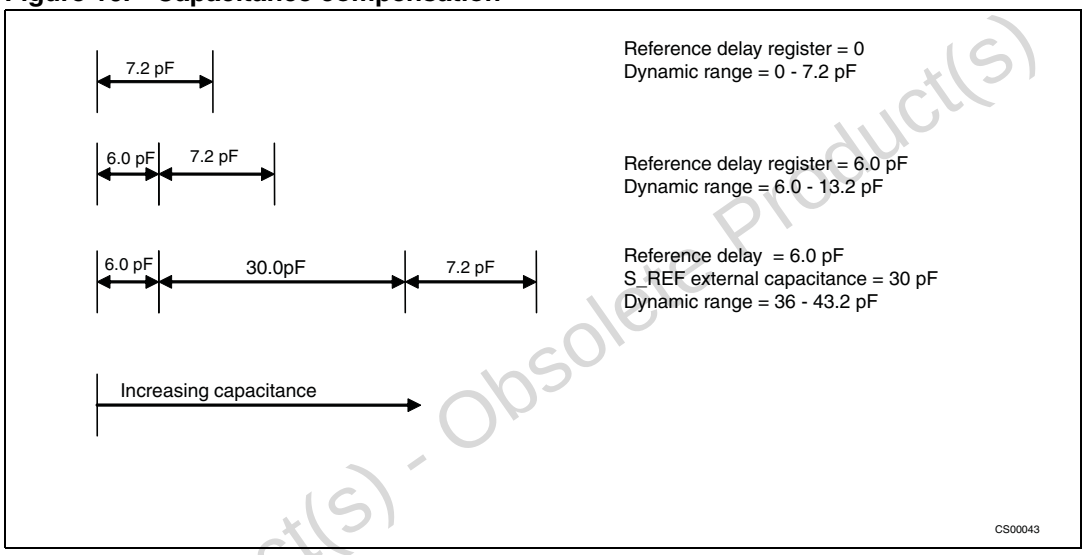


5.2 Capacitance compensation

The STMPE1208S is capable to measuring up to 7.2 pF in capacitance difference between the reference point (Zref) and the individual channels. In the case where the PCB connection between the sensor pads and the device is too long, the "reference delay" register is able to shift the reference by up to 6.0 pF, allowing the touch channels to measure added capacitance 7.2 pF with offset of 6.0 pF, as shown in following diagram.

In case this is still not enough to compensate for the capacitance on sensor lines (due to very long sensor trace), an external capacitor of up to 30 pF can be connected at the A_Ref pin. This allows to further shift up the dynamic range of the capacitance measurement.

Figure 10. Capacitance compensation



The sensed capacitance is accessible to host through the "IMPEDANCE" registers.

5.3 Setting of TVR and EVR

The STMPE1208S uses 2 main parameters to control the sensitivity and calibration of the capacitive sensing system. TVR (touch variance) is a channel-specific value, that specifies the number of steps the sensed capacitance must be above the internal reference, to be considered a touch. Generally, this should be set as 4 –10, but it must be bigger than EVR.

The EVR (environment variance) is a shared value that is applied to all the channels. This specifies the maximum change in capacitance that can be considered due to the shifting of the environmental factor. Generally, this should be set to 1 –5, but it must be less than TVR.

Environment tracking calibration

On power up, a calibration is executed. The initial calibration takes about 150 clock cycles of sensor clock for completion. Using 5 kHz sensor clock, this would be 30 mS.

However, if any of the sensors are touched during powering up, calibration is delayed, until all sensors are untouched. In this case, the time taken for calibration, from the time when all sensors are untouched is:

2 * calibration interval + 150 * sensor clock period

The STMPE1208S maintains 2 parameters for each touch channels: TVR and calibrated impedance. calibrated impedance is an internal reference of which, if the currently measured impedance exceeds the calibrated impedance by a magnitude of TVR, it is considered a touch.

If the impedance is more than the calibrated impedance, but the magnitude does not exceed calibrated impedance by TVR, it is not considered a TOUCH. In this case, 2 scenarios are possible:

1. Environmental changes has caused the impedance to increase

2. Finger is near the sensing pad, but not near enough

In case 1, the change in impedance is expected to be small, as environmental changes are normally gradual. A value "EVR" is maintained to specify the maximum impedance change that is still considered an environmental change.

Table 6. Calibration action under different scenarios

Scenario	Touch sensing and calibration action
IMP>CALIBRATED IMP + TVR	Touch, no calibration
IMP>CALIBRATED IMP + EVR	No touch, no calibration
IMP<CALIBRATED IMP + TVR IMP<CALIBRATED IMP + EVR	No touch, new Calibrated IMP = previous
IMP>CALIBRATED IMP	Calibrated IMP + change in IMP
IMP<CALIBRATED IMP	No touch, new alibrated IMP = new IMP

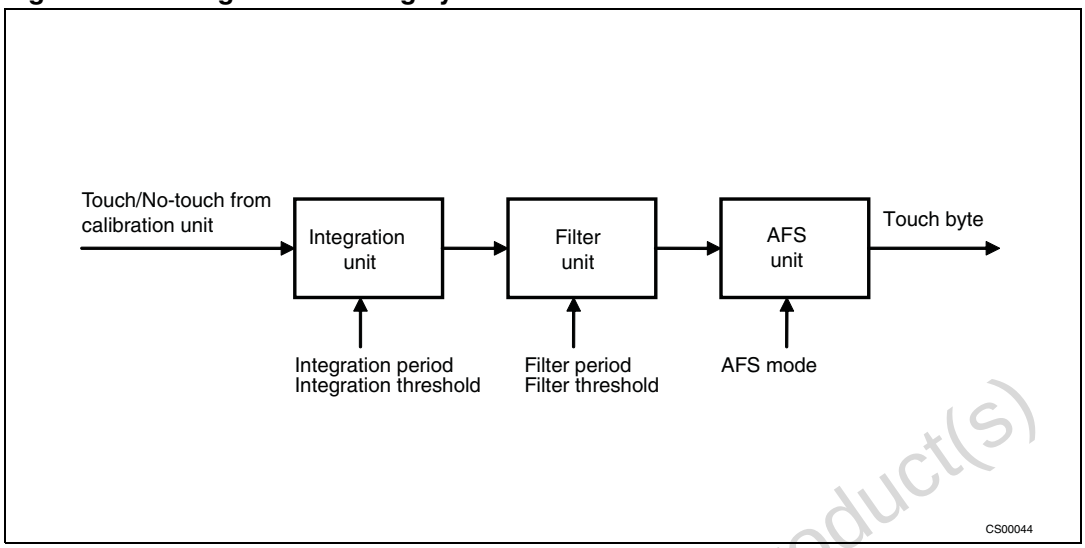
ETC WAIT register state a period of time of which, all touch inputs must remain "no touch" for the next calibration to be carried out.

CAL INTERVAL states the period of time between successive calibrations when there are prolonged no touch condition.

5.3.1 3-stage data filtering system

The output from the calibration unit is an instantaneous "touch" or "no touch" status. This output is directed to the filtering stage where the 2 stage noise filtering and 1 stage data filtering is applied to the touch status.

Figure 11. 3-stage data filtering system



Integration and filtering unit

Touch is sampled across a programmable period of time. The output of the integration stage would be a "strength" (in strength register) that indicates the number of times a "touch" is seen, across the integration period. The "strength" is then compared with the value in "strength threshold" register. If strength exceeds the strength threshold, this is considered a valid touch.

If required, a 2nd stage filtering feature controlled by filter_ period and filter_threshold registers.

In data filtering stage, 3 modes of operation are supported:

AFS Mode 1: Only the touch channel with highest strength is taken

AFS Mode 2: All touch channels with strength > strength threshold is taken

AFS Mode 3: The 2 touch channels with the highest strength are selected.

These modes are selected using the feature selector register.

The final, filtered data is accessible through the touch_byte register.

5.3.2 Noise filtering

When the STMPE1208S is operating in the vicinity of highly emissive circuits (DC-DC converter, PWM controller/drive etc), the sensor inputs will be affected by high-frequency noise. In this situation, the 2-stage time-integrating function could be used to distinguish between real touch, or emission-related false touch.

5.3.3 BEEP output

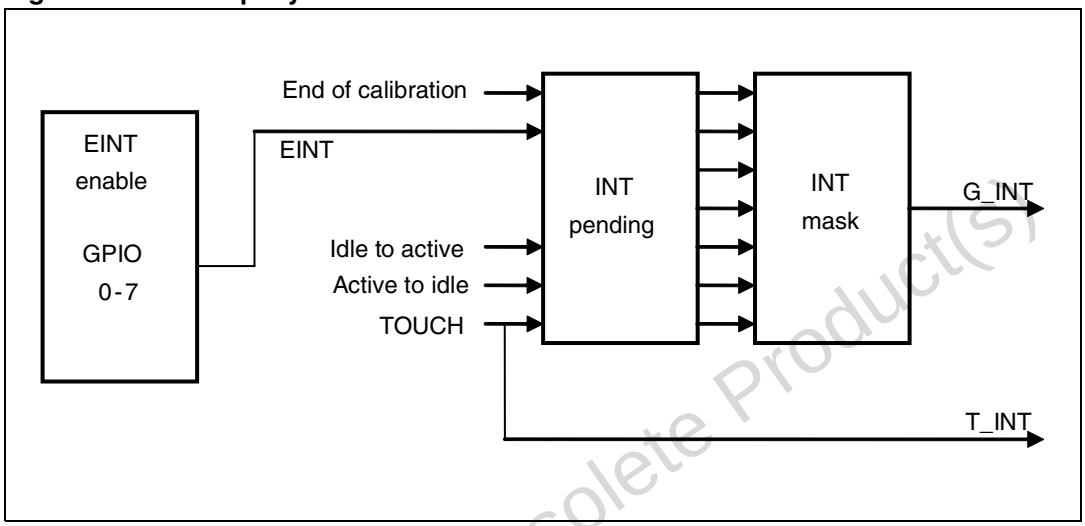
STMPE1208S is able to drive an external piezo buzzer directly with the built-in beep generator. The beep output can be programmed to varies from 1.5 kHz to 400 kHz, with period of 100 µS to 2.5 S.

5.3.4 Interrupt system

2 interrupt pins are available in STMPE1208S for different application needs.

- G_INT asserts when there are any unmasked interrupt events
- T_INT asserts when there are any touch events

Figure 12. Interrupt system



1. G_INT is cleared by writing to the INT CLEAR register
2. T_INT is cleared by reading the Touch Byte register

6 Register map and function description

This section lists and describes the registers of the STMPE1208S device, starting with a register map and then detailed descriptions of register types.

Table 7. Register summary map table

Address	Module register	Type	Reset value	Description
0x00	FEATURE_SEL	R/W	0x04	Feature selection
0x01 –0x0C	TVR 0 –11	R/W	0x08	TVR (touch variance) setting of each capacitive channel
0x0D	EVR	R/W	0x04	EVR (enviromental variance) setting of all 12 channels
0x0E	ETC_WAIT	R/W	0x27	Wait time for calibration
0x0F	REF_DELAY	R/W	0x00	Value of reference delay chain
0x10 – 0x1B	STRENGTH_THRES	R/W	0x01	Setting of strength threshold for each channel
0x1C	INTEGRATION_ TIME	R/W	0x0F	Integration time for AFS mode
0x1D	IDLE_TIME	R/W	0x0F	Period to enter IDLE mode after non-activity
0x1E	GPIO_REG_L	R/W	0x00	Output state of I/O if configured as GPIO
0x1F	GPIO_REG_H	R/W	0x00	Output state of I/O if configured as GPIO
0x20	GPIO_CFG_L	R/W	0x00	To configure I/O as GPIO or direct capacitive measurement output
0x21	GPIO_CFG_H	R/W	0x00	To configure I/O as GPIO or direct capacitive measurement output
0x22	GPIO_DIR_L	R/W	0x00	Direction of GPIO
0x23	GPIO_DIR_H	R/W	0x00	Direction of GPIO
0x24	CTRL_1	R/W	0x00	Functional control of capacitive sensing
0x25	CTRL_2	R/W	0x00	Functional control of capacitive sensing
0x26	INT_MASK	R/W	0x00	Mask for GINT interrupt sources
0x27	INT_CLR	R/W	0x00	Writing this register clears the INT pending register
0x28	BEEP_PER	R/W	0x00	Set the period of beep output
0x29	BEEP_FREQ	R/W	0x00	Set the frequency of beep output

Table 7. Register summary map table (continued)

Address	Module register	Type	Reset value	Description
0x2A	CAL_INTERVAL	R/W	0x30	Set the interval between calibrations
0x2B	EXT_INT_EN	R/W	0x00	Enable for GPIO interrupt
0x2C	EXT_INT_POL	R/W	0x00	Polarity of GPIO interrupt
0x2D	FILTER_PERIOD	R/W	0x00	Set the period for filter feature
0x2E	FILTER_TRES	R/W	0x00	Set the threshold of filter feature
0x50 –0x5B	STRENGHT	R	0x00	Strength recorded during each integration period in AFS mode
0x5C –0x67	CAL_IMP	R	0x00	Reference impedance of each channel after ETC calibration
0x68 –0x73	IMP	R	0x00	Measured impedance of each channel
0x74	STA	R	0x00	Power management mode
0x75	TOUCH_BYTE_L	R	0x00	Touch sensing data output
0x76	TOUCH_BYTE_H	R	0x00	Touch sensing data output
0x77	INT_PENDING	R	0x00	Status of GINT interrupt sources
0x78	GPIO_IN_L	R	0x00	GPIO input states can be read here
0x79	GPIO_IN_H	R	0x00	GPIO input states can be read here
0xF8	CLK_SRC_INTERN	W	–	
0xF9	CLK_SRC_EXT	W	–	
0xFA	BIAS_OFF	W	–	
0xFB	BIAS_ON	W	–	
0xFC	WAKEUP_SLEEP	W	–	
0xFD	ENTER_SLEEP	W	–	
0xFE	COLD_RST	W	–	
0xFF	WARM_RST	W	–	

FEATURE_SEL Feature selection register

7	6	5	4	3	2	1	0
RESERVED				AFS3	AFS2	AFS1	FILTER_EN

Address: 0x00

Type: R/W

Reset: 0x04

Description: The feature selection register is used to select the AFS mode and filter enable

[7:4] RESERVED

[3] AFS3: write '1' to enable AFS mode 3 (two strongest keys only)

[2] AFS2: write '1' to enable AFS mode 2 (all keys above threshold)

[1] AFS1: write '1' to enable AFS mode 1 (one strongest key only)

[0] FILTER_EN: write '1' to enable filter feature

Note: only one bit among AFS1, AFS2, AFS3 could be set to '1' at the same time. If more than one are set to '1', results of the operation would be unpredictable.

TVR Touch variance register [0-11]

7	6	5	4	3	2	1	0
-	TVR [6:0]						

Address: 0x01 - 0x0C

Type: R/W

Reset: 0x08

Description: Setting the TVR between 0 - 99

A high TVR value decreases the sensitivity of the sensor, but increasing its tolerance to ambient noise. A small TVR value increases the sensitivity.

Each step of TVR is equivalent to a capacitance of 60 fF

Recommended value to TVR is 4-8.

[7] Reserved

[6:0] TVR [6:0]

EVR Enviromental variance register

7	6	5	4	3	2	1	0
-	EVR [6:0]						

Address: 0x0D

Type: R/W

Reset: 0x04

Description: EVR is used to detect "Non-Touch" condition. Each step of EVR is equivalent to a capacitance of 60 fF. Recommended value to EVR is 2-6 (EVR must always be smaller than TVR).

[7] Reserved

[6:0] EVR [6:0]

ETC_WAIT Enviromental tracking calibration wait time

7	6	5	4	3	2	1	0
ETC_WAIT [7:0]							

Address: 0x0E

Type: R/W

Reset: 0x27

Description: Wait time for ETC operation, from the first instance of all 12 keys returning to no-touch status. ETC wait time = ETC_wait[7:0] *64 *clock period. A "non-touch" condition must persist for this wait time, before an ETC operation is carried out.

[7:0] ETC_WAIT [7:0]

REFERENCE_DELAY Reference delay

7	6	5	4	3	2	1	0
RESERVED	REFERENCE_DELAY						

Address: 0x0F

Type: R/W

Reset: 0x00

Description: Reference delay register. Valid range = 0-128. Each step represents capacitance value of 60 pF. Warm reset is required after this value is updated.

[7] Reserved

[6:0] Reference_delay:
Valid range= 0-127
Each step represents capacitance value of 0.06 pF
Warm reset is required after this value is updated

STRENGTH_THRES Strength threshold

7	6	5	4	3	2	1	0
STRENGTH_THRESHOLD							

Address: 0x10 - 0x1B

Type: R/W

Reset: 0x01

Description: Setting threshold to be used in AFS mode to determin a valid touch.

[7:0] Strength_threshold

INTEGRATION_TIME Integration time register

7	6	5	4	3	2	1	0
INTEGRATION_TIME							

Address: 0x1C

Type: R/W

Reset: 0x0F

Description: Integration time in AFS mode.

[7:0] Integration_time:
Total period of integration = sensor clock period * integration time [7:0]

IDLE_TIME Idle time register

7	6	5	4	3	2	1	0
IDLE_TIME							

Address: 0x1D

Type: R/W

Reset: 0x0F

Description: The device enters in idle state if there is not touch detected for a period equal to idle time [7:0] * 5000 * clock_sensor_period.

[7:0] IDLE_TIME

GPIO_STA_L GPIO state register L

7	6	5	4	3	2	1	0
IO-7	IO-6	IO-5	IO-4	IO-3	IO-2	IO-1	IO-0

Address: 0x1E

Type: R/W

Reset: 0x00

Description: If a DIO is set to function as GPIO (GPIO_CFG register) and output (GPIO_DIR register), the bits in this register would determine the output value of the corresponding GPIO. Applicable for GPIOs 0 - 7.

GPIO_STA_H GPIO state register H

7	6	5	4	3	2	1	0
RESERVED				IO-11	IO-10	IO-9	IO-8

Address: 0x1F

Type: R/W

Reset: 0x00

Description: If a DIO is set to function as GPIO (GPIO_CFG register) and output (GPIO_DIR register), the bits in this register would determine the output value of the corresponding GPIO. Applicable for GPIOs 8 - 11.

GPIO_CFG_L GPIO configuration register

7	6	5	4	3	2	1	0
IO-7	IO-6	IO-5	IO-4	IO-3	IO-2	IO-1	IO-0

Address: 0x20

Type: R/W

Reset: 0x00

Description: Writing ‘1’ in this GPIO configuration register sets the corresponding DIO as GPIO. Applicable for GPIOs 0-7.

GPIO_CFG_H GPIO configuration register

7	6	5	4	3	2	1	0
RESERVED				IO-11	IO-10	IO-9	IO-8

Address: 0x21

Type: R/W

Reset: 0x00

Description: Writing ‘1’ in this GPIO configuration register sets the corresponding DIO as GPIO. Applicable for GPIOs 8-11.

GPIO_DIR_L GPIO direction register

7	6	5	4	3	2	1	0
IO-7	IO-6	IO-5	IO-4	IO-3	IO-2	IO-1	IO-0

Address: 0x22

Type: R/W

Reset: 0x00

Description: Writing '1' in this register sets the corresponding GPIO as input. Writing '0' in this register sets the corresponding GPIO as output. Applicable for GPIOs 0-7.

GPIO_DIR_H GPIO direction register

7	6	5	4	3	2	1	0
RESERVED				IO-11	IO-10	IO-9	IO-8

Address: 0x23

Type: R/W

Reset: 0x00

Description: Writing '1' in this register sets the corresponding GPIO as input. Writing '0' in this register sets the corresponding GPIO as output. Applicable for GPIOs 8-11.

CTRL_1 Control register 1

7	6	5	4	3	2	1	0
-	F2A	PDIV[1:0]		NDIV	HDC_U	HDC_C	HOLD_C

Address: 0x24

Type: R/W

Reset: 0x00

Description: Control register.

[7] Reserved

[6] F2A:
Write '1' to force the device to stay in active mode at all times. For best performance and stability, this bit must be set to ‘1’ at all times.

[5:4] PDIV[1:0]:
'00' : System clock = 1.6MHz
'01' : System clock = 800KHz
'10' : System clock = 400KHz
'11' : System clock = 200KHz

[3] NDIV:
Sensor clock frequency setting:
'0' :sensor clock = system clock / 80
'1' :sensor clock = system clock / 160
Initial calibration time = sensor clock * 150

[2] HDC_U:
Unconditional host driven calibration. Executes an unconditional calibration. This is valid only if "Hold C" bit is set, and device in Active mode. Reads '0' when calibration is completed.

[1] HDC_C:
Conditional host driven calibration. Executes a calibration if no touch is being sensed.

[0] HOLD_C:
'0' for auto-calibration mode
'1' disables auto-calibration

CTRL_2 Control register 2

7	6	5	4	3	2	1	0
RESERVED				REGD	SCD	BEEP_ON	INT_POL

Address: 0x25

Type: R/W

Reset: 0x00

Description: Control register.

[7:4] Reserved

[3] REGD:
'0' to enable internal regulator (default)
'1' to disable

[2] SCD: Sensor clock disable.
Write '1' to disable sensor clock.

[1] BEEP_EN:
'1' to enable beep output

[0] INT_POL: Interrupt polarity
'0' for rising edge
'1' for falling edge

INT_MASK Interrupt mask

7	6	5	4	3	2	1	0
-	EOC	EINT	-		I2A	A2I	TOUCH

Address: 0x26

Type: R/W

Reset: 0x08

Description: Writing '1' to this register disables the corresponding interrupt source.

[7] Reserved

[6] EOC:
End of calibration.

[5] EINT:
EINT interrupt sources (GPIO input) changes.

[4:3] Reserved

[2] I2A:
SLEEP to active transition

[1] A2I:
Active to idle transition

[0] Touch:
Touch detect.

INT_CLR Interrupt clear register

7	6	5	4	3	2	1	0
-	EOC	EINT	-		I2A	A2I	TOUCH

Address: 0x27

Type:

Reset: 0x00

Description: If the corresponding bit in the INT_PENDING register is set, system software must write '1' to this register to clear the bits in INT_PENDING register.

[7] Reserved

[6] EOC:
End of calibration.

[5] EINT:
EINT interrupt sources (GPIO input) changes.

[4:3] Reserved

[2] I2A:
Sleep to active transition

[1] A2I:
Active to idle transition

[0] Touch:
Touch detect.

BEEP_PERIOD Beep period

7	6	5	4	3	2	1	0
BEEP_PERIOD [7:0]							

Address: 0x28

Type: R/W

Reset: 0x00

Description: Beep period

[7:0] Beep_period:
Period = beep period [7:0] * 8* system clock period

System clock period = 0.625 µs (1.6 MHz) to 5 µs (200 kHz)
Period of beep (min) = 0.625 µs * 8* 1 = 5 µs
Period of beep (max) = 5 µs * 8* 255 = 10 ms

BEEP_FREQUENCY — Beep frequency

7	6	5	4	3	2	1	0
BEEP_FREQUENCY[7:0]							

Address: 0x29

Type: R/W

Reset: 0x00

Description: Beep frequency in kHz = system clock/(beep frequency [7:0]*2)+2)

[7:0] Beep_frequency:
Min Freq = 200 kHz/512 = 390 Hz
Max Freq = 1.6 MHz/2 = 800 kHz

CAL_INTERVAL — Calibration interval

7	6	5	4	3	2	1	0
INTERVAL[7:0]							

Address: 0x2A

Type: R/W

Reset: 0x30

Description: Calibration interval

[7:0] Interval:
Interval between calibration = Calibration Interval [7:0] * sensor clock period * 50

EXT_INT_EN — External interrupt enable register

7	6	5	4	3	2	1	0
IO-7	IO-6	IO-5	IO-4	IO-3	IO-2	IO-1	IO-0

Address: 0x2B

Type: R/W

Reset: 0x00

Description: Enable of the GPIO interrupt.

'1' enables the corresponding GPIO to generate an interrupt on detecting change in its input. Only GPIO 0-7 is able to generate interrupts.

EXT_INT_POL External interrupt polarity register

7	6	5	4	3	2	1	0
IO-7	IO-6	IO-5	IO-4	IO-3	IO-2	IO-1	IO-0

Address: 0x2B

Type: R/W

Reset: 0x00

Description: Polarity of GPIO interrupt.

‘0’ positive edge on external interrupt input sets GINT.

‘1’ negative edge on external interrupt input sets GINT.

FILTER_PERIOD Filter period

7	6	5	4	3	2	1	0
FILTER_PERIOD[7:0]							

Address: 0x2D

Type: R/W

Reset: 0x00

Description: Filter period.

[7:0] Filter_count:

Additional filter to stabilize touch output in AFS mode.

AFS touch output is monitored for filter period [7:0] times every integration time. For each time a "touch status" is detected, an internal "filter counter" is incremented once. This counter value is then compared with filter threshold (register 0x3E).

FILTER_THRESHOLD Filter threshold

7	6	5	4	3	2	1	0
FILTER_THRESHOLD							

Address: 0x2E

Type: R/W

Reset: 0x00

Description: Filter threshold.

[7:0] Filter_Thershold:

An internal "filter counter" is compared with filter threshold [7:0] to determine if a valid touch has occurred.

Note: I^2C writes to this register will not be acknowledged. However as long as I^2C timing is followed, the writing to this register will work correctly.

STRENGTH Strength

7	6	5	4	3	2	1	0
STRENGTH							

Address: 0x50 - 5B

Type: R

Reset: 0x00

Description: Counts the number of times a sensed impedance exceeds calibrated reference impedance over and integration time. Maximum strength equals integration time [7:0]

[7:0] STRENGTH:

Read-only field.

CALIBRATED_IMPEDANCE Calibrated impedance

7	6	5	4	3	2	1	0
CAL_IMPEDANCE							

Address: 0x5C - 0x67

Type: R

Reset: 0x00

Description: Calibrated reference impedance = 128 - CAL.Impedance[7:0].

[7:0] CAL_IMPEDANCE:
Calibrated reference impedance.

IMPEDANCE Impedance

7	6	5	4	3	2	1	0
IMPEDANCE							

Address: 0x68 - 0x73

Type: R

Reset: 0x00

Description: Impedance is the instantaneous impedance value seen at the input pin of each cap. sensing pin.

[7:0] Impedance:
Currently sensed impedance

STATUS Status register

7	6	5	4	3	2	1	0
RESERVED							IDLE

Address: 0x74

Type: R

Reset: 0x00

Applicability:

Description: IDLE: Reads '1' if device is currently in IDLE mode, reads '0' if device is not in IDLE mode

[7:6] RESERVED

[0] IDLE:
Currently sensed impedance

TOUCH_BYTE_L Touch byte L

7	6	5	4	3	2	1	0
CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Address: 0x75

Type: R

Reset: 0x00

Description: CH n: Reads the touch status of channel n (n=0-7). If the key is touched (Impedance > calibrated impedance + TVR), the corresponding bit in this register will read '1'. Reading touch_byte_l and touch_byte_h will clear the TINT assertion.

TOUCH_BYTE_H Touch byte H

7	6	5	4	3	2	1	0
RESERVED				CH11	CH10	CH9	CH8

Address: 0x76

Type: R

Reset: 0x00

Description: CH n: Reads the touch status of channel n (n=8-11). If the key is touched (impedance > calibrated impedance + TVR), the corresponding bit in this register will read '1'. Reading touch_byte_l and touch_byte_h will clear the TINT assertion.

[7:4] RESERVED

[3] CH11:

[2] CH10:

[1] CH9:

[0] CH8:

INT_PENDING Interrupt pending

7	6	5	4	3	2	1	0
RESERVED				EOC	I2A	A21	TOUCH

Address: 0x77

Type: R

Reset: 0x00

Description: This register reflects the status of various possible interrupt sources. Upon the occurrence of an event, the corresponding bit in this register will be set to '1' by the hardware.

[7:4] Reserved

[3] EOC:
End of calibration

[2] I2A:
Sleep to active transition

[1] A21:
Active to sleeptransition

[0] Touch:
Touch detect

GPIO_IN_L GPIO input state (lower) register

Address: 0x79

Type: R

Reset: 0x0

Description: Reads the current logical level of corresponding DIO if it is set as GPIO input.

GPIO_IN_H GPIO input state (higher) register

Address: 0x7A

Type: R

Reset: 0x00

Description: Reads the current logical level of corresponding DIO if it is set as GPIO input.

7 Command registers

The command registers do not have a data field. The device carries out a predetermined operation upon receiving a write access to these address offset. However, a dummy data-phase is used to complete the I^2C transaction.

Table 8. Command registers

Command	Operation
0xF8 CLK_SRC_INTERNAL	Use internal OSC as clock source
0xF9 CLK_SRC_EXTERNAL	Use TCLK pin as clock source
0xFA BIAS_OFF	Turns OFF biasing for internal LDO When external supply is used for V25, turning OFF the biasing for internal LDO reduces current consumption
0xFB BIAS_ON	Turns ON biasing for internal LDO
0xFC Wake up	Exits from sleep and enters active mode
0xFD Enter sleep	Enter sleep mode
0xFE Cold reset	Resets all states and registers
0xFF Warm reset	Resets internal state machines, register values remain the same NOTE: I^2C WRITE TO THIS REGISTER WILL NOT BE ACKNOWLEDGED. However as long as I^2C timing is followed, the writing to this register will work correctly

Figure 13. Software interface (G_INT based)

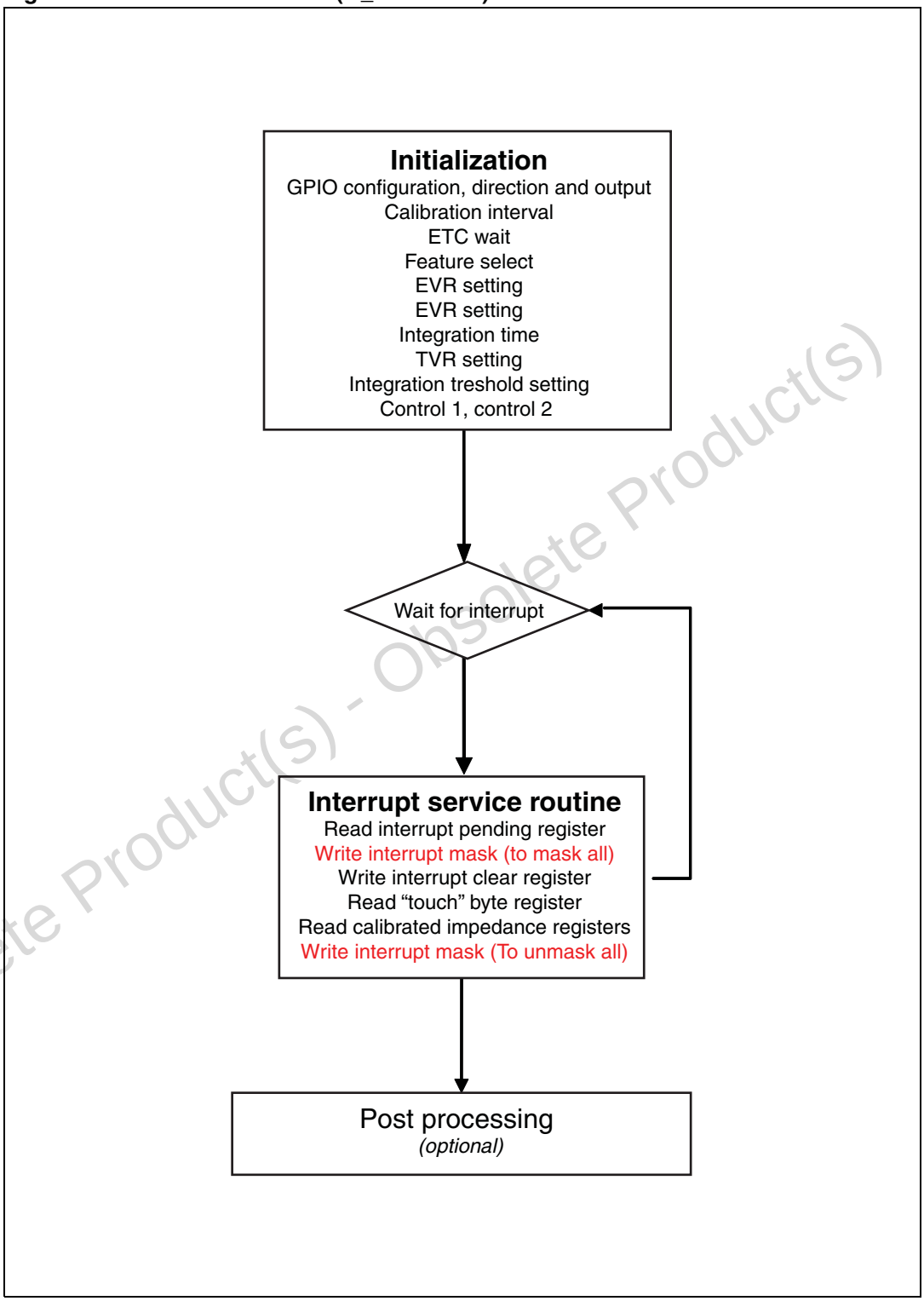
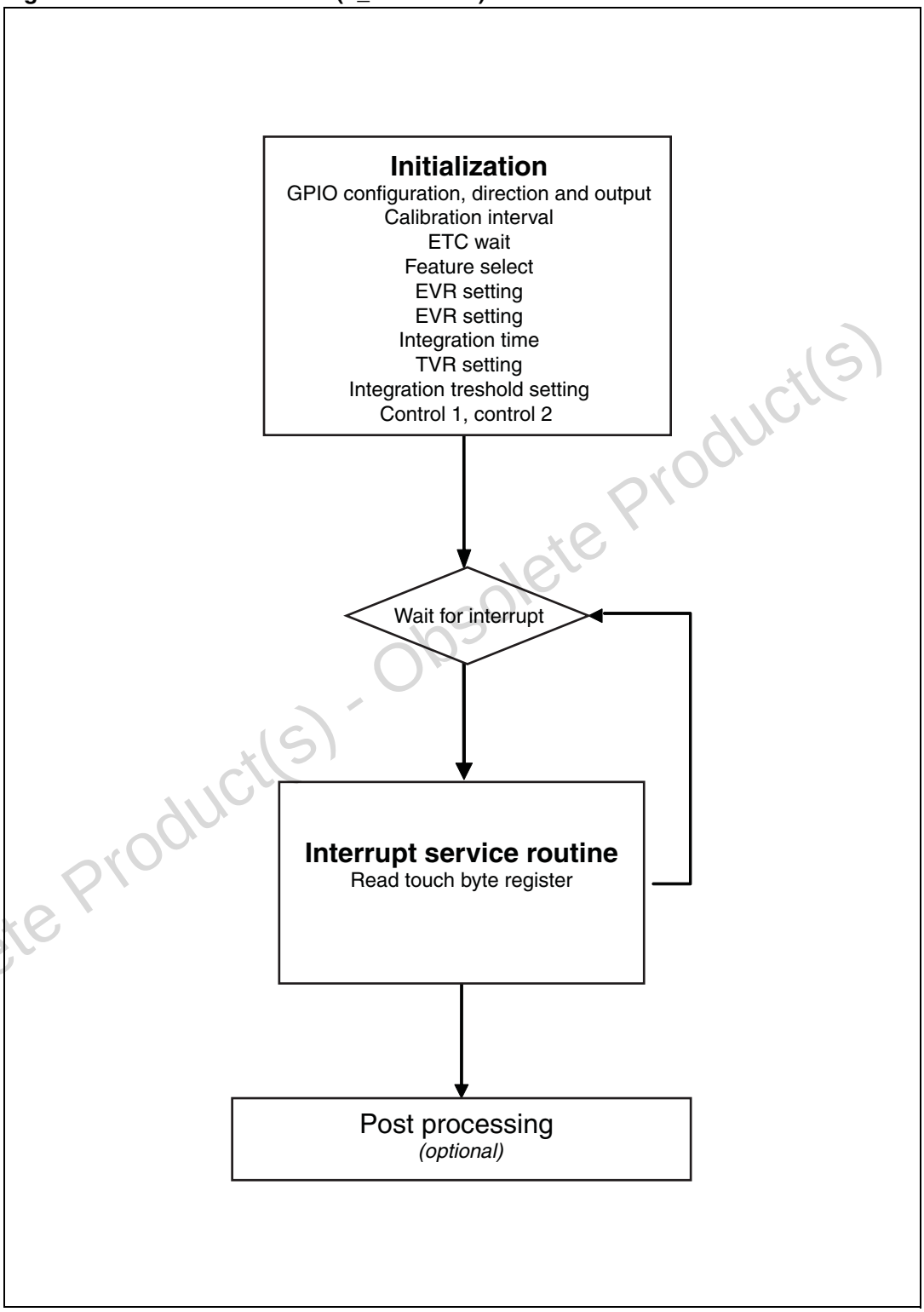


Figure 14. Software interface (T_INT based)



8 Maximum rating

Stressing the device above the rating listed in the “Absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
Vph	Power supply	3.0	-	5.5	V
V25	Power supply	2.15	-	2.90	V
V_{IN}	Digital input	-0.3	-	V_{PH} +0.3	V
T_J	Operating temperature	-40	-	85	°C
T_S	Storage temperature	-55	-	95	°C
ESD	HBM on capacitive sensor pins	-	7	-	kV

8.1 Recommended operating conditions

Table 10. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
Vph	Power supply	3.0	-	5.5	V
V25	Power supply	2.25	2.5	2.75	V
T_J	Operating temperature	-40	25	85	°C

9 Electrical specifications

Table 11. DC electrical characteristics (-40 –85 °C unless otherwise stated)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
I_{out}	GPIO driving current	Vout = 0.75*VPH	-	-	2	mA
I_{active}	Active current	Touch present	-	98	160	µA
I_{idle}	Idle current	No-touch	-	60	80	µA
I_{sleep}	Sleep current	Sleep mode	-	0.1	1	µA
V_{IL}	Digital input low		-	-	1.0	V
V_{IH}	Digital input high		0.7Vph	-	-	V
V_{OL}	Digital output low		-	-	1.0	V
V_{OH}	Digital output high		Vph-0.5	-	-	V
I_{out}	GPIO drive current		-	-	2	mA
I_{in}	GPIO sink current	Total sink current on all GPIOs 〈 80 mA	-	-	10	mA
$I_{leakage}$	Input leakage	V_{IN} = 5.5 V V_{PH} = 5.5 V	-	0.2	2	µA

10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 12. QFN40 (5 x 5 mm) mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	-	0.05
A3		-0.203 ref	
b	0.15	0.20	0.25
D		5.00 BSC	
E		5.00 BSC	
D2	3.70	3.80	3.90
E2	3.70	3.80	3.90
e		0.40 BSC	
L	0.30	0.35	0.40
L1	-	-	0.10
P	-	45° BSC	-
aaa	-	0.15	-
ccc	-	0.10	-

Figure 15. QFN40 (5 x 5 mm) package outline

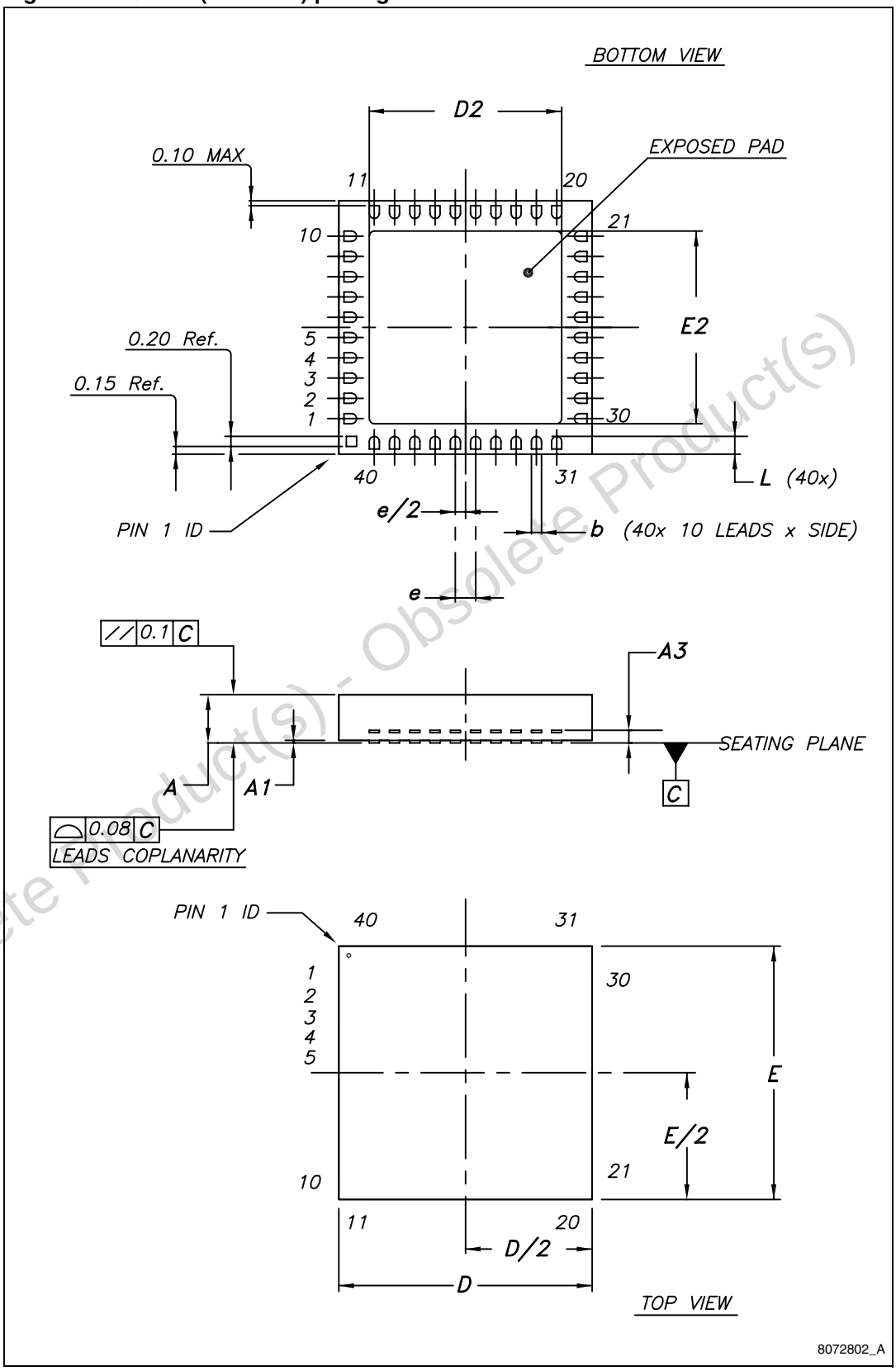


Figure 16. QFN40 recommended footprint without ground pad VIA

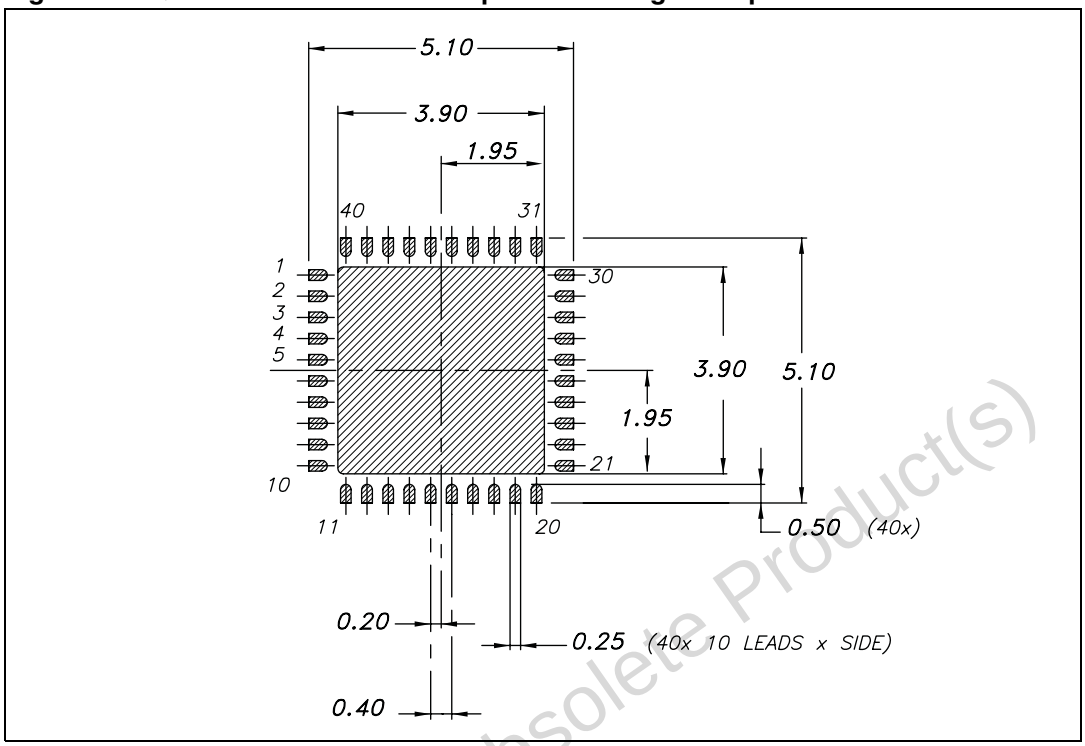


Figure 17. QFN40 recommended footprint with ground pad VIA

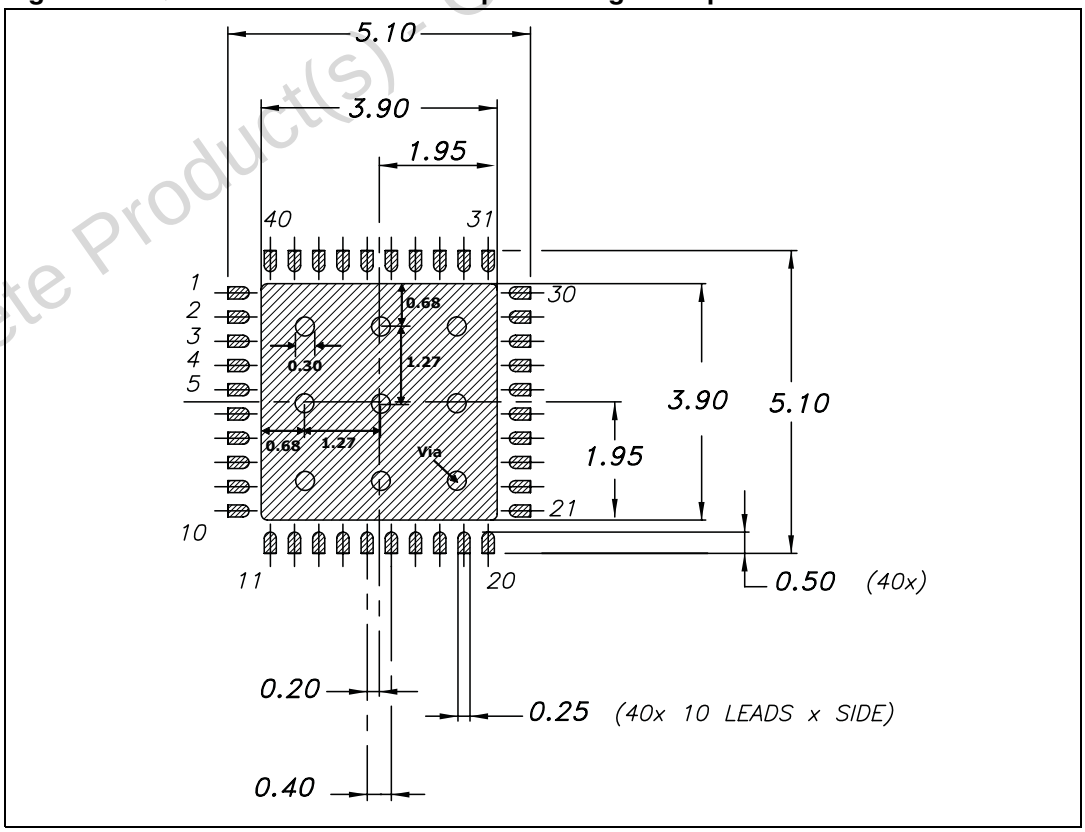


Figure 18. QFN40 tape information

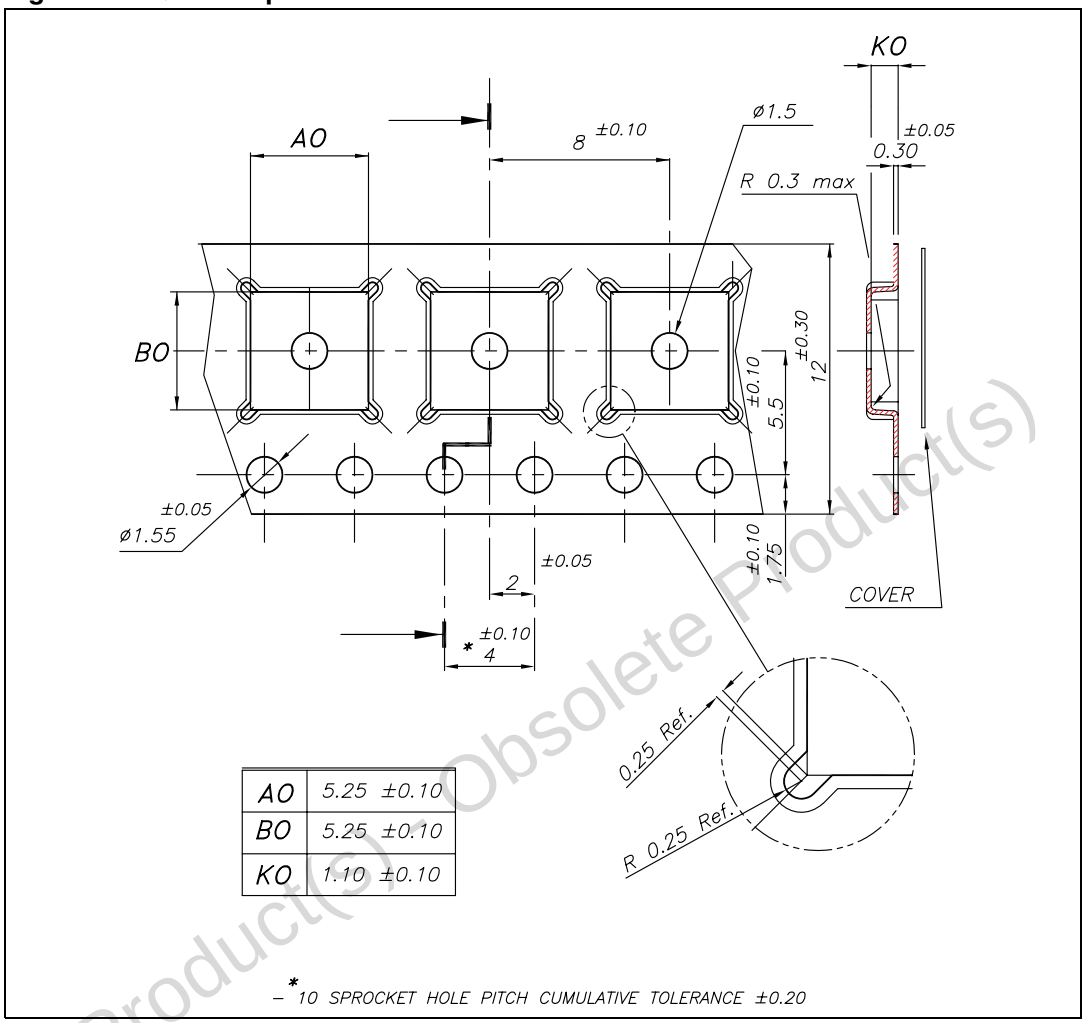
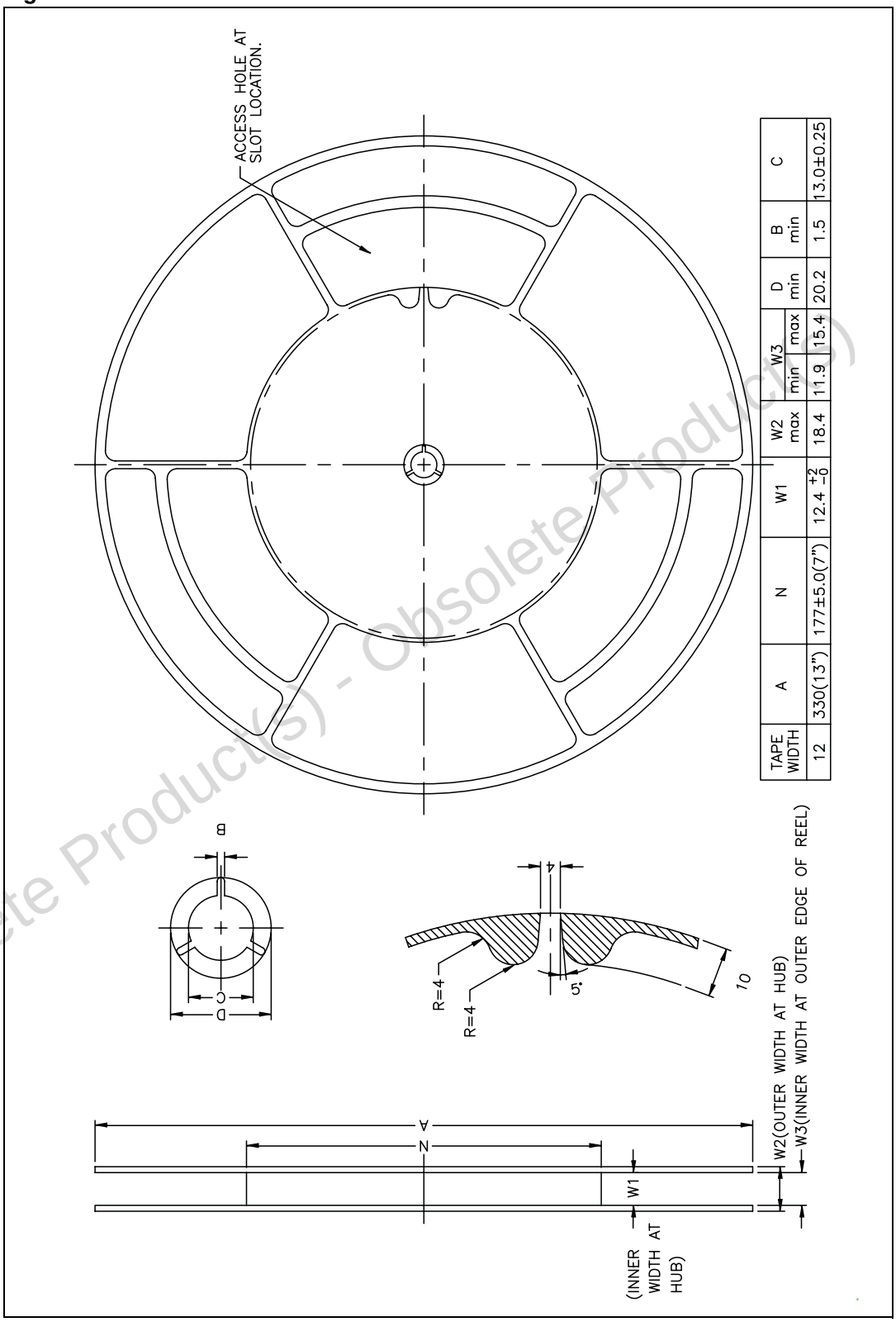


Figure 19. Reel information



TAPE WIDTH	A	N	W1	W2 max	W3 min	W3 max	D min	B min	C
12	330(13")	177±5.0(7")	12.4 $^{+2}_{-0}$	18.4	11.9	15.4	20.2	1.5	13.0±0.25

11 Revision history

Table 13. Document revision history

Date	Revision	Changes
14-Feb-2008	1	Initial release.
04-Jun-2008	2	Modified title in cover page and ETC_WAIT register description. Updated: *Table 5: Operation modes on page 12* Added *Figure 16: QFN40 recommended footprint without ground pad VIA on page 43*.
18-Jul-2008	3	Document status promoted from preliminary data to datasheet. Modified: Beep_period and beep_frequency registers description, HBM ESD protection value, *Table 2: Pin assignments and description on page 6* and *Chapter 10: Package mechanical data on page 41*. Updated: *Section 8: Maximum rating on page 39* and *Section 9: Electrical specifications on page 40*.
26-May-2008	4	Modified: *Table 9* and *Table 10*.
18-Dec-2009	5	Modified: title, operating voltage in the features and power supply values in *Table 9* and *Table 10*.

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