



# STP52N25M5

N-channel 250 V, 0.055  $\Omega$ , 28 A, TO-220  
MDmesh™ V Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STP52N25M5	250 V	< 0.065 $\Omega$	28 A

- Amongst the best R<sub>DS(on)</sub>\* area
- High dv/dt capability
- Excellent switching performance
- Easy to drive
- 100% avalanche tested

## Application

- Switching applications

## Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

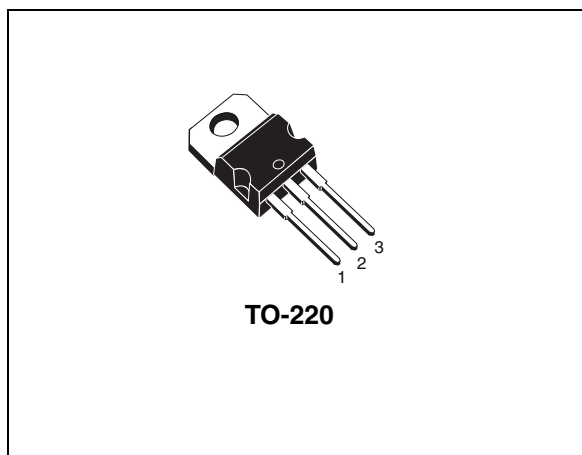


Figure 1. Internal schematic diagram

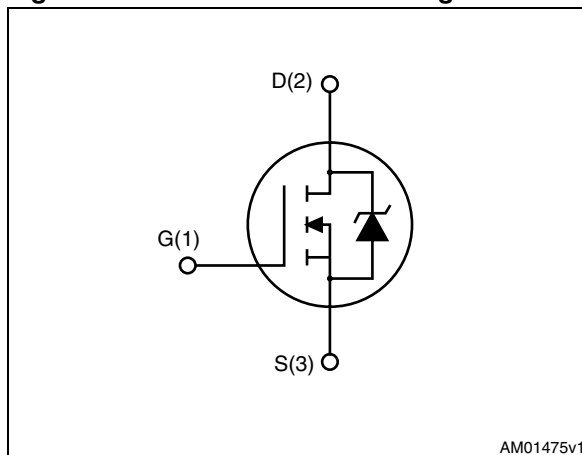


Table 1. Device summary

Order code	Marking	Package	Packaging
STP52N25M5	52N25M5	TO-220	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	25	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	28	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	18	A
$I_{DM}^{(1)}$	Drain current (pulsed)	112	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	110	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	10	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	230	mJ
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 28\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{Peak} < V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.14	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-pcb max	62.5	$^{\circ}\text{C}/\text{W}$
$T_J$	Maximum lead temperature for soldering purpose	300	$^{\circ}\text{C}/\text{W}$

## 2 Electrical characteristics

(T<sub>case</sub> = 25 °C unless otherwise specified).

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}$ , $V_{GS} = 0$	250			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125 \text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25 \text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100 \mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 14 \text{ A}$		0.055	0.065	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 50 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{GS} = 0$	-	1770 110 17	-	pF pF pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0$ , $V_{DS} = 0 \text{ to } 80\%$ $V_{(BR)DSS}$	-	93	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related	$V_{GS} = 0$ , $V_{DS} = 0 \text{ to } 80\%$ $V_{(BR)DSS}$	-	178	-	pF
$R_g$	Gate input resistance	$f = 1 \text{ MHz}$ open drain	-	2	-	$\Omega$
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 200 \text{ V}$ , $I_D = 28 \text{ A}$ , $V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 14</a> )	-	47 10 24	-	nC nC nC

1.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
2.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 125\text{ V}$ , $I_D = 14\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13</a> )	-	40	-	ns
$t_{r(V)}$	Voltage rise time			18		ns
$t_{f(I)}$	Current fall time			64		ns
$t_{c(off)}$	Crossing time			82		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		28	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				112	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 28\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 28\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$ (see <a href="#">Figure 15</a> )	-	168		ns
$Q_{rr}$	Reverse recovery charge			1.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			14.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 28\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 15</a> )	-	196		ns
$Q_{rr}$	Reverse recovery charge			1.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			17		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

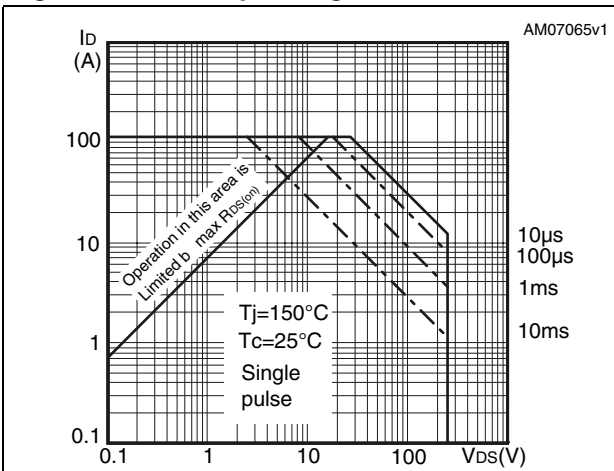


Figure 3. Thermal impedance

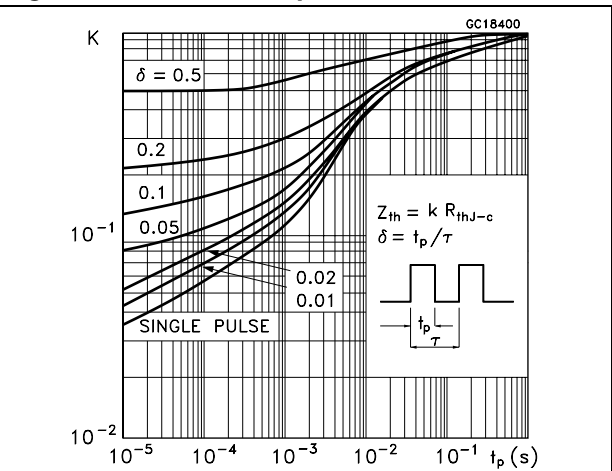


Figure 4. Output characteristics

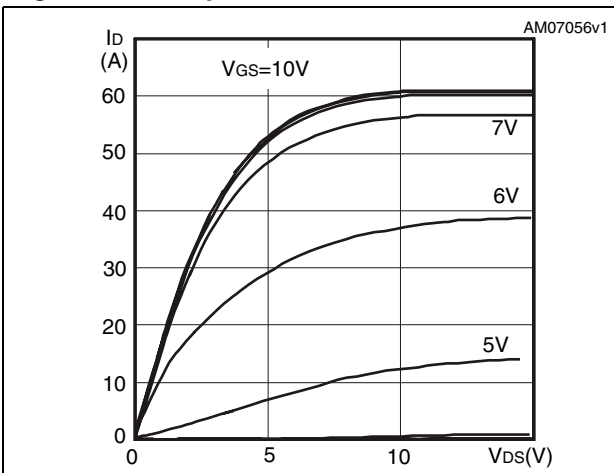


Figure 5. Transfer characteristics

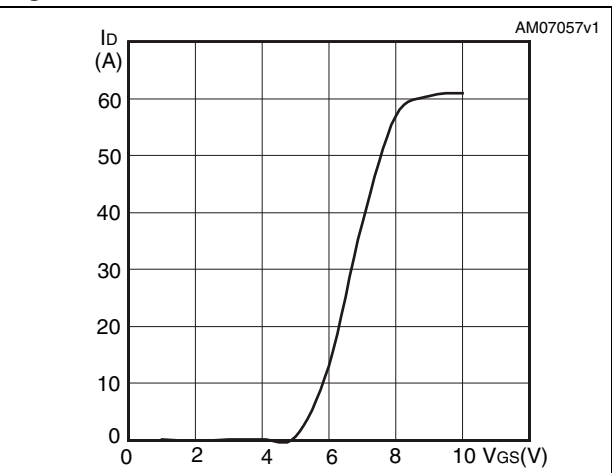


Figure 6. Gate charge vs gate-source voltage

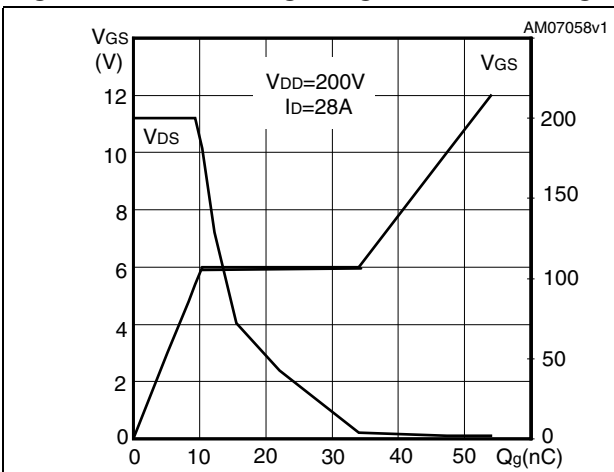


Figure 7. Static drain-source on resistance

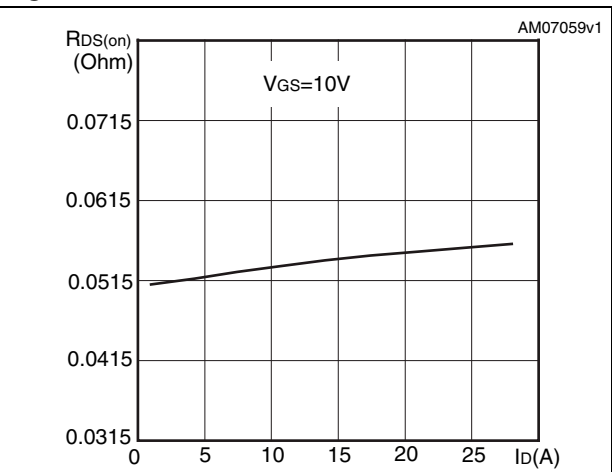


Figure 8. Capacitance variations

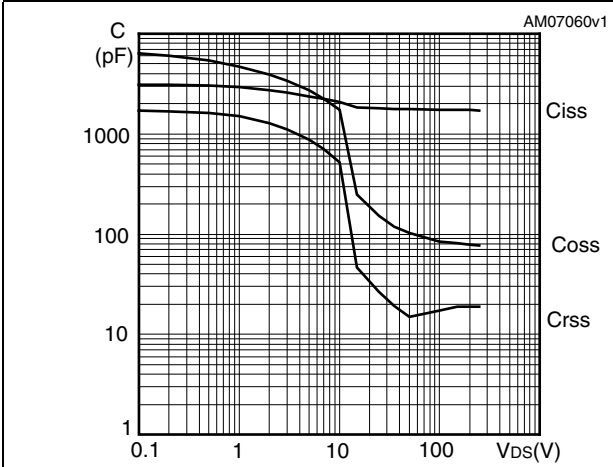


Figure 9. Output capacitance stored energy

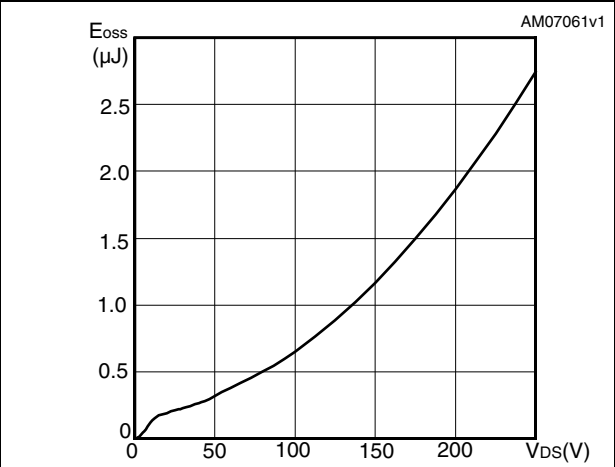


Figure 10. Normalized gate threshold voltage vs temperature

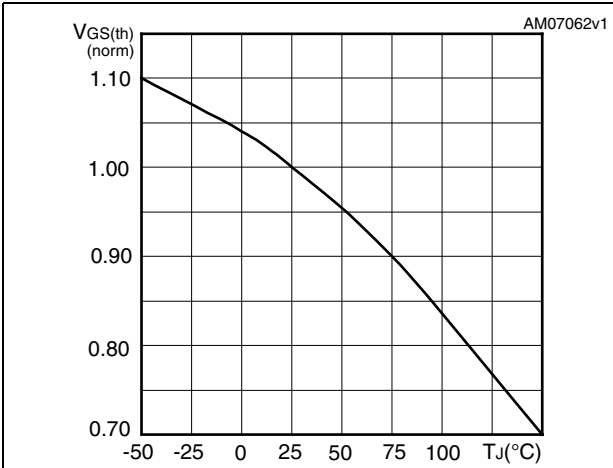


Figure 11. Normalized on resistance vs temperature

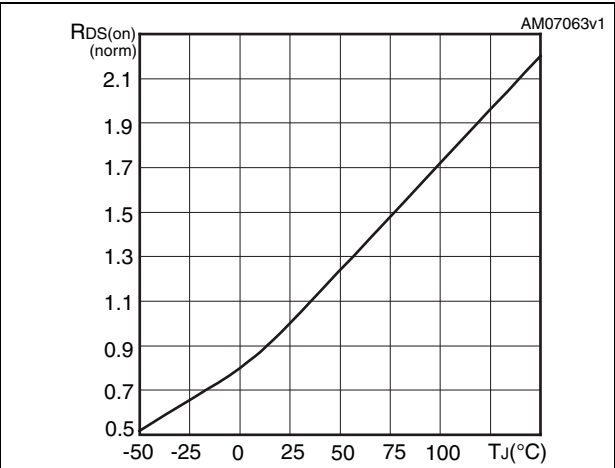
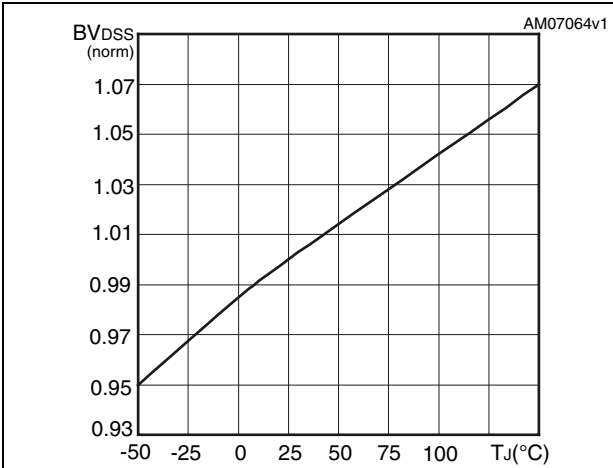
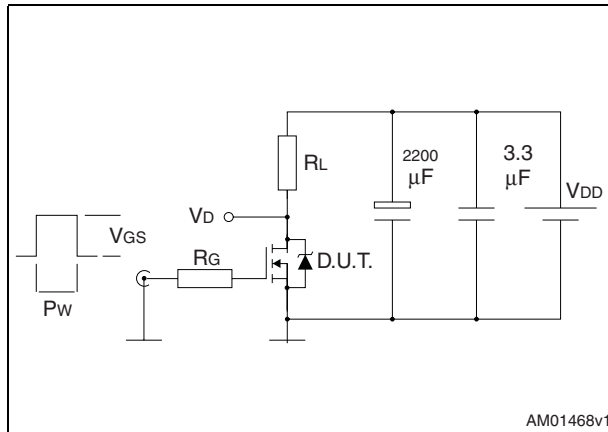


Figure 12. Normalized B<sub>VDS</sub> vs temperature

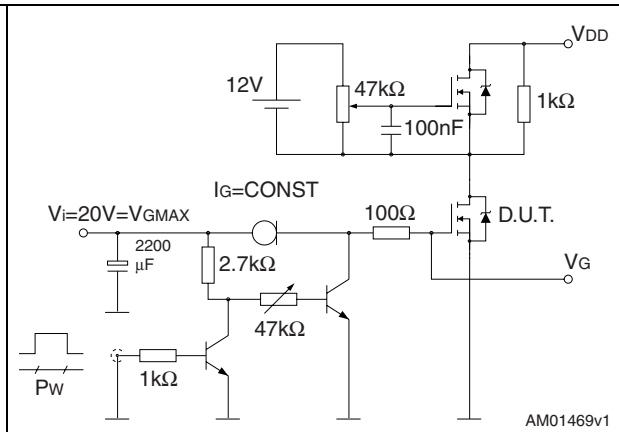


### 3 Test circuits

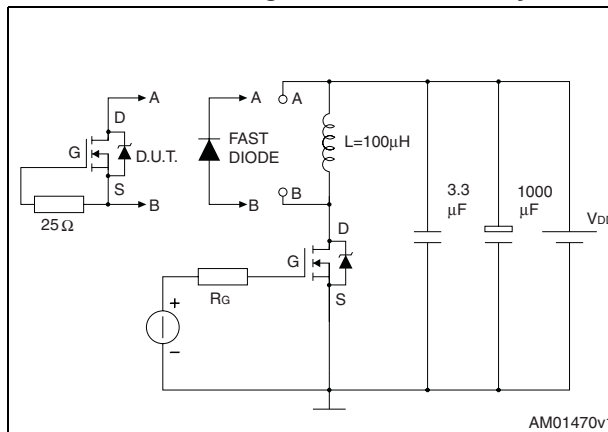
**Figure 13. Switching times test circuit for resistive load**



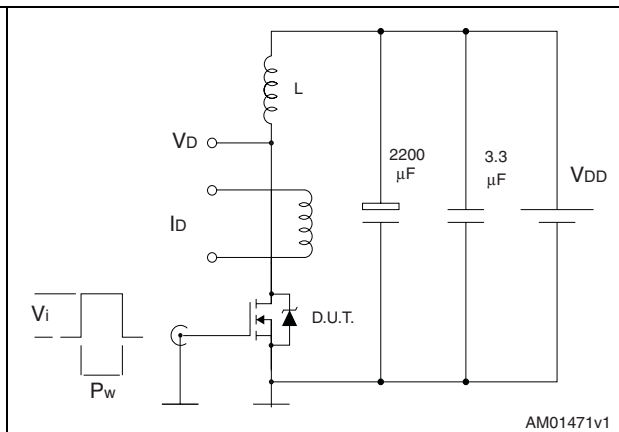
**Figure 14. Gate charge test circuit**



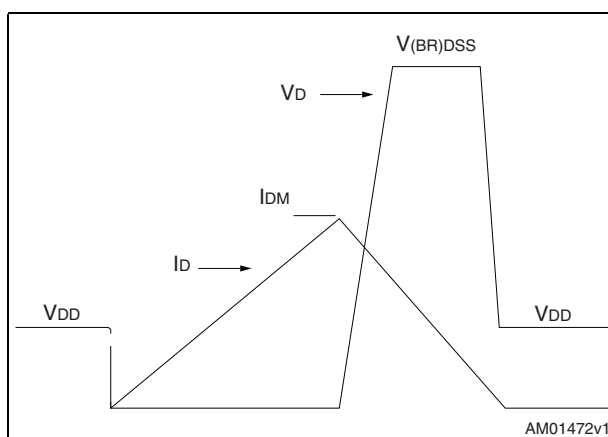
**Figure 15. Test circuit for inductive load switching and diode recovery times**



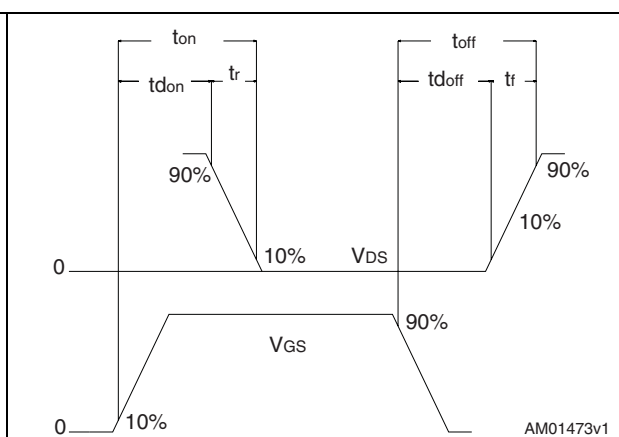
**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**



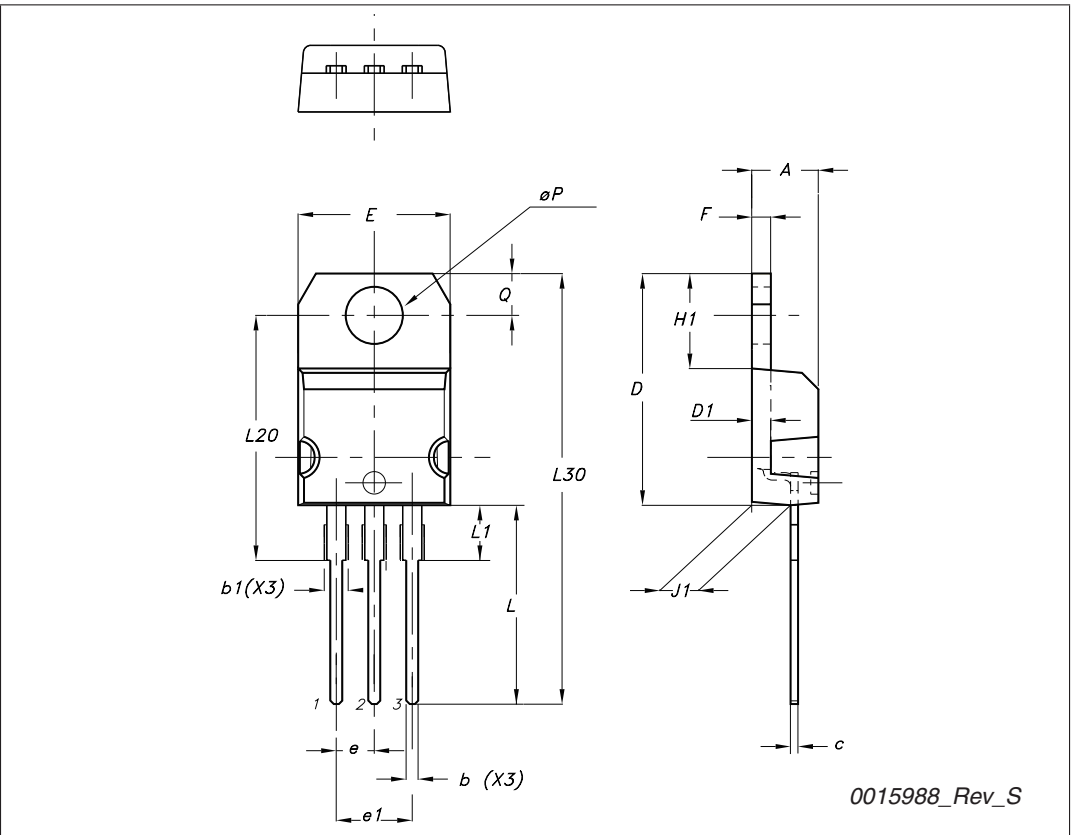


## 4      **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
29-Jul-2010	1	First release

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