

# Quad, Differential I/O, 2X1 Multiplexed High Gain Preamp

## FEATURES

- 4 DIFFERENTIAL OUTPUT CHANNELS
- 2 SETS OF 4 DIFFERENTIAL INPUTS
- 90MHz BANDWIDTH UP TO 3.5$V_{PP}$ OUTPUT
- GAIN OF 190V/V (No External Load)
- LOW 0.65nV/$\sqrt{Hz}$ INPUT NOISE VOLTAGE
- 50mA QUIESCENT CURRENT (5V Supply)
- LOW CROSSTALK, TQFP-48 PACKAGING
- TTL/CMOS CHANNEL SELECT LINE

## APPLICATIONS

- TAPE PREAMP
- TEST EQUIPMENT
- MULTI-CHANNEL TWISTED PAIR RECEIVER
- SAW FILTER POSTAMPLIFIER
- HIGH GAIN QUAD ADC DRIVERS
- ULTRA SOUND PRE-AMPLIFIERS

### RELATED PARTS

| PART NUMBER | DESCRIPTION |
|---|---|
| OPA2846 | Dual, Low-Noise Op Amp |
| ADS5121 | Octal, 10-Bit 40MSPS ADC |

## DESCRIPTION

The MPA4609 is one of the lowest noise, fixed gain, 5V single-supply, differential amplifiers available for amplification of low-level signals in a variety of system applications. The chip has two sets of four differential input, low-noise amplifiers that are routed to four output stages. Two standard logic input select lines control which set of four input preamps are active. For applications such as tape recorders, four heads in forward and four heads in reverse can be selected at one time.

The quad consists of eight differential low noise (0.65nV$\sqrt{Hz}$) voltage preamps. Two select lines control two pairs of inputs. Each of the output stages provides a nominal 470Ω-output impedance on each half of the differential output stages. The overall gain of 190V/V may be attenuated by adding an external load resistor between each set of differential outputs. For example, adding an external 940Ω resistor across the output pins will reduce the nominal differential gain by half to 95V/V.

Internal biasing controls the differential inputs to 2.0V and outputs to a 2.1V common-mode operating level. The maximum no-load differential output swing is 3.5$V_{PP}$ centered on the 2.1V bias level. A low input offset voltage and bias current offset holds the maximum output differential offset to < ±350mV for no-load conditions.

The low (3.5pF) input capacitance makes this part useable for applications requiring wide bandwidth and multiple pick-ups often seen in testers, medical equipment, twisted pair receivers, and optical systems. The single +5V supply and its low quiescent current of 50mA make it exceptionally attractive in multi-channel, low power, high bandwidth designs.

## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Power Supply | +7V |
| Internal Power Dissipation | 750mW |
| Differential Input Voltage | ±1.2V |
| Input Voltage Range | GND to $+V_S$ |
| Storage Temperature Range: PFB | –65°C to +125°C |
| Junction Temperature ($T_J$) | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| ESD Rating (Human Body Model) | 3000V |
| (Charge Device Model) | 1500V |
| (Machine Model) | 200V |

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

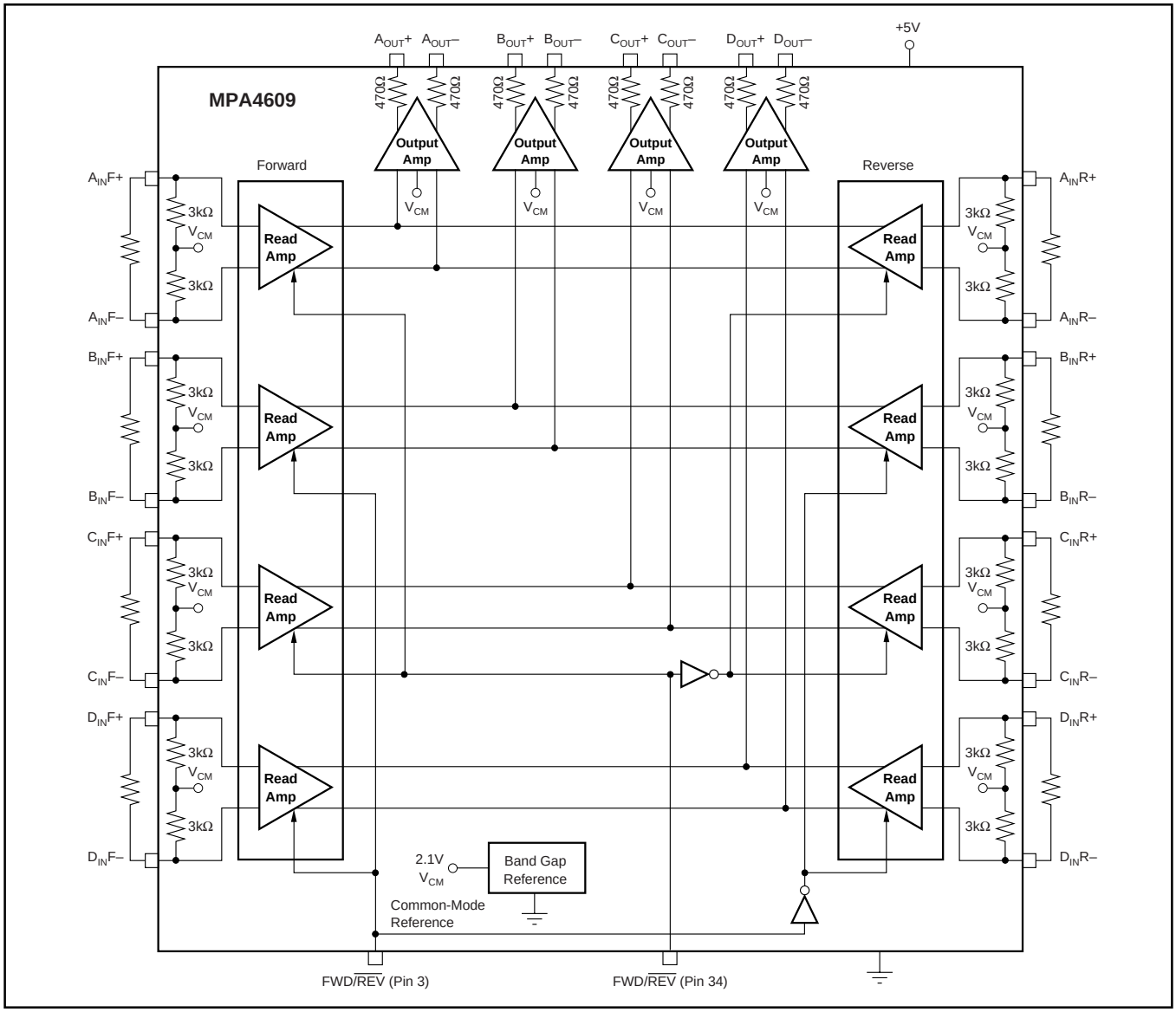
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | SPECIFIED TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---|---|---|---|---|---|---|
| MPA4609 | TQFP-48 | PFB | –40°C to +85°C | MPA4609 | MPA4609IPFBT | Tape and Reel, 250 |
| " | " | " | " | " | MPA4609IPFBR | Tape and Reel, 2000 |

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## BLOCK DIAGRAM



# ELECTRICAL CHARACTERISTICS: $V_S$ = +5.0V

**Boldface** limits are tested at **+25°C**.

At $T_A$ = +25°C, $R_S$ = 65Ω (differential), $VI_{CM}$ = 2.0, $VO_{CM}$ = 2.1V, $R_L$ > 2kΩ,unless otherwise noted.

| PARAMETER | CONDITION | MPA4609IPFB | | | | | |
|---|---|---|---|---|---|---|---|
| | | TYP | MIN/MAX OVER TEMPERATURE(1) | | | | TEST LEVEL(2) |
| | | +25°C | +25°C | 0 to +70°C | UNITS | MIN/MAX | |
| **AC PERFORMANCE (Figure 1)** | | | | | | | |
| Large Signal Bandwidth, | $V_O$ = 500mV$_{PP}$, no load | 90 | 80 | 75 | MHz | min | B |
| Minimum Midband Gain [$R_L$ = 940Ω] | $V_O$ = 200mV$_{PP}$ (DC to 20MHz) | 95 | **78** | 65 | V/V | min | A |
| Maximum Midband Gain [$R_L$ = 940Ω] | $V_O$ = 200mV$_{PP}$ (DC to 20MHz) | 95 | **115** | 120 | V/V | max | A |
| Minimum Open Load Gain | $V_O$ = 200mV$_{PP}$ (DC to 20MHz) | 190 | **160** | 140 | V/V | min | A |
| Maximum Open Load Gain | $V_O$ = 200mV$_{PP}$ (DC to 20MHz) | 190 | **220** | 240 | V/V | max | A |
| Differential Slew Rate | No Load, $V_O$ = 3V$_{PP}$ | 150 | | | V/µsec | typ | C |
| Differential Rise/Fall Time | ±250mV Step | 3.5 | 4.4 | 4.7 | nsec | min | B |
| Total Harmonic Distortion | 10MHz, 2V$_{PP}$ Output | –64 | | | dBc | typ | C |
| Input Noise Voltage (differential) | F > 100kHz | 0.65 | 0.80 | 0.85 | nV/√Hz | max | B |
| Input Noise Current (each input) | F > 100kHz | 3.8 | 5.1 | 5.7 | pA/√Hz | max | B |
| Channel-To-Channel X-talk (Input → Output) | F = 5MHz, CH A measured, CH B, C, D driven $R_L$ = open | –55 | | | dBc | typ | C |
| **DC PERFORMANCE(3)** | | | | | | | |
| Input Offset Voltage | $VI_{CM}$ = 2.0V nominal (internally set) | ±0.2 | **±0.9** | ±0.95 | mV | max | A |
| Input Offset Voltage Drift | | | | ±1 | µV/°C | max | B |
| Input Bias Current | | –51 | **–70** | –75 | µA | max | A |
| Input Offset Current | | ±0.25 | | | µA | typ | C |
| Forward/Reverse Gain Match | Channel Pairs | ±2.3 | **±10** | ±11 | % | max | A |
| **INPUT** | | | | | | | |
| Minimum Common-Mode Input Voltage(4) | Externally Applied (CMIR) | 1.3 | **1.4** | 1.5 | V | min | A |
| Maximum Common-Mode Input Voltage(4) | Externally Applied (CMIR) | 2.3 | **2.3** | 2.2 | V | max | A |
| Input Bias Resistor | Each Input to $V_{CM}$ | 3000 | | | Ω | typ | C |
| Input Bias Resistor Tolerance | | | **±15** | ±16 | % | max | A |
| Input Differential Capacitance | | 3.5 | | | pF | typ | C |
| Minimum Common-Mode Bias Voltage | Internal Reference | 2 | **1.85** | 1.75 | V | min | A |
| Maximum Common-Mode Bias Voltage | Internal Reference | 2 | **2.15** | 2.25 | V | max | A |
| Common-Mode Rejection Ratio (DC) | $R_L$ = open, Common-Mode Input to Differential Output | 36 | **25** | 24 | dB | min | A |
| **OUTPUT** | | | | | | | |
| Output Offset Voltage | $R_L$ open, Inputs Open | ±40 | **±350** | ±450 | mV | max | A |
| Minimum Common-Mode Output Voltage | | 2.1 | **1.95** | 1.85 | V | min | A |
| Maximum Common-Mode Output Voltage | | 2.1 | **2.25** | 2.35 | V | max | A |
| Maximum Differential Output Voltage Swing | $VO_{CM}$ = 2.1V, $R_L$ = open | 3.5 | **2.8** | 2.6 | Vpp | min | A |
| Single Ended Output Impedance | | 470 | | | Ω | typ | C |
| Single Ended Output Impedance Tolerance | | | **±15** | ±16 | % | max | A |
| **CHANNEL SELECT (F/$\overline{R}$)** | TTL/CMOS Compatible | | | | | | |
| Highest Logic Low Level | Logic Low = REV Channels | 1.0 | **0.9** | 0.9 | V | max | A |
| Lowest Logic High Level | Logic High = FOR Channels | 1.5 | **1.6** | 1.6 | V | min | A |
| Logic Low Input Bias Current (each pin) | F/$\overline{R}$ pins = 0V | 70 | | | µA | typ | C |
| Logic High Input Bias Current (each pin) | F/$\overline{R}$ pins = 5V | 1 | | | µA | typ | C |
| Channel Switching Time | | 50 | | | nsec | typ | C |
| Output Differential Glitch in Switching | All Inputs, 65Ω Differential Source | ±15 | | | mV | typ | C |
| Unselected Channel Feedthrough | All Channel Pairs, Unselected Input (±100mV) to Output | –50 | **–36** | –36 | dB | max | A |
| **POWER SUPPLY** | | | | | | | |
| Specified Operating Voltage | | 5 | | | V | typ | C |
| Maximum Operating Voltage | | | **6.0** | 6.0 | V | max | A |
| Minimum Operating Voltage | | | **4.5** | 4.5 | V | min | A |
| Maximum Quiescent Supply Current | $V_S$ = +5V | 49 | **52** | 59 | mA | max | A |
| Minimum Quiescent Supply Current | $V_S$ = +5V | 49 | **46** | 42 | mA | min | A |
| Power Supply Rejection Ratio (DC) | $R_L$ = open, Power Supply (±250mV) to Differential Output | 50 | **34** | 33 | dB | min | A |
| **TEMPERATURE RANGE** | | | | | | | |
| Specification: I | | –40 to +85°C | | | °C | typ | C |
| Thermal Resistance, $\theta_{JA}$ | Junction-to-Ambient | | | | | | |
| PFB TQFP-48 | | 60 | | | °C/W | typ | C |

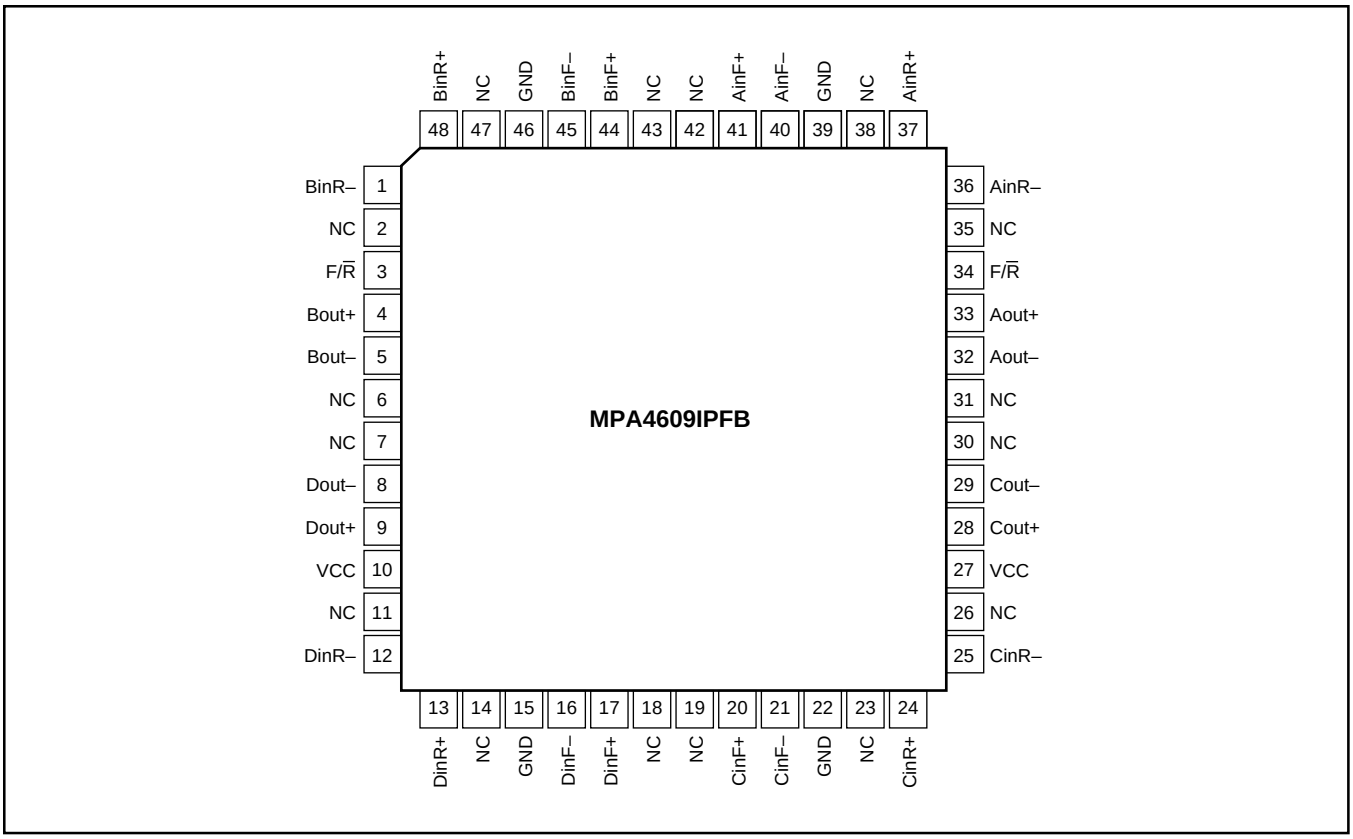
NOTES: (1) Junction temperature = ambient temperature for low temperature limit and +25°C specifications. Junction temperature = ambient temperature +15°C at high temperature limit specifications.

(2) Test Levels:
(A) 100% DC tested at +25°C. Over-temperature limits by characterization and simulation.
(B) Limits set by characterization and simulation.
(C) Typical value only for information.

(3) Current is considered positive out-of-node. $V_{CM}$ is the input and output common-mode voltage.

(4) Tested < 3dB below minimum specified CMRR at CMIR limits.

## PIN CONFIGURATION




## PIN DESCRIPTIONS

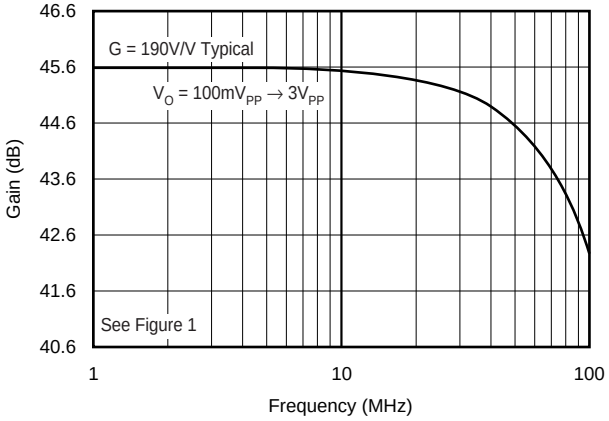
| PIN | NAME | TYPE | DESCRIPTION | PIN | NAME | TYPE | DESCRIPTION |
|---|---|---|---|---|---|---|---|
| 1 | BinR– | A(1) | B –Channel Reverse Inverting Input | 25 | CinR– | A | C –Channel Reverse Inverting Input |
| 2 | NC | | Internally Not Connected - may be grounded | 26 | NC | | Internally Not Connected - may be grounded |
| 3 | F/$\overline{R}$ | D | Forward or Reverse Channel Select Line Ch. B and Ch. D | 27 | VCC | P | Supply Voltage (+5V nominal) |
| 4 | Bout+ | A | B –Channel Non-Inverting Output | 28 | Cout+ | A | C –Channel Non-Inverting Output |
| 5 | Bout– | A | B –Channel Inverting Output | 29 | Cout– | A | C –Channel Inverting Output |
| 6 | NC | | Internally Not Connected - may be grounded | 30 | NC | | Internally Not Connected - may be grounded |
| 7 | NC | | Internally Not Connected - may be grounded | 31 | NC | | Internally Not Connected - may be grounded |
| 8 | Dout– | A | D –Channel Inverting Output | 32 | Aout– | A | A –Channel Inverting Output |
| 9 | Dout+ | A | D –Channel Non-Inverting Output | 33 | Aout+ | A | A –Channel Non-Inverting Output |
| 10 | VCC | P | Supply Voltage (+5V nominal) | 34 | F/$\overline{R}$ | D | Forward or Reverse Channel Select Line |
| 11 | NC | | Internally Not Connected - may be grounded | 35 | NC | | Internally Not Connected - may be grounded |
| 12 | DinR– | A | D –Channel Reverse Inverting Input | 36 | AinR– | A | A –Channel Reverse Inverting Input |
| 13 | DinR+ | A | D –Channel Reverse Non-Inverting Input | 37 | AinR+ | A | A –Channel Reverse Non-Inverting Input |
| 14 | NC | | Internally Not Connected - may be grounded | 38 | NC | | Internally Not Connected - may be grounded |
| 15 | GND | G | Ground | 39 | GND | G | Ground |
| 16 | DinF– | A | D –Channel Forward Inverting Input | 40 | AinF– | A | A –Channel Forward Inverting Input |
| 17 | DinF+ | A | D –Channel Forward Non-Inverting Input | 41 | AinF+ | A | A –Channel Forward Non-Inverting Input |
| 18 | NC | | Internally Not Connected - may be grounded | 42 | NC | | Internally Not Connected - may be grounded |
| 19 | NC | | Internally Not Connected - may be grounded | 43 | NC | | Internally Not Connected - may be grounded |
| 20 | CinF+ | A | C –Channel Forward Non-Inverting Input | 44 | BinF+ | A | B –Channel Forward Non-Inverting Input |
| 21 | CinF– | A | C –Channel Forward Inverting Input | 45 | BinF– | A | B –Channel Forward Inverting Input |
| 22 | GND | G | Ground | 46 | GND | G | Ground |
| 23 | NC | | Internally Not Connected - may be grounded | 47 | NC | | Internally Not Connected - may be grounded |
| 24 | CinR+ | A | C –Channel Reverse Non-Inverting Input | 48 | BinR+ | A | B –Channel Reverse Non-Inverting Input |

NOTE: (1) Pin Types: A (analog), D (digital), G (ground), P (power supply).

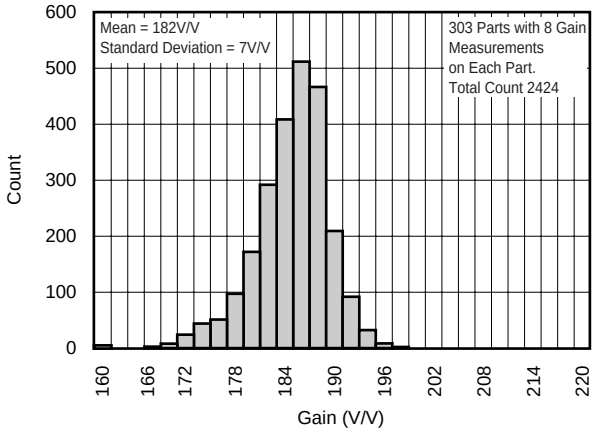
# TYPICAL CHARACTERISTICS: $V_S$ = +5V

$T_A$ = +25°C, $R_S$ = 65Ω (differential), $VI_{CM}$ = 2.0V, $VO_{CM}$ = 2.1V, $R_L$ > 2kΩ, unless otherwise noted.

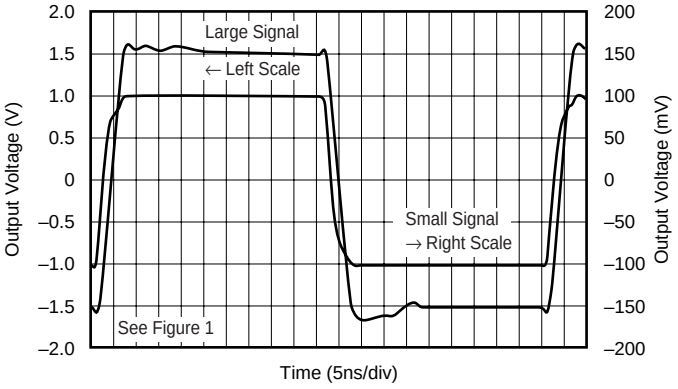
FREQUENCY RESPONSE



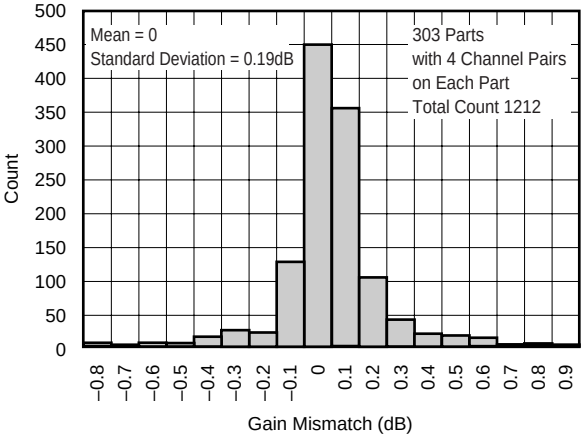

TYPICAL GAIN DISTRIBUTION



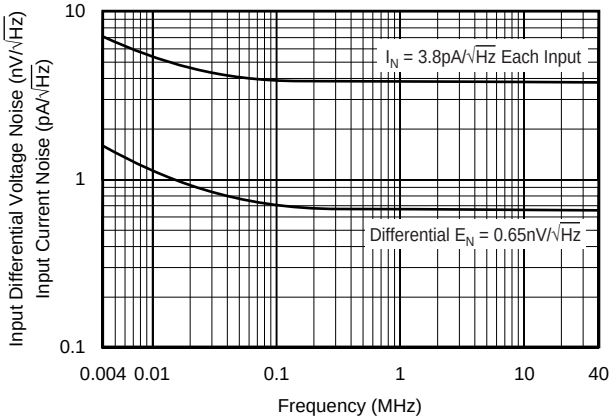

DIFFERENTIAL PULSE RESPONSE



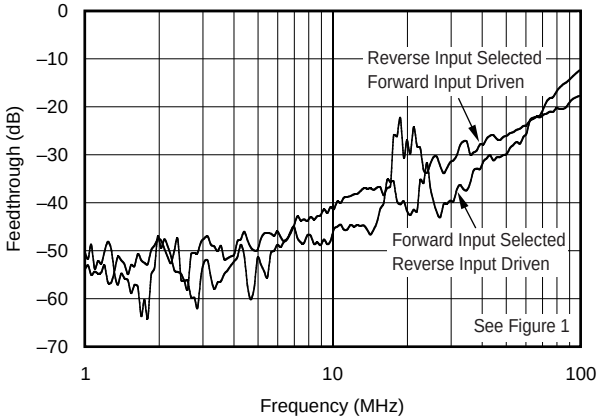

TYPICAL FORWARD/REVERSE CHANNEL GAIN MISMATCH




INPUT VOLTAGE AND CURRENT NOISE DENSITY



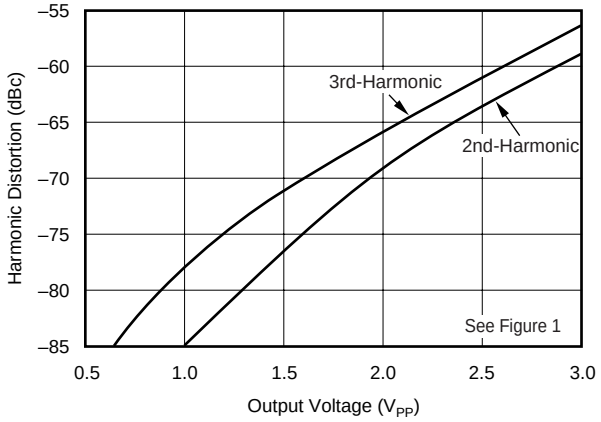

FORWARD/REVERSE CHANNEL FEEDTHROUGH



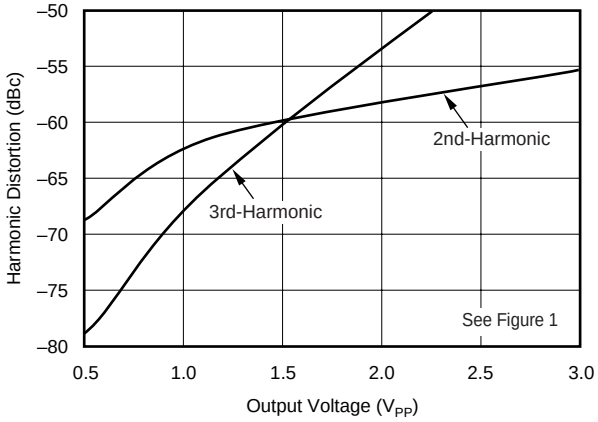
# TYPICAL CHARACTERISTICS: $V_S$ = +5V (Cont.)

$T_A$ = +25°C, $R_S$ = 65Ω (differential), $VI_{CM}$ = 2.0V, $VO_{CM}$ = 2.1V, $R_L$ > 2kΩ, unless otherwise noted.

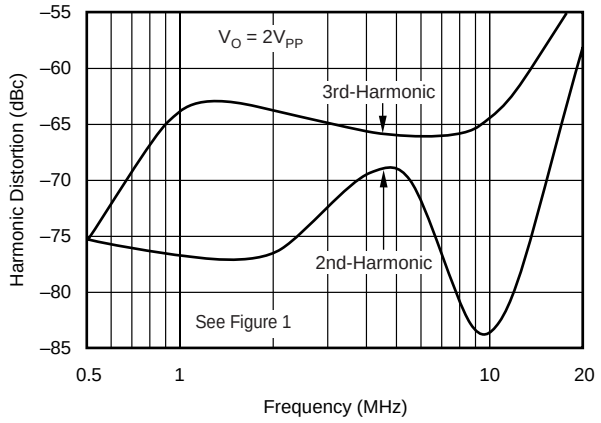
5MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE



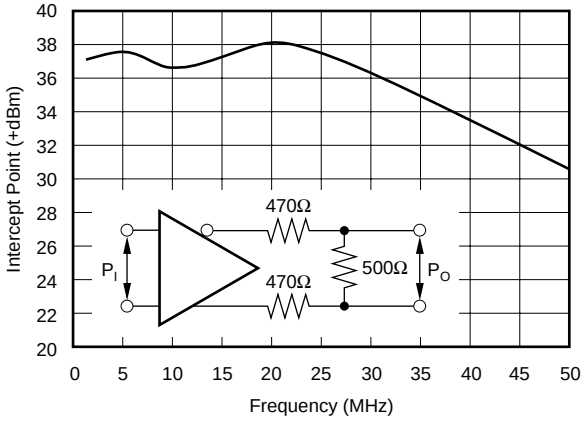

20MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE



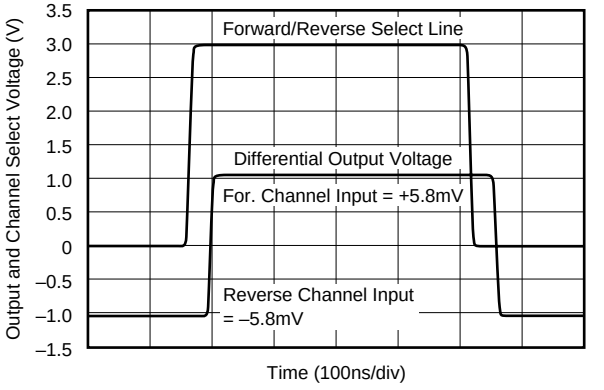

HARMONIC DISTORTION vs FREQUENCY



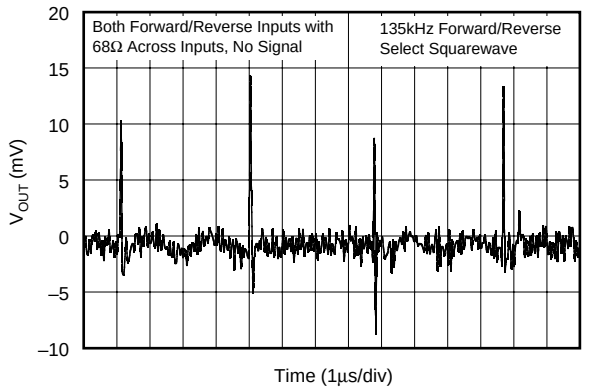

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT 500Ω LOAD




FORWARD/REVERSE SWITCHING TIME



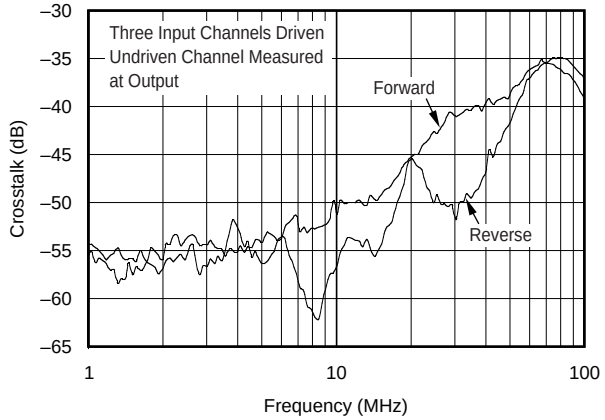

FORWARD/REVERSE SWITCHING GLITCH



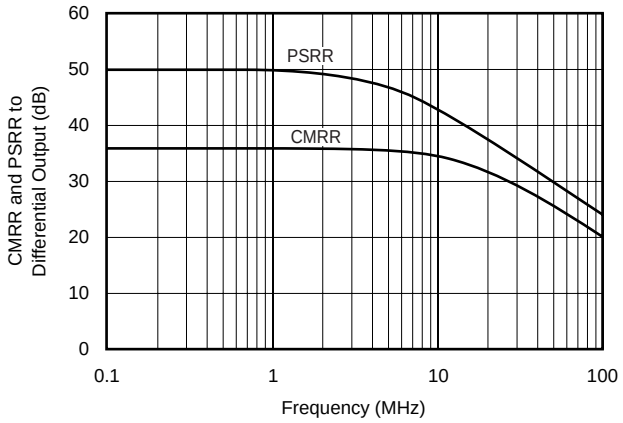
# TYPICAL CHARACTERISTICS: $V_S$ = +5V (Cont.)

$T_A$ = +25°C, $R_S$ = 65Ω (differential), $VI_{CM}$ = 2.0V, $VO_{CM}$ = 2.1V, $R_L$ > 2kΩ, unless otherwise noted.

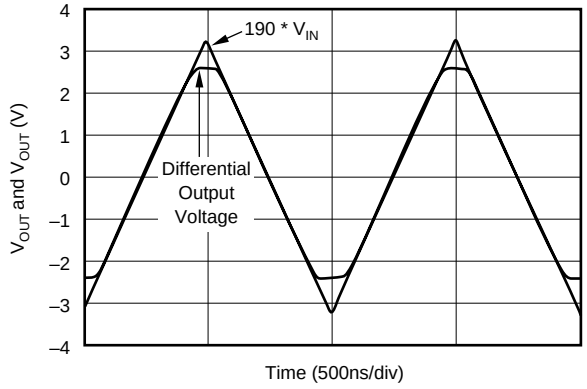
ALL HOSTILE CROSSTALK



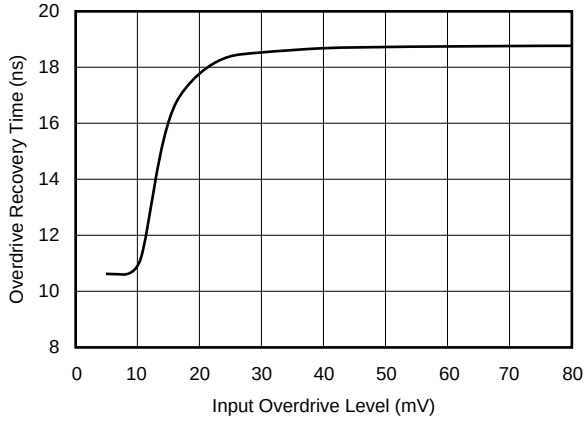

COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO vs FREQUENCY



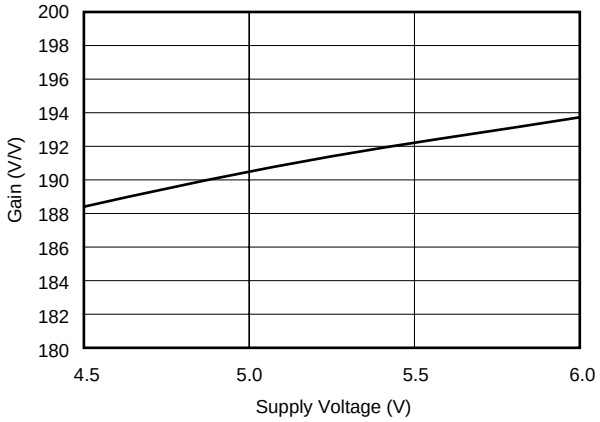

OVERDRIVE RECOVERY



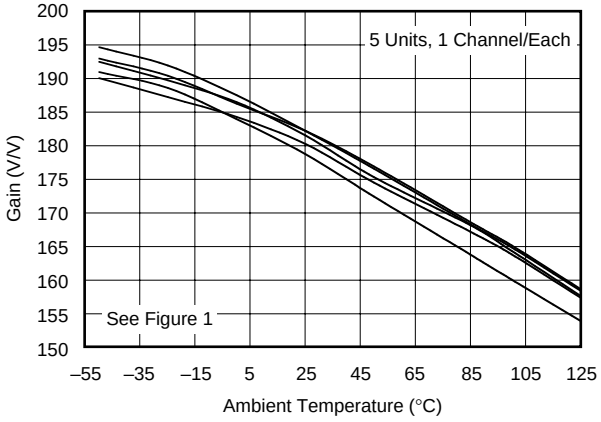

OVERDRIVE RECOVERY TIME vs OVERDRIVE LEVEL




GAIN vs SUPPLY VOLTAGE



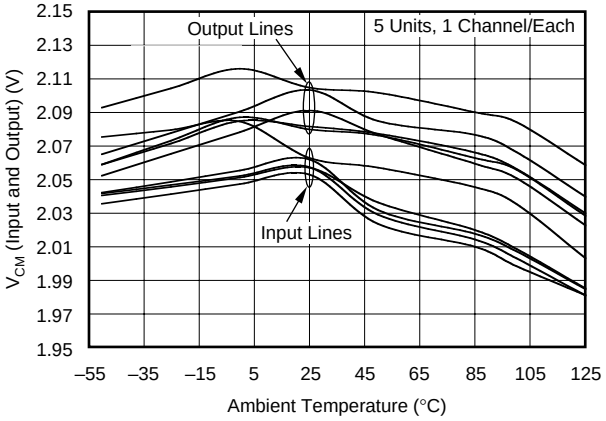

TYPICAL OPEN LOAD GAIN vs TEMPERATURE



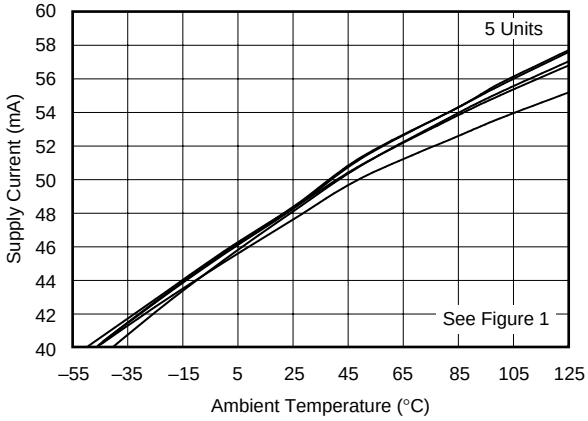
# TYPICAL CHARACTERISTICS: $V_S$ = +5V (Cont.)

$T_A$ = +25°C, $R_S$ = 65Ω (differential), $VI_{CM}$ = 2.0V, $VO_{CM}$ = 2.1V, $R_L$ > 2kΩ, unless otherwise noted.

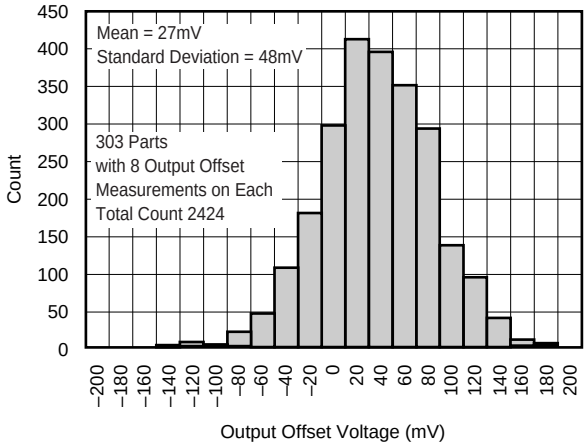
INPUT AND OUTPUT COMMON-MODE VOLTAGE vs TEMPERATURE



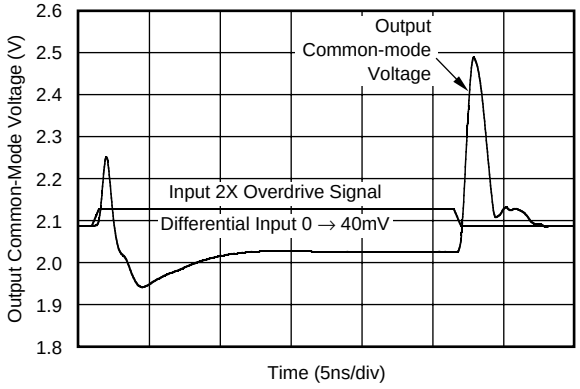

TYPICAL SUPPLY CURRENT vs TEMPERATURE



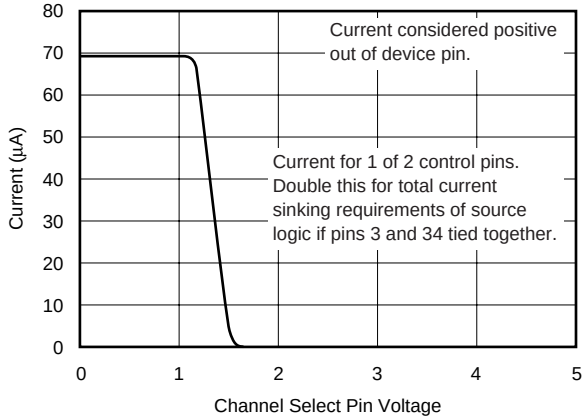

TYPICAL OUTPUT OFFSET VOLTAGE DISTRIBUTION



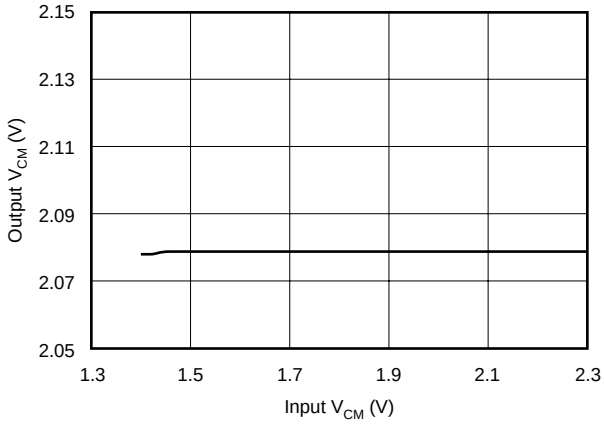

OUTPUT COMMON-MODE LOOP RECOVERY




FORWARD/REVERSE CHANNEL SELECT CURRENT




COMMON-MODE $V_O$ vs INPUT $V_{CM}$



# APPLICATIONS INFORMATION

## DIFFERENTIAL FIXED GAIN AMPLIFIER OPERATION

The MPA4609 consists of four pairs of two-channel, low-noise, differential input stages that can be selected using a pair of digital control pins. These two pins, F/$\overline{R}$, are intended to switch 4 differential preamps from the forward tape head to the reverse tape head in a tape preamp application. This multiplexing capability can be used in other applications as well. Where a high gain, quad differential output is required, one set of inputs can be used for signal transmission while the other set can be applied as a reference signal input or as a simple *look-away* during high overdrive conditions on the signal input. Channel switching is a fast 50ns.

Figure 1 shows the internal configuration for 1 of 4 channels along with a simplified external configuration used for test. Since the MPA4609 is such a high gain device, the input signal is typically attenuated for test purposes at the input through a resistive divider network that matches the source and provides a 65Ω differential source impedance looking out of the inputs. Those are not shown in Figure 1, but some input signal interface components were typically present when the Typical Characteristics curves were taken.

All input pins are DC-biased from an internal 2.1V bandgap reference through 3kΩ resistors. In application, the total AC source impedance is dominated by the low source impedance of the head, giving a minimal gain for the input current noise terms. For a low output DC offset, very low input voltage offset and bias current offset terms are required. The ±0.8mV maximum input offset voltage along with the ±0.25µA typical input bias current offset give a low total output DC differential offset voltage. AC loading for the source is minimal given the low 3.5pF differential input capacitance looking into each of the 8 inputs.

Channel select is provided in the 1st stage of the amplifier. The unselected input stage is biased down. The output stage includes a common-mode control loop referenced to the 2.1V internal bandgap reference. Output swings specified in the Specifications and Characteristics are at the internal nodes ($V'_O$) prior to the series 470Ω resistors provided in each output leg. These resistors provide an easy way to adjust the overall differential gain by including an external $R_L$. However, it is the internal output swing ($V'_O$) that matters in setting the limits to performance.

The 2.1V I/O DC bias voltage is intended to retain maximum differential output voltage swing when the nominal +5V single supply drops as low as +4.5V. Each output can swing ±0.75V around this bias giving a maximum $3V_{PP}$ differential signal at $V'_O$. This $3V_{PP}$ available swing is adequate to support most differential ADC input ranges. The series 470Ω output resistors also provide an easy means to bandlimit at the input of the ADC with a single capacitor. Input signals that require DC coupling can override the input common-mode reference over the specified 1.4 to 2.3V input common-mode range limits at 25°C.

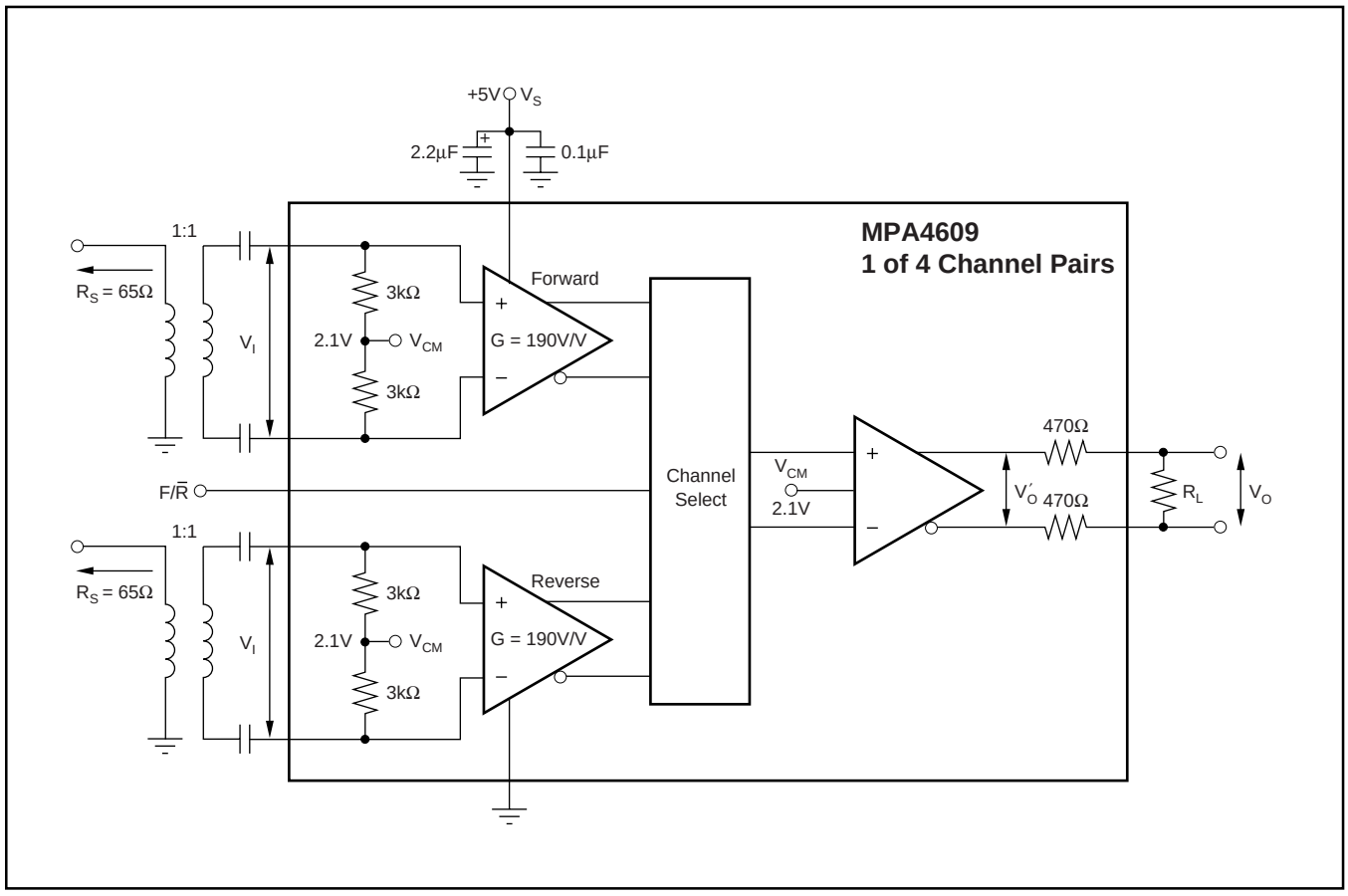



FIGURE 1. Typical Test Circuit for 1 of 4 Channel Pairs.

## CHANNEL SELECT

Two pins are provided to switch between input channels. Pin 3 controls channels B and D while pin 34 controls channels A and C. These are normally tied together for tape preamp applications but can be operated separately if the application requires it. The channel select is a voltage control that switches at approximately 1.25V. Voltages less than 0.9V are assured to select the REV channel while voltages > 1.6V will select the FOR channel. This allows a direct interface to 3.3V (or lower) logic outputs. Virtually no pin current is required in the logic high state while a low 70µA/pin out of the pin is required in the logic low state. Left unconnected, the channel select defaults to the forward selection.

The channels switch in approximately 50ns typically. With no input present, there is minimal output glitching when switched.

## CONNECTING TO LOW IMPEDANCE MR HEADS FOR TAPE RECORDERS

The MPA4609 is designed to detect and amplify the voltage signal from a Magneto Resistive (MR) head with minimal SNR degradation from the SNR intrinsic to the head. A typical MR head interface is shown in Figure 2. Not considering any postfiltering, the amplifier's 0.65nV/$\sqrt{Hz}$ input noise voltage and 90MHz bandwidth combine to produce a very low 7.7$\mu V_{RMS}$ input referred noise floor. Even with a conservative 20dB S/N margin, input signals as low as 77$\mu V_{PP}$ may be detected. With a maximum differential output of 3$V_{PP}$ and a 190V/V gain, a maximum input of 15.7m$V_{PP}$ may be applied. This wide range of inputs translates into 46dB input dynamic range. Since the MR head is biased through external voltages, it is often required to connect the signal through series blocking capacitors as shown in Figure 2. The high-pass pole created by these capacitors ($C_B$) and the source resistance are selected to pass the lowest frequencies required by the system.

## TWISTED PAIR RECEIVER

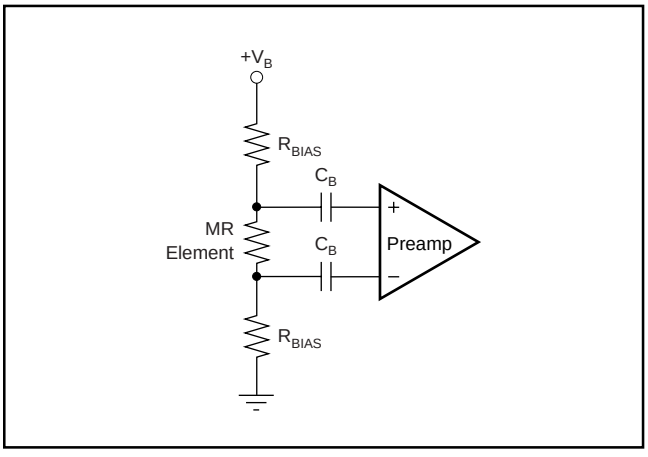



FIGURE 2. Typical MR Head Interface.

The extremely high gain and low input noise of the MPA4609 can provide a very capable, multi-channel, twisted pair receiver. This would be particularly useful for narrowband higher frequency carriers that suffer from significant cable loss. For broadband carriers, a high-pass filter should be included to reduce the low frequency receiver power. Since the MPA4609 provides a gain constant over frequency, the lower frequency region, that does not have as much loss in the twisted pair as the higher frequencies, can easily overdrive the output without the high-pass filter present.

## HIGH PERFORMANCE QUAD ADC DRIVER

The high gain, wide bandwidth, capability of the MPA4609 can provide a very cost effective input stage to quad high performance ADCs. Figure 3 shows an example implementation where a 2nd-order passive low-pass filter has been included in the interface to bandlimit the noise. The filter in this example is set to approximately 18MHz cutoff with a Butterworth (maximally flat) response including the internal 470Ω output resistors in the design. The distortion performance of the MPA4609 will support up to 10-bit converters through approximately 10MHz maximum input analog frequency. For a 2$V_{PP}$ output, the THD shown in the Typical Characteristic Curves is ≤ 63dBc through 10MHz. The 18MHz Butterworth filter limits the noise power bandwidth for the amplifier output noise to approximately 20MHz. With a 0.65nV/$\sqrt{Hz}$ input voltage noise and 190V/V nominal gain, this 124nV/$\sqrt{Hz}$ output noise integrates to approximately 555$\mu V_{RMS}$ at the differential input of the converter. This RMS noise is approximately 1/2 of an LSB for a 2$V_{PP}$ full-scale input range.

The example here does not take advantage of the two sets of multiplexed inputs on each of the four channels. The

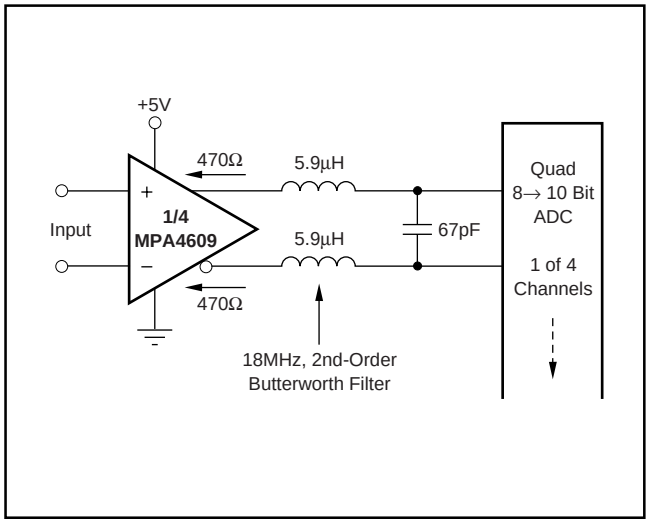



FIGURE 3. Quad, ADC Input Driver.

second input could be used for simple input multiplexing; for instance, where the source signal is fed through two different filters, then selected at the MPA4609, or as a test signal input. Another good application of this second input is to provide an attenuated version of the input present on one stage where additional input dynamic range is required. The example of Figure 4 shows the configuration for the input stages were an added 20dB attenuation is taken in the lower channel. The total differential input impedance of this circuit is 200Ω where each input presents a 400Ω differential load. The shunt resistor has been adjusted up slightly to account for the internal 6kΩ differential load across the inputs as part of the common-mode bias setup.

If the converter full-scale input range is a differential $2V_{PP}$, the maximum input signal that can be passed through the upper stage of Figure 4 is $2V_{PP}/(153V/V) = 13mV_{PP}$. As the converter detects an over-range condition, it can switch to the lower stage of Figure 4 where a maximum input of $2V_{PP}/(15.3V/V) = 130mV_{PP}$ would be supported. While this lower channel certainly suffers from a higher equivalent input referred noise, it would only be used when the input signal is relatively high, keeping the output SNR almost constant.

## PHOTODIODE DIFFERENTIAL AMPLIFIER

The high gain and low noise with a differential input can be applied to photodiode detector applications where a photovoltaic mode is required and a reference dark current detector can be used. Figure 5 shows an example for this, where two matched diodes operate with a 0V bias and generate a small signal through a grounded sense resistor. One diode is not exposed to the light signal, having only dark current, while the other diode has both dark current plus signal current. This mode is sometimes used for very large area detectors where the diode dark current and parasitic capacitance are relatively large.

## SONAR AND PIEZOELECTRIC SENSORS

High-frequency sonar and piezoelectric sensors will benefit

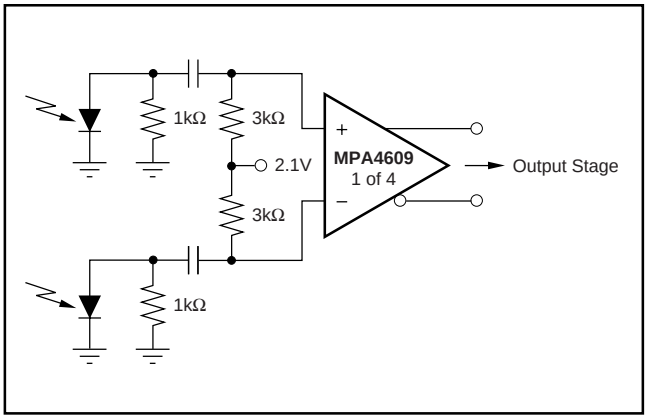



FIGURE 5. Photo-Diode Differential Amplifier.

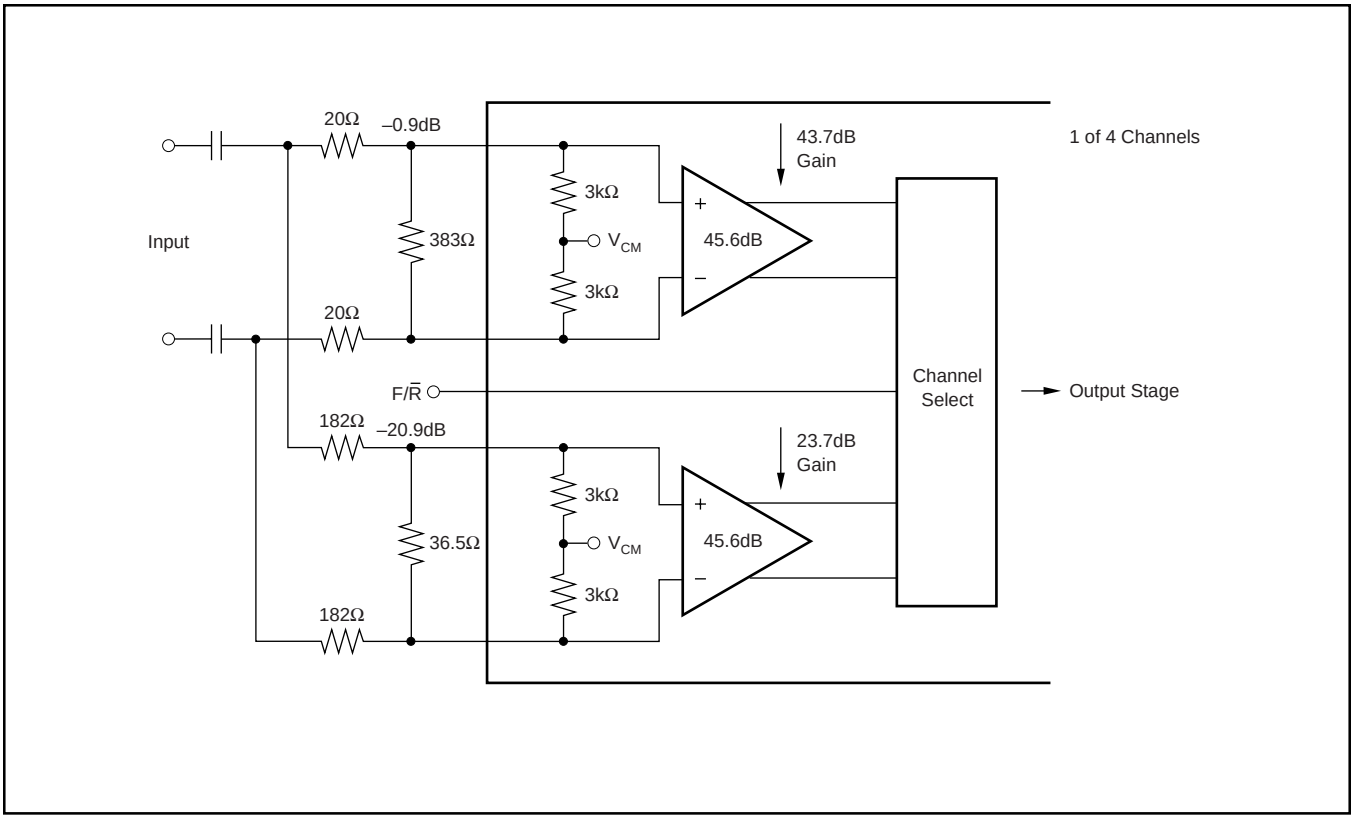



FIGURE 4. Switched Attenuator to Increase ADC Dynamic Range.

from the low voltage noise of the MPA4609, providing excellent channel density where an array of sensors is used. For sonar, it is also useful to use the second input available on each channel of the MPA4609 as a *look-away* during the high signals that may be present just after the transmitted pulse. While the MPA4609 recovers very well to overdrives (< 20ns), using this *look-away* feature to an open input channel will minimize large output voltage steps. In AC-coupled channels, large output overdrives require large charge and discharge currents through the blocking capacitor giving a potentially long recovery tail on the output side of the blocking capacitors. Each channel pair of the MPA4609 has relatively well-matched DC output offset (±200mV maximum difference). It is only the charging current required by this output offset difference that would need to be accounted for if the approach of Figure 6 where used under high input overdrive conditions.

Figure 6 shows an example piezoelectric amplifier where a Time Gain Control (TGC) amplifier follows the output to provide for an increasing gain with time. Depending on the propagation speed and attenuation of the medium, this gain would ramped up to compensate for the increasing losses with distance.

A piezoelectric sensor is modeled as a charge source with a shunt capacitor and resistor, or as a voltage source with a series capacitor and resistor. The 50Ω input resistors limit the current under high overdrive conditions that would flow into the Schottky clamp diodes. These diodes limit the maximum input to approximately ±0.4V—still well beyond the maximum useable input signal of ±20mV. Should very high overdrives occur, the MPA4609 allows the designer to switch to a dummy input, holding the output stage in range during this period. When the piezoelectric signal drops to < 20mV, the channel select may be switched back to this channel and the output detected.

The VCA610 is a differential input to ground referenced single-ended output voltage controlled gain amplifier. A constant bandwidth vs gain of 30MHz provides adequate bandwidth for this application.

The MPA4609 outputs are AC-coupled to grounded termination resistors. This removes the DC differential offset (as high as ±250mV) prior to the input to the VCA610. The inputs to the dummy channel are left open to provide the same DC source impedance to its input bias currents as the signal channel. This is intended to help match the DC output offset voltage as the channels are switched, minimizing settling tails through the output blocking capacitors.

As an example, use the VCA610 to adjust the gain over a 40dB range from –20dB to +20dB while the input to the MPA4609 goes from $20mV_{PP}$ maximum input to $200\mu V_{PP}$. The net gain through the MPA4609, including the input resistive attenuation and the divider at the input of the VCA610, will be 42.3dB nominally. At maximum input of $20mV_{PP}$, this gives a $2.6V_{PP}$ input to the VCA610. If it is operated at minimum gain at this point, then its –20dB gain will give an output of $260mV_{PP}$. As the input signal decreases down to $200\mu V_{PP}$, the gain of the VCA610 is increased to +20dB. With the input to the MPA4609 at $200\mu V_{PP}$, the input to the VCA610 will see $26mV_{PP}$ input. Then, with a gain of 20dB, this is brought back up to $260mV_{PP}$. The VCA610 could be used to continue adding another 20dB of gain, allowing the MPA4609 input to decrease to $20uV_{PP}$ while still producing a $260mV_{PP}$ at the VCA610 output—over 80dB of gain with > 20MHz bandwidth.

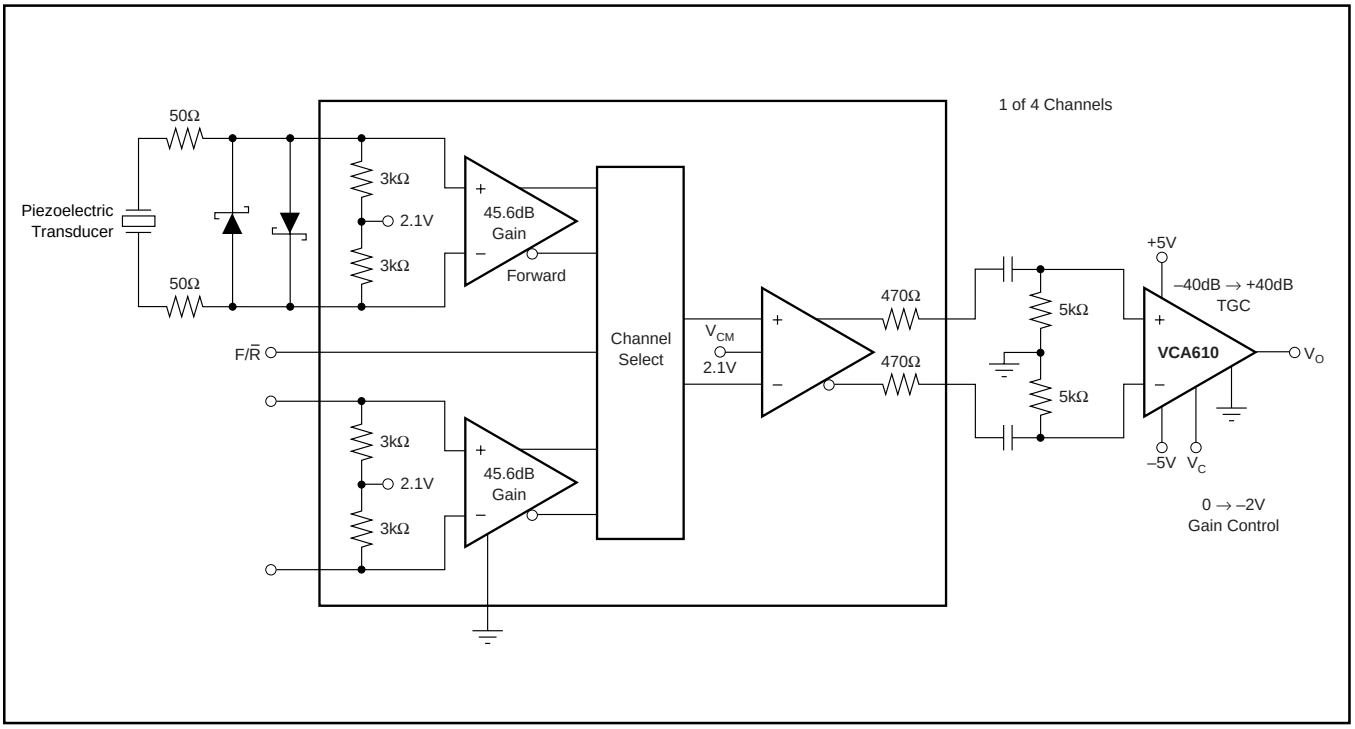



FIGURE 6. Sonar Amplifier with Time Gain Control.

One limiting factor to this approach is the input bias current noise times the 3kΩ bias resistors to the common-mode voltage at the input. That current, plus the 3kΩ resistor noise, combine to produce a 12nV/$\sqrt{Hz}$ total differential input noise. If the overall system noise power bandwidth is limited to 2MHz, this gives an input referred noise of 17$\mu V_{RMS}$. While a 200$\mu V_{PP}$ input will certainly still be detectable, the 20u$V_{PP}$ at maximum VCA610 gain of 40dB may be below the noise floor. Using an external common-mode voltage for the MPA4609 with lower resistors can improve this performance.

# OPERATING INFORMATION

## INPUT STAGE AND CHANNEL SWITCHING

Each channel pair of the MPA4609 provides two very low noise, bipolar, differential input stages that are selected by controlling their tail current sources with their output collectors connected together. Figure 7 shows a simplified schematic for one channel pair with the channel select circuitry shown.

The active input channel is selected by controlling which stage is biased by their tail current sources (Q5 or Q12). The F/$\overline{R}$ pin controls a simple differential stage (Q15 and Q16) that steers small currents to the emmitters of Q7 and Q14. Given a fixed-base string bias voltage for those two current mirror transistors, a small current through their emmitter resistors is adequate to shut off one or the other transistor. A low voltage on the F/$\overline{R}$ pin will steer $I_B$ to the Q7 emmitter, shutting off the bias for Q5 and turning off the forward input transistor pair (Q1 and Q2). Conversely, zero current out of Q16 leaves the bias to Q12 operating turning on the Reverse channel inputs.

Both inputs are biased through 3kΩ resistors to the internal $V_{CM,}$ a 2.1V bandgap reference with minimal temperature drift. The specified input common-mode voltage is slightly reduced from this 2.1V by the input transistor base currents through the 3kΩ resistors. Each input stage transistor collector is also bootstrapped through a second set of transistors (Q3, Q4 and Q10, Q11) that cascode the signal current through to the 2nd stage. These cascode transistors also have a base voltage provided from $V_{CM}$ increased by 1 diode drop. This holds the nominal base-collector voltage of the input transistors (Q1,Q2, and Q8, Q9) at 0V. This arrangement improves the off channel isolation and PSRR giving improved attenuation from an input signal present at the inputs of a de-selected input to the output current from these cascode transistors. This does, however, limit the available positive going common-mode input voltage to only 300mV above $V_{CM}$. Higher input common-mode voltages (when the source is overriding the internally set common-mode input voltage) will start to forward bias the base-collector junction for the input transistors (Q1, Q2, and Q8, Q9). There is more room going negatively to override the input common-mode voltage, where the limit is the saturation of Q5 or Q12.

## OUTPUT STAGE OPERATION

The output stage is a unity-gain differential I/O buffer including a common-mode control loop to hold the output common-

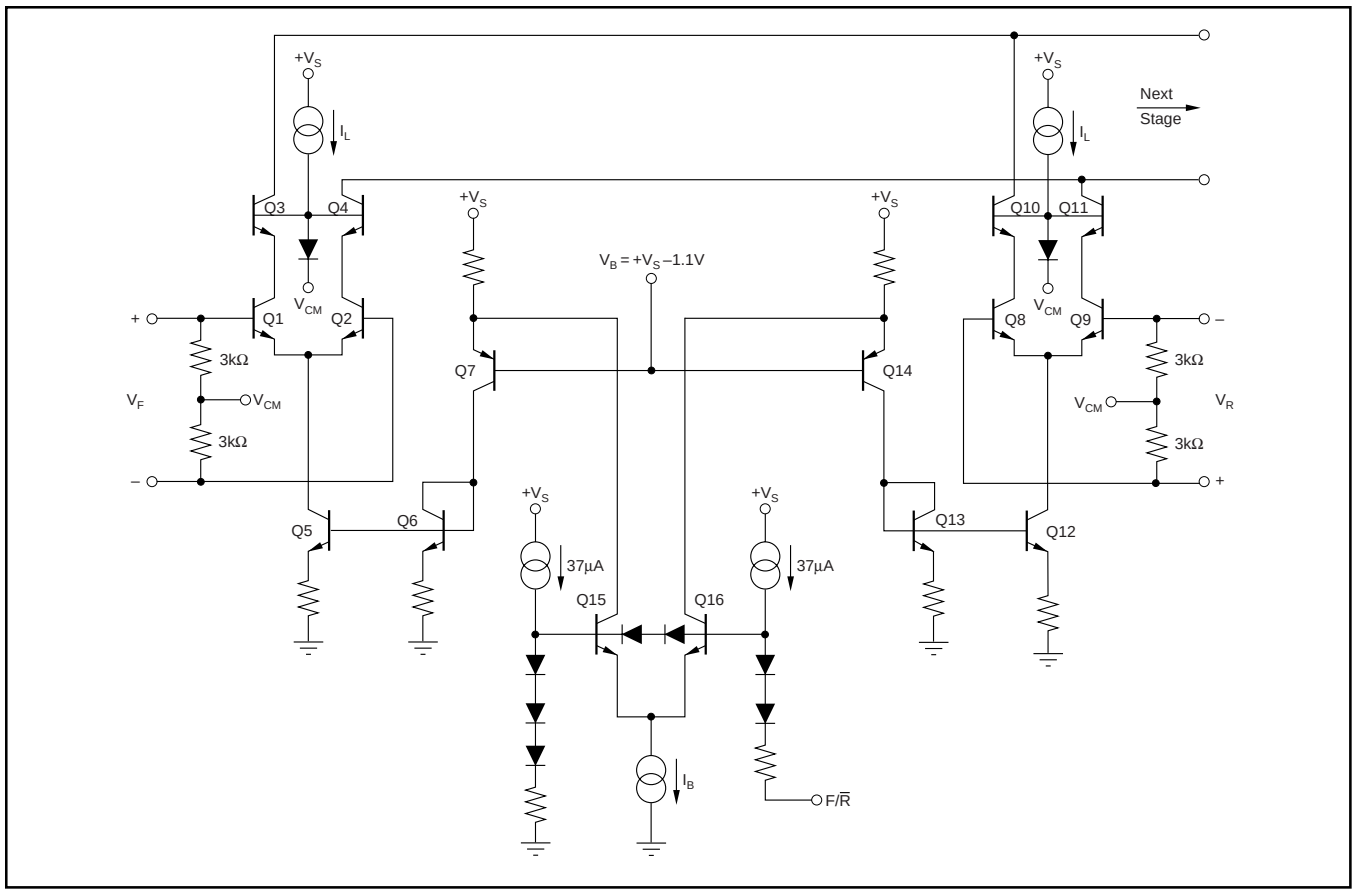



FIGURE 7. Input Stage Schematic (1 of 4 channels).

mode voltage at the internal bandgap reference ($V_{CM}$). Figure 8 illustrates each of the four output stages, showing a common-mode feedback point picked off prior to the 470Ω series output resistors.

The common-mode loop will serve to set these internal nodes to $V_{CM}$, regardless of what is happening on either the input stage or output loading. Under output voltage overdrive

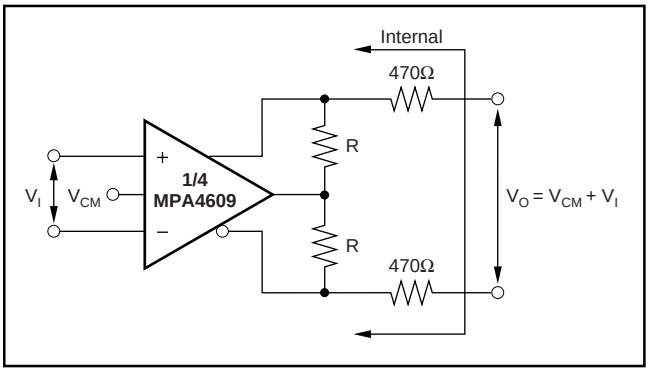



FIGURE 8. Output Stage Buffer.

conditions, the output limit is set asymmetrically around $V_{CM}$, causing the common-mode control loop to servo out of position while the overdrive is present. When removed, the output common-mode voltage will recover as shown in the Typical Characteristic curves. It is important to consider that not only will the outputs clip in overdrive (with a fast 50ns recovery) for the differential voltage, but there will be a relatively slow tail in the common-mode voltage recovery after the overdrive is removed.

Some applications for the MPA4609 require the signal gain to be attenuated. This is most easily achieved by placing a resistor across the two outputs to attenuate the differential signal, with no common-mode loading on the output. Figure 9 shows an example where a 940Ω resistor between the outputs attenuates the differential gain for the MPA4609 to 95V/V nominally.

An alternative method would be to connect a resistor to ground on each output. This will attenuate both the differential gain while also level-shifting the common-mode voltage

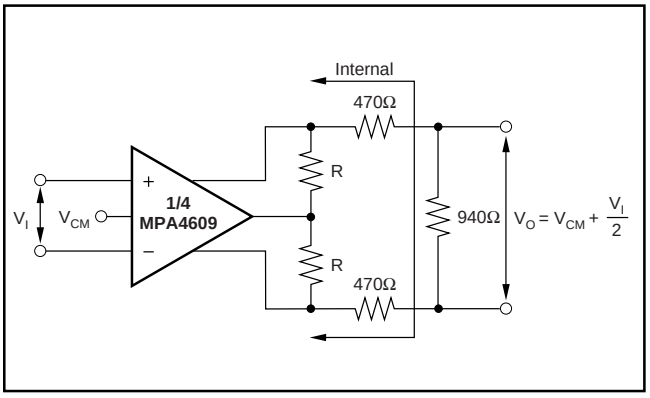



FIGURE 9. Differential Gain Attenuation..

by the same attenuation. Figure 10 shows this approach where the $V_{CM}$ and $V_I$ is attenuated by 1/2, but in this case also requires a 2.1V/(940Ω) = 2.2mA bias current from each output and drops the common-mode voltage at the load to $1.05V_{DC}$.

The internal output stage resistors may be used to implement a simple low-pass filter as part of the signal path. For instance, if a simple 50MHz low pass pole were desired,

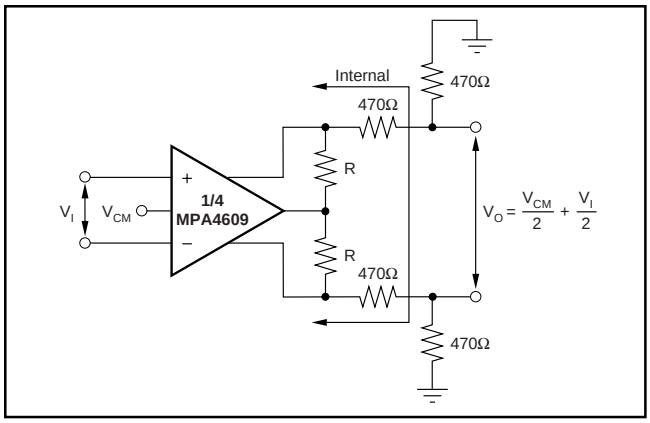



FIGURE 10. Grounded Load Attenuation.

often to limit noise power bandwidth, two capacitors to ground (one on each output) equal to 6.8pF would be needed. This can also be implemented as a single capacitor across the outputs of 1/2 this value, or 3.4pF. These low values also indicate the strong effect that layout parasitic capacitance can have on the overall signal bandwidth. With a 470Ω internal output impedance, very little external parasitic capacitance can limit the signal bandwidth. If external gain attenuation resistors are used, the source impedance becomes the parallel combination of the 470Ω and these external resistors. For instance, Figure 11 shows the gain of 95V/V condition of Figure 9 with an added differential capacitance to set the frequency response for the differential output signal to 50MHz. Since the source impedance on each side is now effectively 470Ω || 470Ω = 235Ω, the single-ended capacitor required would double to 13.6pF from that calculated above, and then drop to 6.8pF if implemented as a capacitor across the outputs.

## HARMONIC DISTORTION

Being a differential I/O device, the MPA4609 shows lower 2nd-harmonic distortion than 3rd-harmonic distortion. This

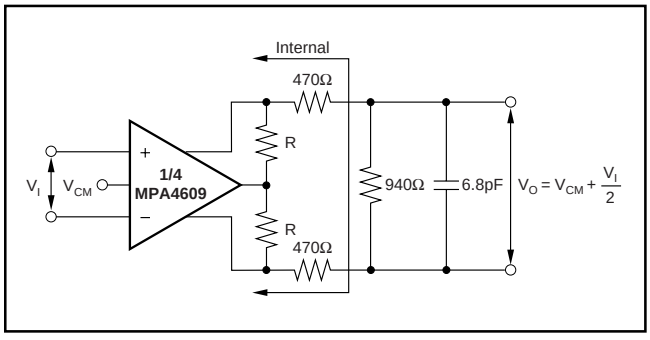



FIGURE 11. Bandlimited Output Stage.

dominant 3rd-order term holds at very low levels through frequencies that are a significant portion of the available –3dB bandwidth due to the open loop design. Since the differential output distortion is dominated by the 3rd-order harmonic, passive postfiltering can be very effective at improving the SFDR at the filter output. For instance, the Typical Characteristics show the 3rd-order harmonic distortion increasing rapidly above the 10MHz fundamental from a low –65dBc for a $2V_{PP}$ output. If the maximum desired input frequency is 20MHz, a 2nd-order low pass filter placed with a $F_{-3dB}$ at 30MHz will hold the distortion out of the filter at the 10MHz level. As the fundamental frequency rises above 10MHz, the dominant 3rd-order distortion term is extending beyond the 30MHz cutoff of the filter. The rolloff of a 2nd-order filter exceeds the rate of increase for the 3rd-harmonic in going from 10MHz to 20MHz. At 20MHz input, the 3rd-harmonic occurs at 60MHz—well into the cutoff region of the filter.

Figure 12 shows an example RLC filter design where a high-pass pole at 100kHz is included, and the converter common-mode input voltage is used to reference the filter output. This filter is designed to provide a –3dB frequency at 30MHz with exceptional flatness through 20MHz.

The design methodology for this type of filter can be found in TI application note SBAA108. The simulated frequency response for this filter is shown in Figure 13.

Looking at this response, there is a slight (1dB) attenuation in the passband due to the resistor divider loss. The filter was designed with a slight peaking, which does show up and extends the bandwidth slightly. Of most interest is the attenuation for the 3rd-harmonic at 10MHz and 20MHz fundamental frequencies. The MPA4609 shows –65dBc for a $2V_{PP}$ output at 10MHz. This harmonic, falling at 30MHz, will be attenuated 2.5dB at the filter output to give –67.5dB SFDR. As the input frequency moves up to 20MHz, the MPA4609 shows –53dBc 3rd-harmonic distortion. This term falls at 60MHz where the filter is giving about 11.5dB attenuation. Hence, the filter output will show an SFDR of –64.5dBc at 20MHz—only slightly different than the 10MHz result.

The Typical Characteristics also show a high 3rd-order, two-tone, intermodulation intercept. For measurement purposes, a relatively low 500Ω load across the outputs was used. The intercept for lighter loads, such as ADC inputs, will be higher than for this 500Ω load. Since this is not a 50Ω environment, more typically used in intercept plots, the 37dBm intercept shown in the Typical Characteristics will need some interpretation. This plot was actually the Intercept for the differential *voltage* swings for two closely-spaced tones at the output prior to the 470Ω series output resistors. To predict the intermodulation SFDR, calculate the single-tone power at this internal point as if it were driving 50Ω, then use the familiar intercept equation to predict how far down (dBc) the 3rd-order spurious levels will be.

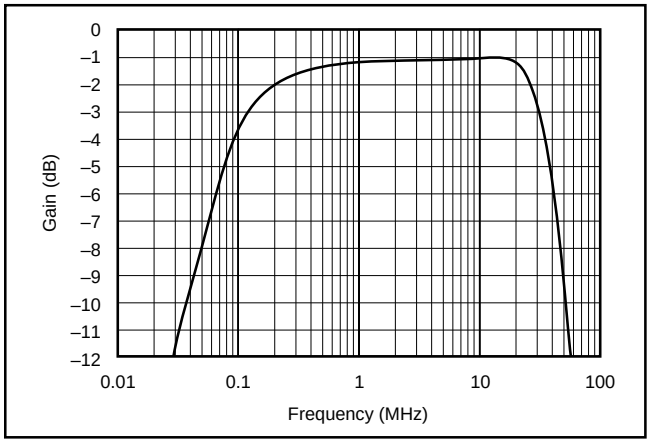



FIGURE 13. Simulated Frequency Response for Differential Filter.

For instance, if a $2V_{PP}$ 2-tone envelope is needed at the internal output nodes ($V'_O$ in Figure 1), consider each $1V_{PP}$ tone to be the 4dBm that would be strictly correct for a 50Ω load across these internal nodes. Then, the 3rd-order spurious levels will be 2 • (IM3 – 4dBm) below the power level of the two carriers. With a 37dBm intercept (IM3), this predicts the 3rd-order intermodulation terms to be 2 • (37 – 4) = 66dBc below the carrier. This is very consistent with the 3rd-harmonic distortion, which is also 66dBc below a $2V_{PP}$ output for frequencies up to 10MHz. The output interface will not change the relative levels of the carrier vs. 3rd-order intermodulation spurious levels. Similarly, at lower output swings, the SFDR improves significantly as shown in both the harmonic distortion vs. output swing and the intercept plots. At $1V_{PP}$ output, (at $V'_O$), the 3rd-harmonic distortion is –78dBc down. For an equal power 2-tone envelope, each tone is at $0.5V_{PP}$ differential or –2dBm for the analysis here. With a 37dBm intercept, this calculates to a 3rd-intermodulation order, spurious-free-range of 2 • (37 – (–2)) = –78dBc.

## TOTAL OUTPUT NOISE CALCULATION

The total output noise can be very low, given the 0.65nV/$\sqrt{Hz}$ input voltage noise. To take full advantage of this low voltage

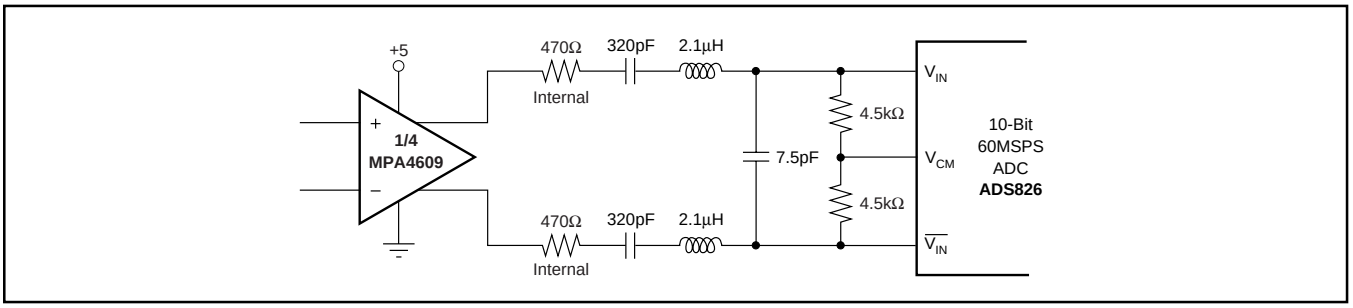



FIGURE 12. 3rd-Order Filter to Improve Harmonic Distortion.

noise, careful attention to the source impedance and PSRR are needed. Figure 14 shows a general analysis circuit for the differential output noise for the MPA4609.

This circuit includes a common-mode reference voltage noise source. This can normally be neglected if:

1. There is no real ground (AC or DC) at the midpoint of the source resistor—if $R_S$ is simply connected across the inputs, the common-mode bias noise remains common-mode, and will only appear at the output as the CMRR rolls off with frequency. The Typical Characteristics show the CMRR remains > 20dB through 40MHz. This rejection is defined to the output differential signal. For common-mode noise as high as 100nV/$\sqrt{Hz}$, this will appear as a differential output noise of < 10nV/$\sqrt{Hz}$ through 40MHz. To input refer this portion of the output noise, divide by the minimum differential gain of 160V/V to get an input referred contribution equal to 0.06nV/$\sqrt{Hz}$ that can certainly be neglected.
2. If the source does have an AC or DC centerpoint ground, the common-mode noise will remain a common-mode input noise source as long as the voltage divider formed by the 3kΩ bias resistor and the source impedance on each side is well-balanced. Low-source impedances, normally required for an overall low noise path, will also attenuate the available common-mode input noise across the inputs. For instance, using 1/2 of the 65Ω test condition source impedance to a centerpoint AC ground will attenuate the common-mode noise by 32.5Ω/3.03kΩ = 0.0011 (60dB). Even for a common-mode noise voltage as high as 100nV/$\sqrt{Hz}$, this will get to the inputs as a 0.1nV/$\sqrt{Hz}$ term. Then, even for divider imbalances as high as 10%, this will give only 0.01nV/$\sqrt{Hz}$ differential noise contribution.

Given the excellent CMRR rejection for the MPA4609, the common-mode noise source, while present, will be neglected from the noise analysis. Combining $R_S$ in parallel with $R_B$ ($R_S$ || $R_B$ = $R_T$) will give the total input referred differential noise expression of Equation 2.

$$e_n = \sqrt{e_{ni}^2 + 2\left(R_T i_b\right)^2 + 2\left(4kTR_T\right)} \qquad \left(4kT = 1.6E-20J \text{ at } 290°k\right) \tag{2}$$

Using the typical values for noise and resistors ($R_T$ = 32.2Ω) will give a total input-referred differential voltage noise shown in Equations 3a → 3c.

$$e_n = \sqrt{(0.65nV)^2 + 2(32.2\Omega \bullet 3.8pA)^2 + 2(1.6E-20 \bullet 32.2\Omega)} \tag{3a}$$

$$= \sqrt{(0.65nV)^2 + (0.17nV)^2 + (1.02nV)^2}$$

$$= 1.22nV / \sqrt{Hz} \tag{3b}$$

The individual noise terms shown in Equation 3b show that (3c) the dominant noise term is the resistor noise of the source. The low input voltage and current noise terms for the MPA4609 increase the total input noise voltage only slightly over the Johnson noise of the resistor itself.

Taking this total input-referred differential voltage noise to the output, and integrating over a noise-power bandwidth set only by the 1-pole rolloff of the MPA4609 itself, will give the a total output RMS noise shown in Equations 4a → 4c.

$$e_{O_{RMS}} = e_n \bullet Gain \bullet \sqrt{Bandwidth \bullet 1.54}$$

$$e_{O_{RMS}} = 1.22nV / \sqrt{Hz} \bullet 190V/V \bullet \sqrt{90MHz \bullet 1.54} \tag{4a}$$

$$e_{O_{RMS}} = 2.7mV_{RMS} \tag{4b}$$

More narrowly restricting the noise-power bandwidth will reduce this integrated noise. For instance, using the 30MHz, (4c) 2nd-order filter of Figure 12 will reduce the noise-power

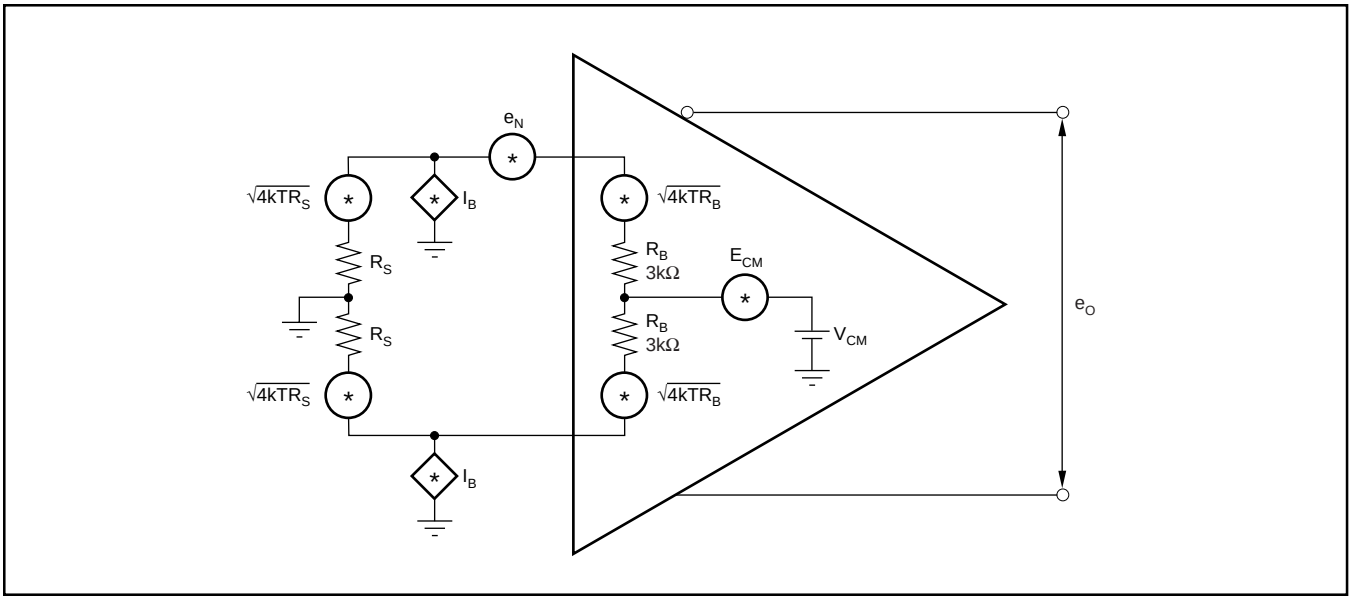



FIGURE 14. Output Noise Analysis Circuit.

bandwidth to approximately 1.11 • $F_{-3dB}$ = 33.3MHz. This will give a differential RMS output noise given by Equations 5a → 5b.

$$e_{O_{RMS}} = 1.22nV/\sqrt{Hz} \bullet 190V/V \bullet \sqrt{30MHz \bullet 1.1}$$

$$e_{O_{RMS}} = 1.34mV_{RMS} \quad (5a)$$

A more complete noise analysis description can be found in TI application note SBOA066, *Noise Analysis for High Speed Op Amps*. (5b)

One added contribution to apparent output noise can be power supply noise coming through to the output. The MPA4609 provides good PSRR (defined as going from the supply to the differential output voltage). The Typical Characteristics show a PSRR holding above 20dB through 30MHz. To estimate the contribution of power-supply noise, consider an example of 10mV of system clocking related noise at 30MHz. This will come through to the output as approximately a 1mV differential signal given the 20dB PSRR at 30MHz. To input-refer this, divide by the 190V/V gain to get an equivalent input-referred term of 5.2µV.

High-frequency glitches on the supply can have significant harmonic content well above this 30MHz frequency. If the system can be expected to have large, high-frequency, clock noise on the supplies, a PI filter into the MPA4609 supply pins can be used to reduce their amplitude adequately to limit their contribution to the output signal. An example design is shown in Figure 15.

For instance, at 30MHz the two-1000pF capacitors show a 2.65Ω impedance (the 0.1µF capacitor has gone self-resonant at 10MHz typically) while the ferrite bead shows approximately 80Ω (from the manufacturers data sheet for the part number shown) to give a 30dB attenuation at 30MHz. By 90MHz, the capacitive impedance is dropped to 0.9Ω while the ferrite bead has increased to 130Ω to give a 43dB attenuation in supply noise.

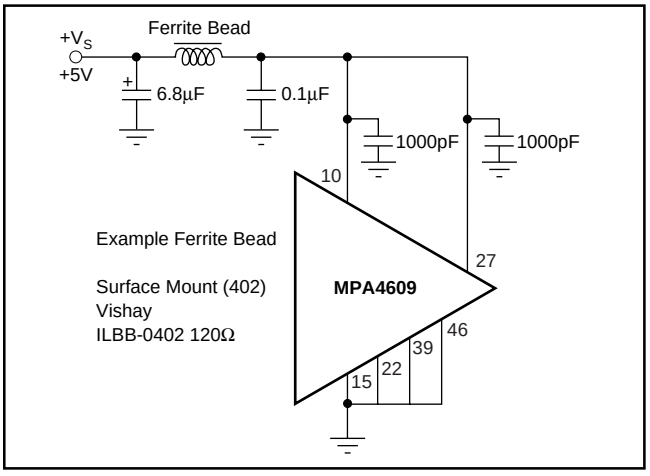



FIGURE 15. Power Supply PI Filter for Improved PSRR.

## CHANNEL SELECT OPERATION

Figure 7 shows a simplified channel select circuit as part of the input stage schematic. The channel select includes an internal level shift through two diodes to compare into a differential stage biased with three diodes above ground. Full switching of the differential stage occurs at approximately two diodes above ground (plus a slight IR drop) to give the nominal 1.25V switching point. The reverse channel will be selected when the F/$\overline{R}$ pin voltage is < 0.9V while the forward channel will be selected when the control pin voltage is > 1.6V. Leaving the F/$\overline{R}$ pin unconnected will default to the high state with the Forward channels selected. This low switching threshold, with minimal current requirements, allows very low-voltage CMOS logic to be directly interfaced to the F/$\overline{R}$ pin.

When the F/$\overline{R}$ pin is at ground, each channel select circuit sends approximately 35µA out of the F/$\overline{R}$ pin. Since there are two channels on each of the two select pins (pins 3 and 34), this give the specified total sinking current when each F/$\overline{R}$ pin is low of 70µA in each pin. As the control logic goes high, this bias current is diverted through two diodes connected across the differential stage—intended to clamp the maximum differential voltage across this stage. This gives a zero current requirement at the control pins in the logic high state.

## THERMAL ANALYSIS

Neither heatsinking nor airflow will be required for most applications of the MPA4609. Exceptional performance over temperature is maintained using carefully designed temperature coefficients for the quiescent currents in each stage. The common-mode reference shows very little change over temperature. The limit to operation will then be either the maximum system defined junction temperature or the specified absolute maximum of junction temperature of 150°C.

Operating junction temperature ($T_J$) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation ($P_D$) is the sum of quiescent power ($P_{DQ}$) and additional power dissipated in the output stage ($P_{DL}$) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. $P_{DL}$ will be very low due to the internal 470Ω output resistors. To get a worst-case output stage power estimate, consider the outputs to be grounded—giving an average output current on each side set by $V_{CM}$/470Ω = 4.5mA. Putting 4.5mA in each of the eight output stages (two for each of the four differential pairs) times the total internal voltage drop of $V_S$ gives an absolute worst- case output stage power dissipation = 180mW total for all channels.

Continuing this worst-case example, compute the maximum $T_J$ using this maximum output stage power and the maximum quiescent power. Operating at the maximum specified ambient temperature of +85°C, the maximum internal power is given in Equation 6:

$$P_D = 5V \bullet 52mA + 180mW = 440mW$$
$$\text{Maximum } T_J = +85°C + (0.44W \bullet 60°C/W) = 111.4°C \quad (6)$$

All actual applications will operate at a lower junction temperature than the 111.4°C computed above. Compute your actual output stage power to get an accurate estimate of

maximum junction temperature, or use the results shown here as an absolute maximum.

The "I" suffix indicates operation from –40°C to +85°C ambient. As the Typical Characteristic curves show, D.C. performance is stable over a very wide temperature range. However, since the intended application is only for a commercial 0°C to +70°C range, min/max specifications are provided only over this range.

## BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier like the MPA4609 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

**a) Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause unintentional bandlimiting of the signal. To reduce unwanted capacitance, create a window around the signal I/O pins in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board. Also, since the outputs are differential, maintain adequate output trace separation to keep the parasitic differential output capacitance low.

**b) Minimize the distance** (< 0.25") from the power supply pins to high frequency 0.1µF and 1000pF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

**c) Careful selection and placement of external components will preserve the high frequency performance of the MPA4609.** Use resistors that have low reactance at high frequencies. Surface mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pins are the most sensitive to parasitic capacitance, always position the series output blocking capacitor, if any, as close as possible to the output pin. Keep resistor values as low as possible, consistent with load driving considerations.

**d) Socketing a high-speed part like the MPA4609 is not recommended**. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the MPA4609 onto the board.

### INPUT AND ESD PROTECTION

The MPA4609 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are not reflected in the Absolute Maximum Ratings table as this device is only intended for +5V (±10%) supply operation. Internal breakdowns are typically > 12V, but an Absolute Maximum Rating of +7V is shown to limit application at supplies far higher than the MPA4609 design and characterization point.

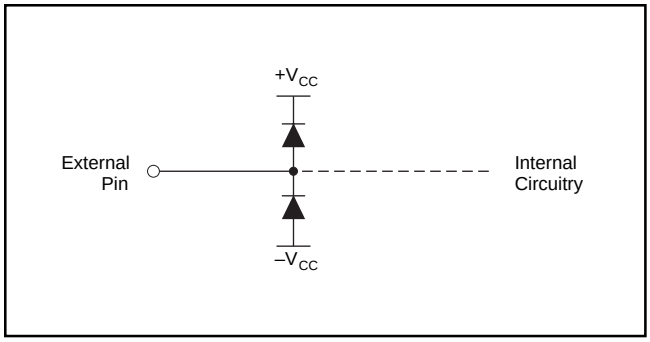



FIGURE 16. Internal ESD Protection.

All device I/O pins are protected with internal ESD protection diodes to the power supply and ground as shown in Figure 16.

These diodes provide moderate protection to input overdrive voltages beyond the supply and ground as well. The protection diodes can typically support 30mA continuous current. Where large common-mode or differential mode transients are possible, current limiting series resistors may be added on the differential inputs. Keep this resistor value as low as possible since high values degrade both noise performance and frequency response.

## Revision History

| DATE | REVISION | PAGE | SECTION | DESCRIPTION |
|---|---|---|---|---|
| 12/08 | E | 2 | Absolute Maximum Ratings | Changed minimum Storage Temperature Range from –40°C to –65°C. |

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MPA4609IPFBR | OBSOLETE | TQFP | PFB | 48 | | TBD | Call TI | Call TI | 0 to 70 | MPA4609 | |
| MPA4609IPFBRG4 | OBSOLETE | TQFP | PFB | 48 | | TBD | Call TI | Call TI | 0 to 70 | | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

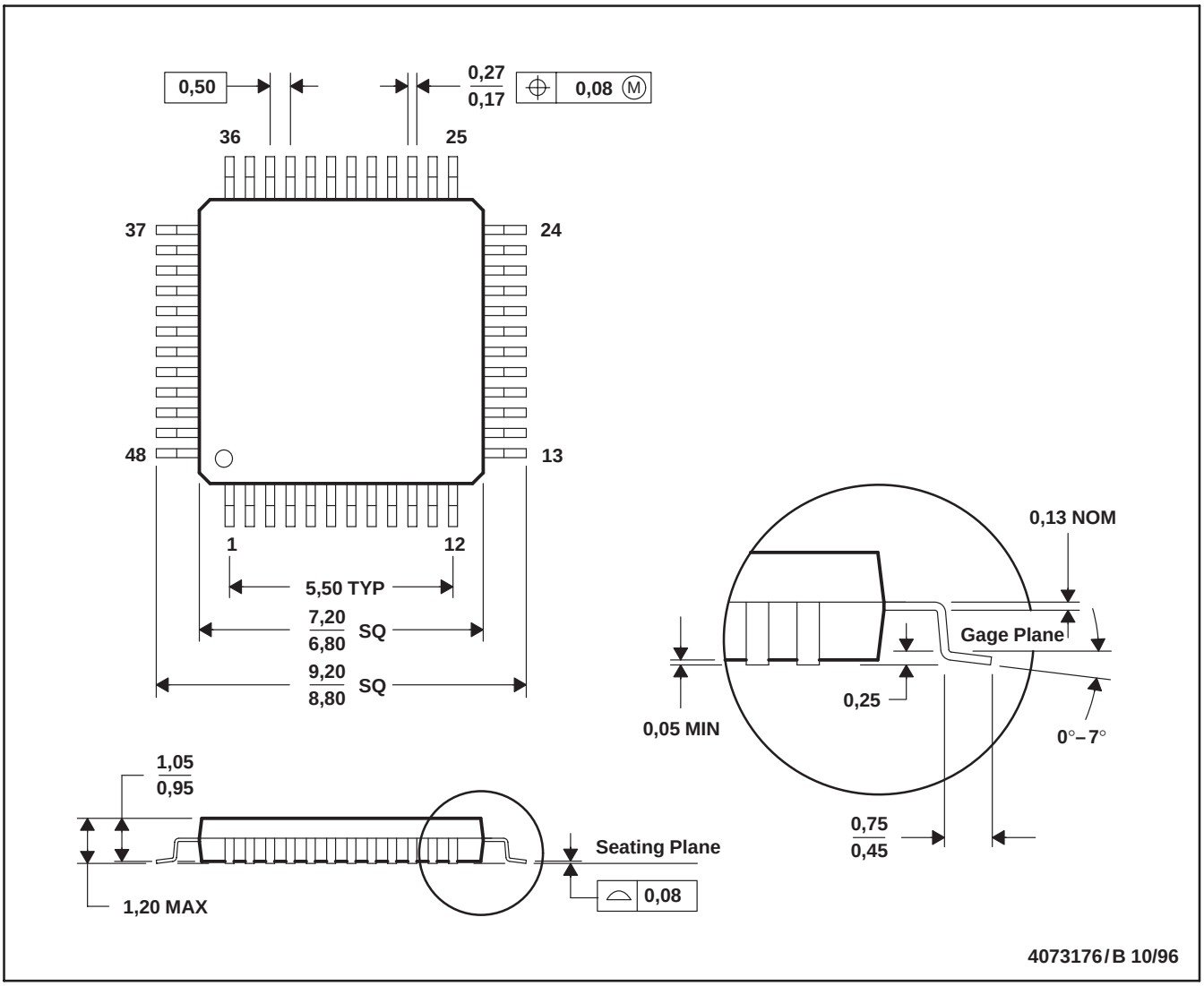
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

**PFB (S-PQFP-G48)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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