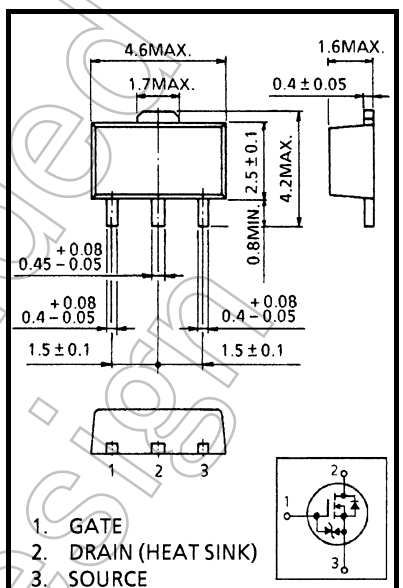
TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (L^2-π-MOS V)

2SK2963

DC-DC Converter, Relay Drive and Motor Drive Applications

- 4-V gate drive
- Low drain-source ON-resistance: $R_{DS\ (ON)}$ = 0.5 Ω (typ.)
- High forward transfer admittance: $|Y_{fs}|$ = 1.2 S (typ.)
- Low leakage current: I_{DSS} = 100 μA (max) (V_{DS} = 100 V)
- Enhancement mode: V_{th} = 0.8 to 2.0 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-5K1B

Weight: 0.05 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	100	V
Drain-gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	100	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	1	A
	Pulse (Note 1)	I_{DP}	3	
Drain power dissipation		P_D	0.5	W
Drain power dissipation (Note 2)		P_D	1.5	W
Single pulse avalanche energy (Note 3)		E_{AS}	137	mJ
Avalanche current		I_{AR}	1	A
Repetitive avalanche energy (Note 4)		E_{AR}	0.05	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Mounted on a ceramic board (25.4 mm × 25.4 mm × 0.8 mm)

Note 3: V_{DD} = 25 V, T_{ch} = 25°C (initial), L = 221 mH, R_G = 25 Ω, I_{AR} = 1 A

Note 4: Repetitive rating: pulse width limited by maximum junction temperature.

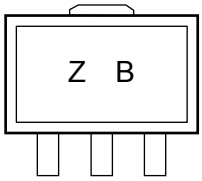
Note 5: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/”Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device.
Handle with care.

Thermal Characteristics

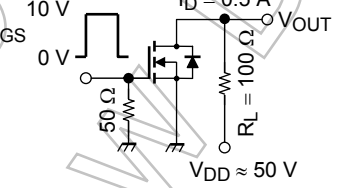
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient	$R_{th\ (ch\text{-}a)}$	250	°C/W

Marking



(The two digits represent the part number.)

Electrical Characteristics (Ta = 25°C)

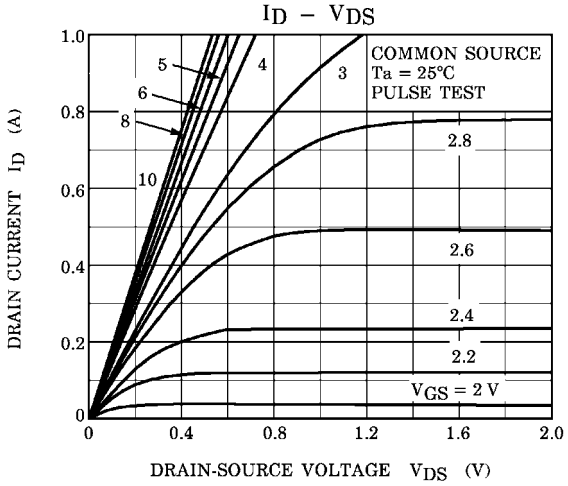
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut-off current		I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	100	μA
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	0.8	—	2.0	V
Drain-source ON resistance		$R_{DS\ (ON)}$	V_{GS} = 4 V, I_D = 0.5 A	—	0.65	0.95	Ω
			V_{GS} = 10 V, I_D = 0.5 A	—	0.5	0.7	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V, I_D = 0.5 A	0.6	1.2	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	140	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	20	—	pF
Output capacitance		C_{oss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	45	—	pF
Switching time	Rise time	t_r		—	8	—	ns
	Turn-on time	t_{on}		—	13	—	
	Fall time	t_f		—	45	—	
	Turn-off time	t_{off}		—	175	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 80 V, V_{GS} = 10 V, I_D = 1 A	—	6.3	—	nC
Gate-source charge		Q_{gs}	V_{DD} ≈ 80 V, V_{GS} = 10 V, I_D = 1 A	—	4.3	—	nC
Gate-drain (“miller”) charge		Q_{gd}	V_{DD} ≈ 80 V, V_{GS} = 10 V, I_D = 1 A	—	2	—	nC

Duty ≤ 1%, t_w = 10 μs

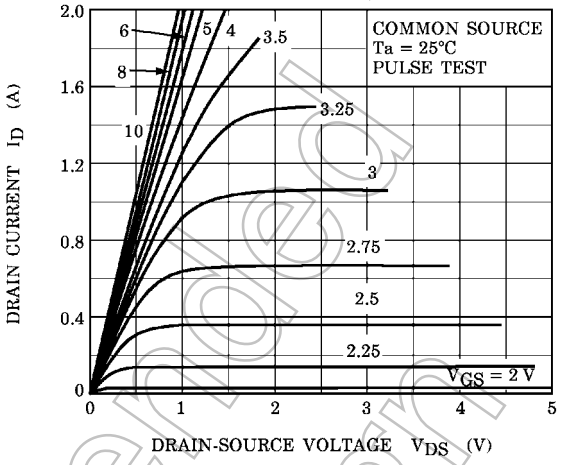
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	1	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	3	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 1 A, V_{GS} = 0 V	—	—	−1.5	V
Reverse recovery time	t_{rr}	I_{DR} = 1 A, V_{GS} = 0 V, dI_{DR}/dt = 50 A/μs	—	80	—	ns
Reverse recovery charge	Q_{rr}	I_{DR} = 1 A, V_{GS} = 0 V, dI_{DR}/dt = 50 A/μs	—	140	—	μC

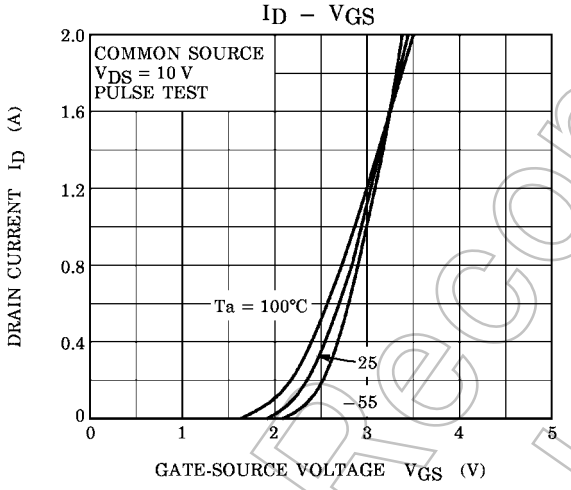
$I_D - V_{DS}$



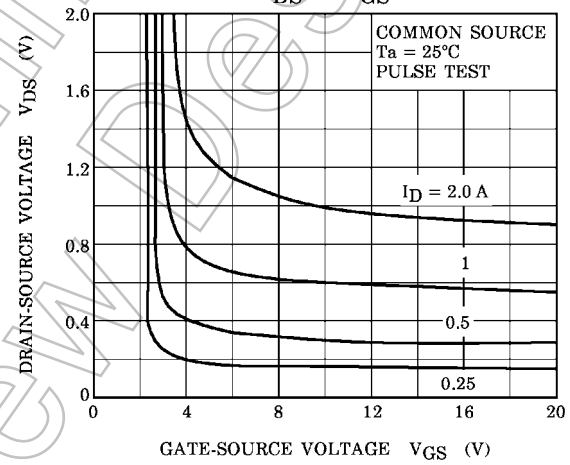
$I_D - V_{DS}$



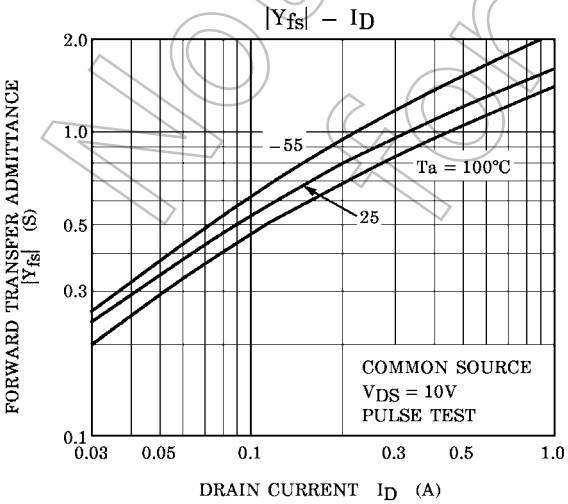
$I_D - V_{GS}$



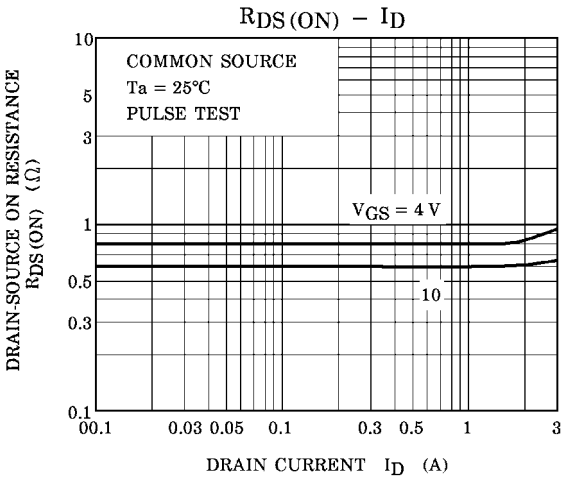
$V_{DS} - V_{GS}$



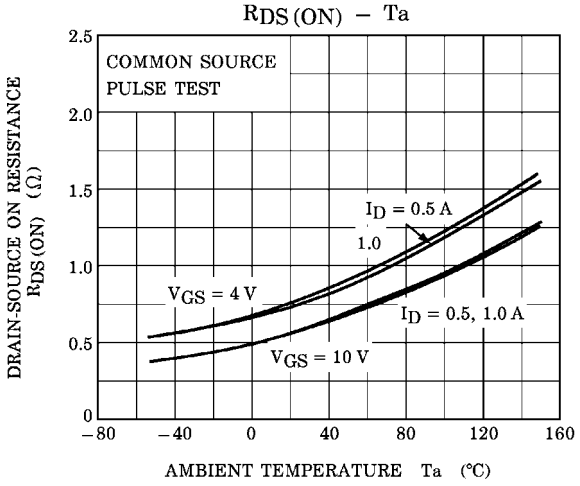
$|Y_{fs}| - I_D$



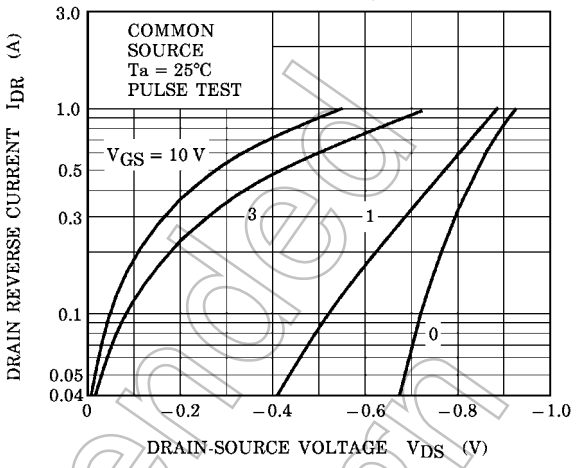
$R_{DS(ON)} - I_D$



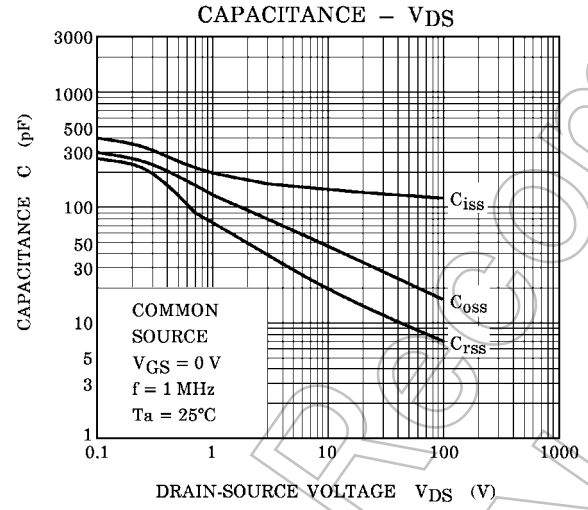
$R_{DS\,(ON)}$ – Ta



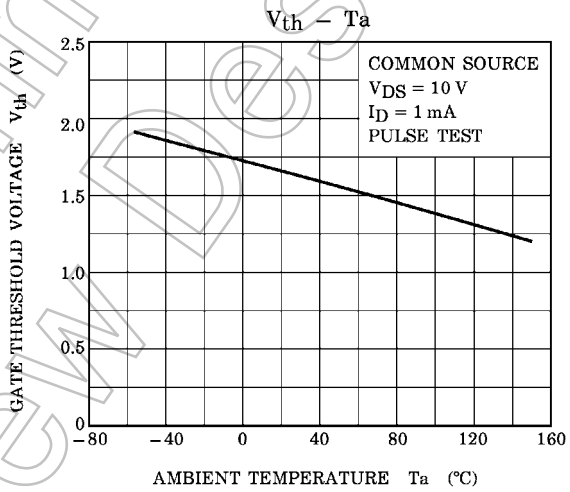
I_{DR} – V_{DS}



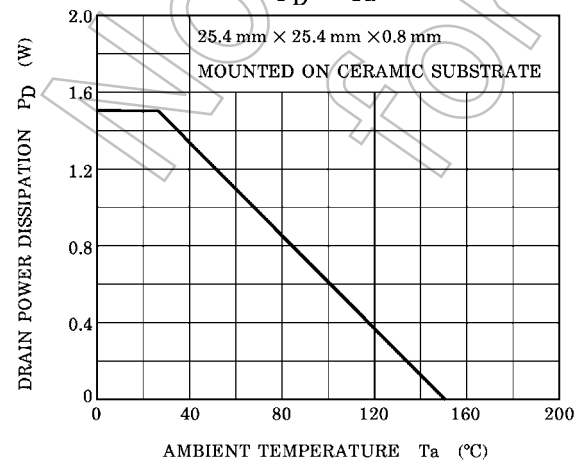
CAPACITANCE – V_{DS}



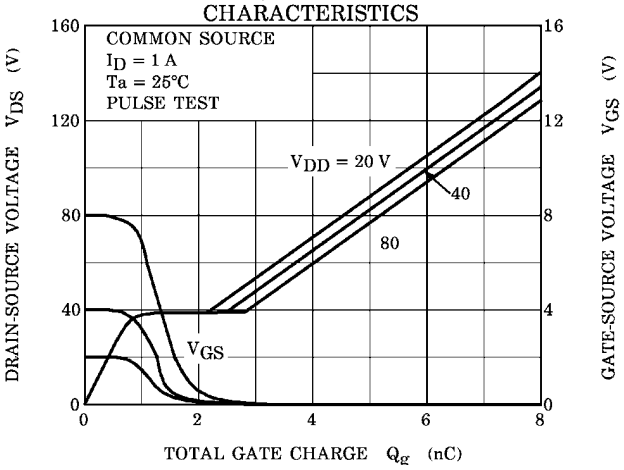
V_{th} – Ta



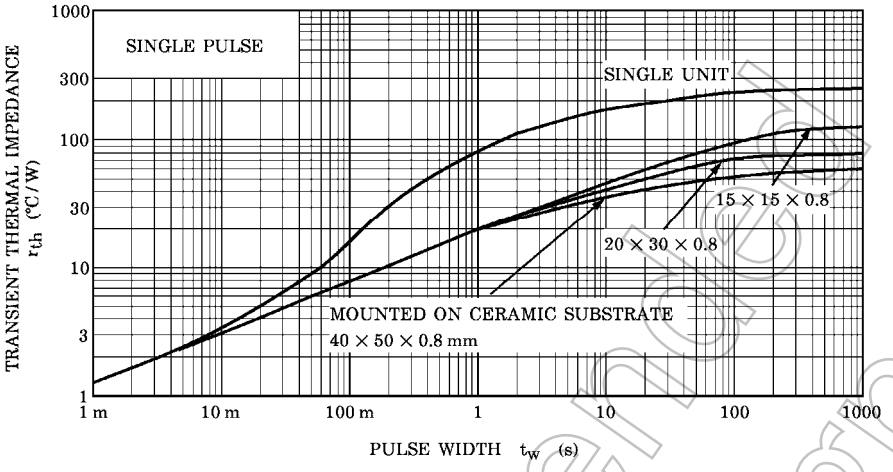
P_D – Ta



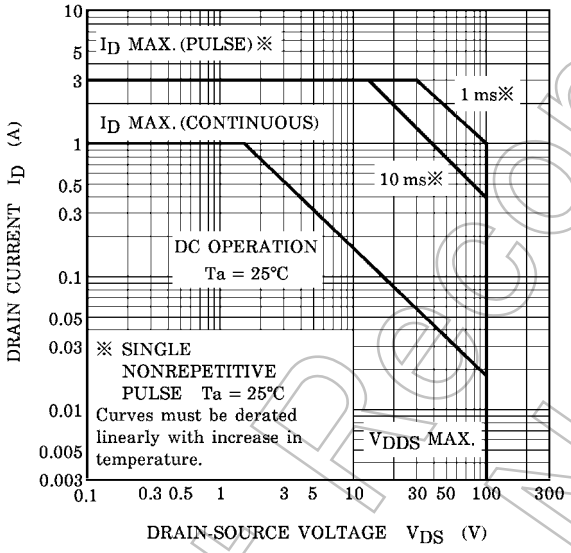
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



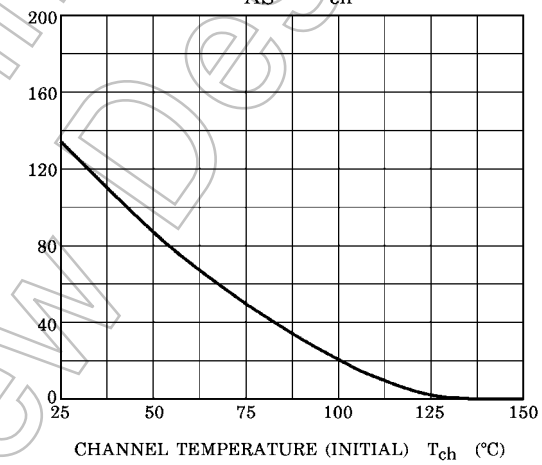
r_{th} – t_w

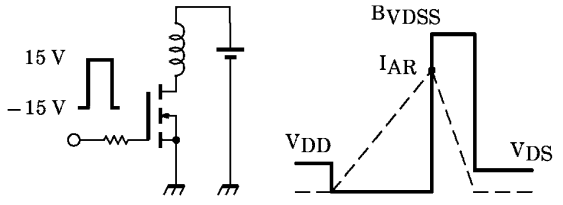


SAFE OPERATING AREA



E_{AS} – T_{ch}





TEST CIRCUIT WAVE FORM

$R_G = 25\ \Omega$
$V_{DD} = 25$ V, L = 221 mH

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$

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