ESD Protection Diodes Silicon Epitaxial Planar

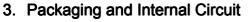
# DF2S6.8MFS

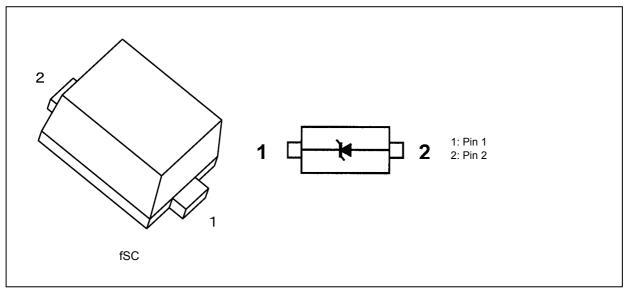
### 1. Applications

- ESD Protection
- Note: This product is designed for protection against electrostatic discharge (ESD) and is not intended for any other purpose, including, but not limited to, voltage regulation.

#### 2. Features

- (1) Ultra compact packaging for easy configuration in any ESD protection circuits.
- (2) Low total capacitance:  $C_t = 0.5 \text{ pF}$  (typ.).





### 4. Absolute Maximum Ratings (Note) (Unless otherwise specified, $T_a = 25^{\circ}C$ )

Characteristics	Symbol	Rating	Unit
Electrostatic discharge voltage (IEC61000-4-2)(Contact)	V <sub>ESD</sub>	±8	kV
Junction temperature	Tj	150	°C
Storage temperature	T <sub>stg</sub>	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

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### 5. Electrical Characteristics (Unless otherwise specified, $T_a = 25^{\circ}C$ )

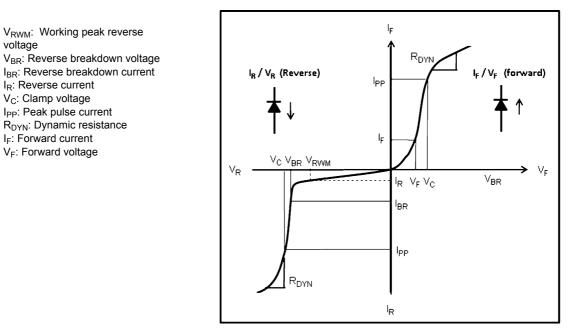


Fig. 5.1 Definitions of Electrical Characteristics

Characteristics	Symbol	Note	Test Condition	Min	Тур.	Max	Unit
Working peak reverse voltage	V <sub>RWM</sub>		_	_	_	5.0	V
Reverse breakdown voltage	V <sub>BR</sub>		I <sub>BR</sub> = 5 mA	6.0	_	_	V
Reverse current	I <sub>R</sub>		V <sub>RWM</sub> = 5 V	_		0.5	μA
Clamp voltage	V <sub>C</sub>	(Note 1)	I <sub>PP</sub> = 1 A	_	15	_	V
Dynamic resistance	R <sub>DYN</sub>	(Note 2)		_	1.3	_	Ω
Total capacitance	Ct	(Note 3)	V <sub>R</sub> = 0 V, f = 1 MHz	_	0.5	0.9	pF

Note 1: Based on IEC61000-4-5 8/20  $\mu s$  pulse.

Note 2: TLP parameter: Z0 = 50  $\Omega$ , tp = 100 ns, tr = 300 ps, averaging window: t1 = 30 ns to t2 = 60 ns,

extraction of dynamic resistance using a least-squares fit of TLP characteristics at  $I_{PP}$  between 3 A to 8 A. Note 3: Guaranteed by design.

### 6. Guaranteed ESD Protection (Note)

Test Condition	ESD Protection
IEC61000-4-2 (Contact discharge)	±8 kV

Note: Criterion: No damage to devices.

### 7. Marking

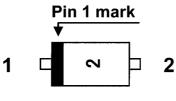


Fig. 7.1 Marking

8. Land Pattern Dimensions (for reference only)

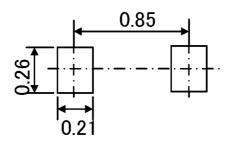


Fig. 8.1 Land Pattern Dimensions (Unit: mm)

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### 9. Characteristics Curves (Note)

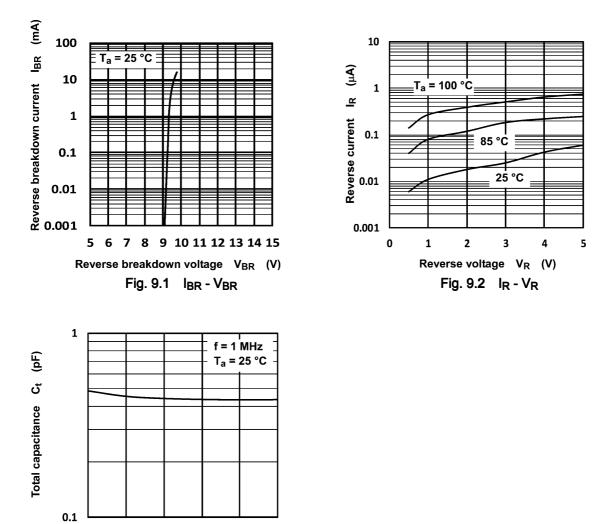
1

0

2

3

Reverse voltage  $V_R$  (V) Fig. 9.3  $C_t - V_R$ 



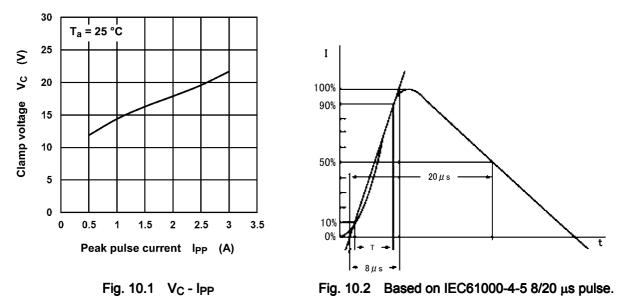
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

5

4

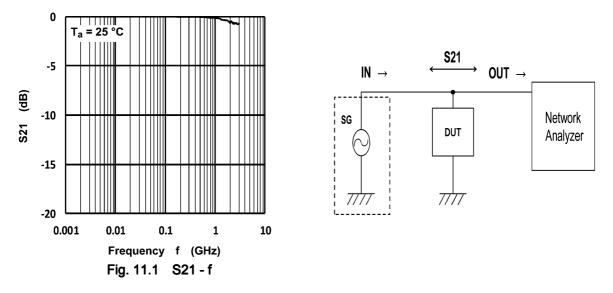
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10. Clamp Voltage V<sub>C</sub> - Peak Pulse Current (I<sub>PP</sub>) (Note)



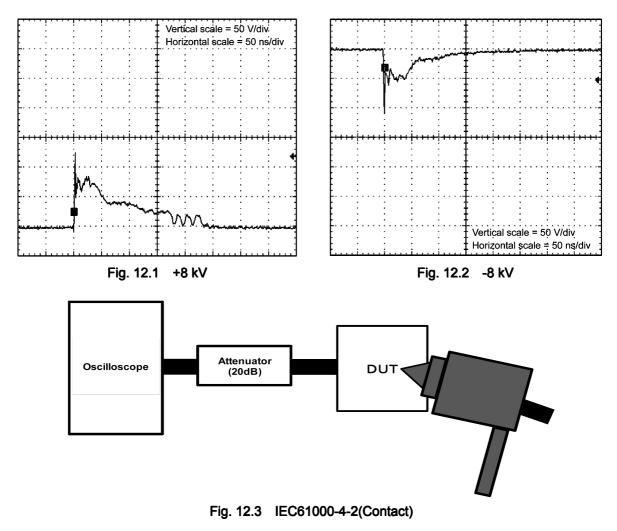
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

### 11. Insertion Loss (S21) (Note)



Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

### 12. ESD Clamp Waveform (Note)

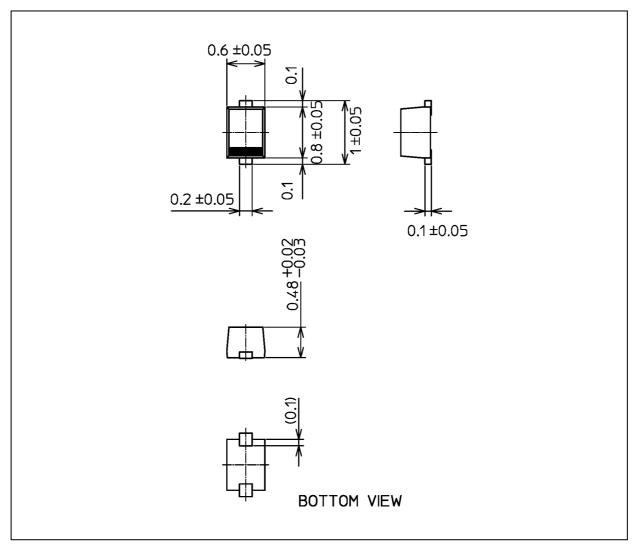


Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



### Package Dimensions

Unit: mm



Weight: 0.6 mg (typ.)

	Package Name(s)	
TOSHIBA: 1-1L1S		
Nickname: fSC		

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